



200MHZ 3-DIMM CLOCK FOR SOLANO CHIPSET

1.0 GENERAL DESCRIPTION

The W83195BR-25 is a Clock Synthesizer for Intel 815 Solano chipset. W83195BR-25 provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

The W83195BR-25 provides I²C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.25% and 0.5% center type spread spectrum to reduce EMI.

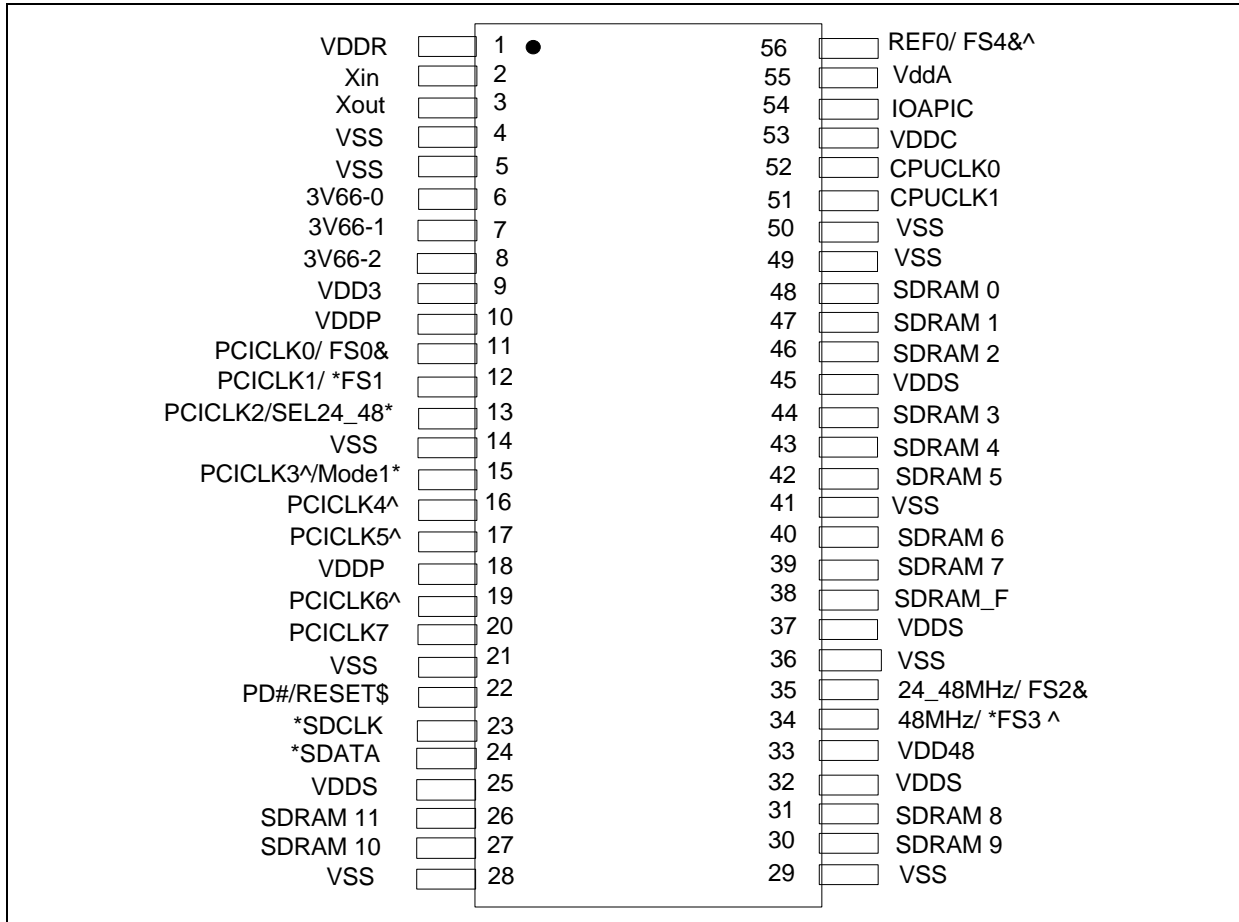
The W83195BR-25 provides stepless frequency programming by controlling the VCO freq. and the clock output divisor ratio. Also skew of CPU,SDRAM and 3V66 clock outputs are programmable. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

The W83195BR-25 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50±5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2.0 PRODUCT FEATURES

- 2 CPU clocks (2.5V)
- 3 3V-66 clocks (3.3V)
- 12 SDRAM clocks for 3 DIMMs(3.3V)
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
(VDDR = VDDP=VDDS = VDD48 = VDD3 = 3.3V, VDDA=VDDC=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200MHz
- I²C 2-Wire serial interface and I²C read back
- 0.25% center and 0.5% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
(mode as Tri-state or Normal)
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 56-pin SSOP

3.0 PIN CONFIGURATION



Note: * Internal pull-up

&: Internal pull-down

^ 1.5~2 strength

\$: Open drain

4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin



PRELIMINARY

- Active Low

* - Internal 250kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	2	IN	Crystal input with internal loading capacitors(36pF) and feedback resistors.
Xout	3	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors(36pF).

4.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:1]	52,51	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU and Chipset.
PD#/RESET\$	22	IN	Mode1*=1, Power Down mode when driven low. Mode1*=0, RESET# open drain (4ms low active pulse when Watch Dog time out)
IOAPIC	54	OUT	Clock outputs synchronous with PCI clock and powered by VddA.
SDRAM_F, SDRAM[0:11]	38, 48,47,46, 44,43,42,40, 39,31, 30,27, 26	OUT	SDRAM clock outputs.
PCICLK0/ FS0&	11	I/O	3.3V 33MHz PCI clock during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=0).
PCICLK1/ *FS1	12	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=1).
PCICLK2/ *SEL24_48	13	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for SEL24_48 at initial power up for the output frequency of 24MHz(HIGH) and 48MHz(LOW) clocks.
PCICLK3/ Mode1*	15	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for Mode* pin at initial power up for the output PD# /RESET# output selection.
PCICLK [4:7]	16,17,19,20	OUT	Low skew (< 250ps) PCI clock outputs.
3V66 [0:2]	6,7,8	OUT	3.3V output clocks for the chipset.

Publication Release Date: May 2000

Revision 0.52

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	24	I/O	Serial data of I ² C 2-wire control interface with internal pull-up resistor.
*SDCLK	23	IN	Serial clock of I ² C 2-wire control interface with internal pull-up resistor.

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 / FS4&	56	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=0).
24_48MHz/FS2&	35	I/O	24MHz or 48MHz output clock. Default is 24MHz. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks(Default=0).
48MHz/ FS3*	34	I/O	48MHz / Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks (Default=1).

4.5 Power Pins

SYMBOL	PIN	FUNCTION
VddC,VddA	53,55	Power supply for CPU & IOAPIC, 2.5V or 3.3V.
Vdd48	33	Power supply for 48MHz output,3.3V.
Vdd3	9	Power supply for 3V_66 output, 3.3V.
VddP	10,18	Power supply for PCICLK, 3.3V.
VddR	1	Power supply for REF0, 3.3V.
VddS	45,37,32,25	Power supply for SDRAM_F,SDRAM[0:11], nominal 3.3V.
Vss	4,5,14,21,28,29,36,41, 49.50	Circuit Ground.



PRELIMINARY

5.0 Frequency Selection BY hardware

FS4	FS3	FS2	FS1	FS0	CPU(MHz)	SDRAM(MHz)	3V66(MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	55.00	82.50	55.00	27.50	13.75
0	0	0	0	1	60.00	90.00	60.00	30.00	15.00
0	0	0	1	0	66.80	100.20	66.80	33.40	16.70
0	0	0	1	1	68.33	102.50	68.33	34.17	17.08
0	0	1	0	0	70.00	105.00	70.00	35.00	17.50
0	0	1	0	1	72.00	108.00	72.00	36.00	18.00
0	0	1	1	0	75.00	112.50	75.00	37.50	18.75
0	0	1	1	1	77.00	115.50	77.00	38.50	19.25
0	1	0	0	0	83.30	83.30	55.53	27.77	13.88
0	1	0	0	1	90.00	90.00	60.00	30.00	15.00
0	1	0	1	0	100.30	100.30	66.87	33.43	16.72
0	1	0	1	1	103.00	103.00	68.67	34.33	17.17
0	1	1	0	0	112.50	112.50	75.00	37.50	18.75
0	1	1	0	1	115.00	115.00	76.67	38.33	19.17
0	1	1	1	0	120.00	120.00	80.00	40.00	20.00
0	1	1	1	1	125.00	125.00	83.33	41.67	20.83
1	0	0	0	0	128.00	128.00	64.00	32.00	16.00
1	0	0	0	1	130.00	130.00	65.00	32.50	16.25
1	0	0	1	0	133.70	133.70	66.85	33.43	16.71
1	0	0	1	1	137.00	137.00	68.50	34.25	17.13
1	0	1	0	0	140.00	140.00	70.00	35.00	17.50
1	0	1	0	1	145.00	145.00	72.50	36.25	18.13
1	0	1	1	0	150.00	150.00	75.00	37.50	18.75
1	0	1	1	1	153.33	153.33	76.67	38.33	19.17
1	1	0	0	0	125.00	93.75	62.50	31.25	15.63
1	1	0	0	1	130.00	97.50	65.00	32.50	16.25
1	1	0	1	0	133.70	100.28	66.85	33.43	16.71
1	1	0	1	1	137.00	102.75	68.50	34.25	17.13
1	1	1	0	0	140.00	105.00	70.00	35.00	17.50
1	1	1	0	1	145.00	108.75	72.50	36.25	18.13
1	1	1	1	0	150.00	112.50	75.00	37.50	18.75
1	1	1	1	1	153.33	115.00	76.67	38.33	19.17



PRELIMINARY

6. SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2,) will be valid and acknowledged.

Frequency Table Setting by I2C (SEL5 ~ SEL0)

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	0	55.00	82.50	55.00	27.50	13.75
0	0	0	0	0	1	60.00	90.00	60.00	30.00	15.00
0	0	0	0	1	0	66.80	100.20	66.80	33.40	16.70
0	0	0	0	1	1	68.33	102.50	68.33	34.17	17.08
0	0	0	1	0	0	70.00	105.00	70.00	35.00	17.50
0	0	0	1	0	1	72.00	108.00	72.00	36.00	18.00
0	0	0	1	1	0	75.00	112.50	75.00	37.50	18.75
0	0	0	1	1	1	77.00	115.50	77.00	38.50	19.25
0	0	1	0	0	0	83.30	83.30	55.53	27.77	13.88
0	0	1	0	0	1	90.00	90.00	60.00	30.00	15.00
0	0	1	0	1	0	100.30	100.30	66.87	33.43	16.72
0	0	1	0	1	1	103.00	103.00	68.67	34.33	17.17
0	0	1	1	0	0	112.50	112.50	75.00	37.50	18.75
0	0	1	1	0	1	115.00	115.00	76.67	38.33	19.17
0	0	1	1	1	0	120.00	120.00	80.00	40.00	20.00
0	0	1	1	1	1	125.00	125.00	83.33	41.67	20.83
0	1	0	0	0	0	128.00	128.00	64.00	32.00	16.00
0	1	0	0	0	1	130.00	130.00	65.00	32.50	16.25
0	1	0	0	1	0	133.70	133.70	66.85	33.43	16.71
0	1	0	0	1	1	137.00	137.00	68.50	34.25	17.13
0	1	0	1	0	0	140.00	140.00	70.00	35.00	17.50
0	1	0	1	0	1	145.00	145.00	72.50	36.25	18.13
0	1	0	1	1	0	150.00	150.00	75.00	37.50	18.75
0	1	0	1	1	1	153.33	153.33	76.67	38.33	19.17
0	1	1	0	0	0	125.00	93.75	62.50	31.25	15.63
0	1	1	0	0	1	130.00	97.50	65.00	32.50	16.25
0	1	1	0	1	0	133.70	100.28	66.85	33.43	16.71
0	1	1	0	1	1	137.00	102.75	68.50	34.25	17.13
0	1	1	1	0	0	140.00	105.00	70.00	35.00	17.50
0	1	1	1	0	1	145.00	108.75	72.50	36.25	18.13



PRELIMINARY

0	1	1	1	1	0	150.00	112.50	75.00	37.50	18.75
0	1	1	1	1	1	153.33	115.00	76.67	38.33	19.17
SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz)
1	0	0	0	0	0	66.8	133.00	66.80	33.40	16.70
1	0	0	0	0	1	135.00	135.00	67.50	33.75	16.88
1	0	0	0	1	0	142.00	142.00	71.00	35.50	17.75
1	0	0	0	1	1	143.00	143.00	71.50	35.75	17.88
1	0	0	1	0	0	144.00	144.00	72.00	36.00	18.00
1	0	0	1	0	1	146.00	146.00	73.00	36.50	18.25
1	0	0	1	1	0	147.00	147.00	73.50	36.75	18.38
1	0	0	1	1	1	148.00	148.00	74.00	37.00	18.50
1	0	1	0	0	0	100.20	133.00	66.80	33.40	16.70
1	0	1	0	0	1	156.00	156.00	78.00	39.00	19.50
1	0	1	0	1	0	158.00	158.00	79.00	39.50	19.75
1	0	1	0	1	1	160.00	160.00	80.00	40.00	20.00
1	0	1	1	0	0	135.00	101.25	67.50	33.75	16.88
1	0	1	1	0	1	139.00	104.25	69.50	34.75	17.38
1	0	1	1	1	0	141.00	105.75	70.50	35.25	17.63
1	0	1	1	1	1	142.00	106.50	71.00	35.50	17.75
1	1	0	0	0	0	143.00	107.25	71.50	35.75	17.88
1	1	0	0	0	1	144.00	108.00	72.00	36.00	18.00
1	1	0	0	1	0	146.00	109.50	73.00	36.50	18.25
1	1	0	0	1	1	147.00	110.25	73.50	36.75	18.38
1	1	0	1	0	0	148.00	111.00	74.00	37.00	18.50
1	1	0	1	0	1	149.00	111.75	74.50	37.25	18.63
1	1	0	1	1	0	153.00	114.75	76.50	38.25	19.13
1	1	0	1	1	1	157.00	117.75	78.50	39.25	19.63
1	1	1	0	0	0	159.00	119.25	79.50	39.75	19.88
1	1	1	0	0	1	162.00	121.50	81.00	40.50	20.25
1	1	1	0	1	0	164.00	123.00	82.00	41.00	20.50
1	1	1	0	1	1	170.00	127.50	85.00	42.50	21.25
1	1	1	1	0	0	175.00	116.67	58.30	29.15	14.58
1	1	1	1	0	1	180.00	120.00	60.00	30.00	15.00
1	1	1	1	1	0	190.00	190.00	63.33	31.67	15.83
1	1	1	1	1	1	200.40	133.60	66.80	33.40	16.70

PRELIMINARY

6.1 Register 0: CPU Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I ² C)
6	0	-	SSEL2 (Frequency table selection by software via I ² C)
5	0	-	SSEL1 (Frequency table selection by software via I ² C)
4	0	-	SSEL0 (Frequency table selection by software via I ² C)
3	0	-	0 = Selection by hardware 1 = Selection by software I ² C - Bit (2, 7:4)
2	0	-	SSEL4 (Frequency table selection by software via I ² C)
1	0	-	SSEL5 (Frequency table selection by software via I²C)
0	0	-	0 = Running 1 = Tristate all outputs

6.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	X	-	FS0#
6	X	-	FS1#
5	X	-	FS2#
4	X	-	FS3#
3	X	-	FS4#
2	0	-	1 = ±0.25% Center type Spread Spectrum Modulation 0 = ±0.5% Center type Spread Spectrum Modulation
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	1	-	1 = Center type Spread Spectrum Modulation 0 = Down type Spread Spectrum Modulation

6.3 Register 2: SDRAM Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	39	SDRAM7 (Active / Inactive)
6	1	40	SDRAM6 (Active / Inactive)
5	1	42	SDRAM5 (Active / Inactive)
4	1	43	SDRAM4 (Active / Inactive)
3	1	44	SDRAM3 (Active / Inactive)
2	1	46	SDRAM2 (Active / Inactive)
1	1	47	SDRAM1 (Active / Inactive)
0	1	48	SDRAM0 (Active / Inactive)

6.4 Register 3: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	20	PCICLK7 (Active / Inactive)
6	1	19	PCICLK6 (Active / Inactive)
5	1	17	PCICLK5 (Active / Inactive)
4	1	16	PCICLK4 (Active / Inactive)
3	1	15	PCICLK3 (Active / Inactive)
2	1	13	PCICLK2 (Active / Inactive)
1	1	12	PCICLK1 (Active / Inactive)
0	1	11	PCICLK0 (Active / Inactive)

6.5 Register 4: Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	8	3V66_2(Active / Inactive)
6	1	7	3V66_1(Active / Inactive)
5	1	6	3V66_0(Active / Inactive)
4	1	26	SDRAM11 (Active / Inactive)
3	1	27	SDRAM10 (Active / Inactive)
2	1	30	SDRAM9 (Active / Inactive)
1	1	31	SDRAM8(Active / Inactive)
0	1	38	SDRAM_F (Active / Inactive)

6.6 Register 5: SDRAM Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	CSkew2 (CPU to SDRAM skew program bit)
6	0	-	CSkew1 (CPU to SDRAM skew program bit)
5	0	-	CSkew0 (CPU to SDRAM skew program bit)
4	1	-	CASkew2 (CPU to 3V66 skew program bit)
3	0	-	CASkew1 (CPU to 3V66 skew program bit)
2	0	-	CASkew0 (CPU to 3V66 skew program bit)
1	1	51	CPUCLK1(Active / Inactive)
0	1	52	CPUCLK0(Active / Inactive)



PRELIMINARY

6.7 Register 6~10: Step-less M/N mode control Register

6.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

6.14 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Version ID
2	0	-	Winbond Version ID
1	1	-	Winbond Version ID
0	0	-	Winbond Version ID

Register10 Bit3-6				Ratio		
Bit6	Bit 5	Bit 4	Bit 3			
DS3	DS2	DS1	DS0	CPU	SDRAM	3V66
0	0	0	0	4	4	6
0	0	0	1	3	3	6
0	0	1	0	2	3	6



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0	0	1	1	2	2	6
0	1	0	0	6	4	6
0	1	0	1	3	4	6
0	1	1	0	6	3	6
0	1	1	1	4	3	6
1	0	x	x	2	2	4
1	1	x	x	2	4	6

7.0 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , VIN	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T _{STG}	Storage Temperature	- 65°C to + 150°C
T _B	Ambient Temperature	- 55°C to + 125°C
T _A	Operating Temperature	0°C to + 70°C

7.2 Electrical Characteristics---Input/Output

Vddq1=Vddq2 = Vddq3 = Vddq4 =3.3V, VddL1 =VddL2= 2.5V , T _A = 0° C to +70° C						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions

PRELIMINARY

Input Low Voltage	V_{IL}	$V_{ss}-0.3$		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		$V_{dd}+0.3$	V_{dc}	
Input Low Current	I_{IL}	-5			μA	No pull-up resistors
Input Low Current	I_{IL}	-200			μA	Pull-up resistors
Input High Current	I_{IH}	-5		5	μA	
Input Capacitance	C_{IN}			5	pF	Logic inputs
	C_{OUT}			6	pF	Output capacitance
	C_{INX}	27		45	pF	Xin and Xout
Operating Supply Current	I_{dd3}			100	MA	CPU = 66.6 MHz PCI = 33.3 Mhz with load
Power Down Supply Current	I_{dd2}			600	μA	
Settling Time	T_s			3	mS	From first crossing to 1% target freq.
Delay	t_{PZH}, t_{PZH}	1		10	nS	Output enable delay
	t_{PLZ}, t_{PZH}	1		10	nS	Output enable delay

7.3 Electrical Characteristics of CPU Clock

$V_{dd}=2.5V \pm 5\%$; $C_L=10-20pF$

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R_{DSP}	13.5		40	Ohm	
Output Impedance	R_{DSN}	13.5		40	Ohm	
Output Low Voltage	V_{OL}			0.4	V	$I_{OL}=1mA$
Output High Voltage	V_{OH}	2.0			V	$I_{OH}=-1mA$
Output Low Current	I_{OL}	27		30	MA	
Output High Current	I_{OH}	-27		-27	MA	
Pull-Up Current Min	$I_{OH(min)}$	-27			MA	$V_{out} = 1.0 V$
Pull-Up Current Max	$I_{OH(max)}$			-27	MA	$V_{out} = 2.0V$
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{RF(min)}$	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{RF(max)}$			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	$V_T=1.25V$
Skew	T_{SK}			175	ps	$V_T=1.25V$
Jitter	T_{sc-c}			250	ps	$V_T=1.25V$

PRELIMINARY

7.4 Electrical Characteristics of 3V66 Clock

V_{dd}=3.3V +/- 5%; C_L=10-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	15		55	Ohm	
Output Impedance	R _{DSN}	15		55	Ohm	
Output Low Voltage	V _{OL}			0.55	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} =-1mA
Output Low Current	I _{OL}	30		38	MA	
Output High Current	I _{OH}	-33		-33	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T _{RF(min)}	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T _{RF(max)}			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	V _T =1.5V
Skew	T _{SK}			175	ps	V _T =1.5V
Jitter	T _{SC-C}			500	ps	V _T =1.5V

7.5 Electrical Characteristics of SDRAM Clock

V_{dd}=3.3V +/- 5%; C_L=20-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	13.5		40	Ohm	
Output Impedance	R _{DSN}	13.5		40	Ohm	
Output Low Voltage	V _{OL}			0.45	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} =-1mA
Output Low Current	I _{OL}	54		54	MA	
Output High Current	I _{OH}	-54		-45	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T _{RF(min)}	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T _{RF(max)}			1.6	ns	20pF Load
Duty Cycle	Dt	45		55	%	V _T =1.5V
Skew	T _{SK}			250	ps	V _T =1.5V
Jitter	T _{SC-C}			250	ps	V _T =1.5V

PRELIMINARY

7.6 Electrical Characteristics of PCI Clock

V_{dd}=3.3V +/- 5%; C_L=10-30pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	15		55	Ohm	
Output Impedance	R _{DSN}	15		55	Ohm	
Output Low Voltage	V _{OL}			0.55	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} =-1mA
Output Low Current	I _{OL}	30		38	MA	
Output High Current	I _{OH}	-33		-33	MA	
Rise/Fall Time Min Between 0.4 V and 2.0 V	T _{RF(min)}	0.5			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	T _{RF(max)}			2.0	ns	20pF Load
Duty Cycle	Dt	45		55	%	V _T =1.5V
Skew	T _{SK}			500	ps	V _T =1.5V
Jitter	T _{SC-C}			500	ps	V _T =1.5V

7.7 Electrical Characteristics of 48MHz, REF Clock

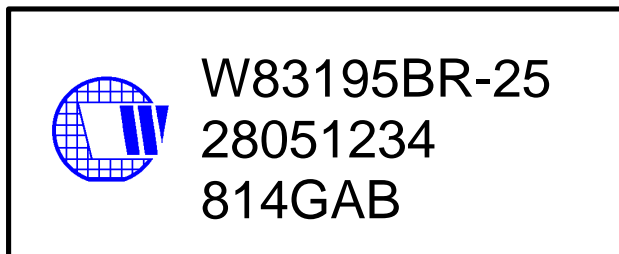
V_{dd}=3.3V +/- 5%; C_L=10-20pF

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Impedance	R _{DSP}	20		55	Ohm	
Output Impedance	R _{DSN}	20		55	Ohm	
Output Low Voltage	V _{OL}			0.4	V	I _{OL} =1mA
Output High Voltage	V _{OH}	2.4			V	I _{OH} =-1mA
Output Low Current	I _{OL}	29		27	MA	
Output High Current	I _{OH}	-29		-23	MA	
RiseTime	T _R		1.8	4	ns	10pF Load
Fall Time	T _F		1.7	4	ns	20pF Load
Duty Cycle	Dt	45		55	%	V _T =1.5V
Skew	T _{SK}			500	ps	V _T =1.5V
Jitter	T _{SC-C}			1000	ps	V _T =1.5V

8.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83195BR-25	56 PIN SSOP	Commercial, 0°C to +70°C

9.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83195BR-25

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G A B

814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code



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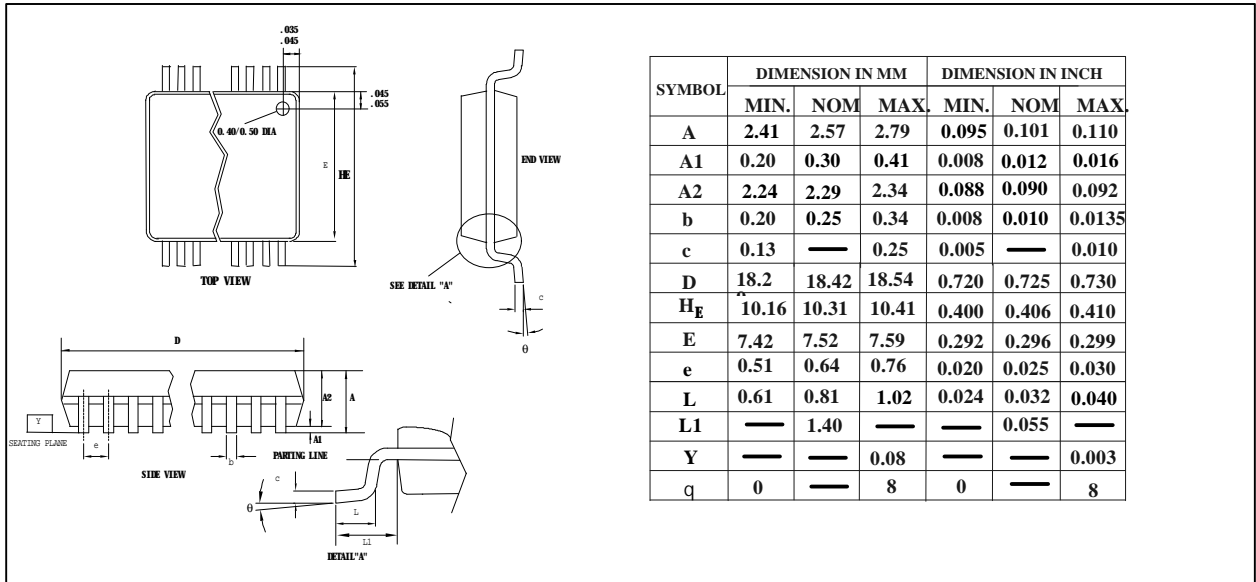
B: IC revision

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10.0 PACKAGE DRAWING AND DIMENSIONS



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Publication Release Date: May 2000

Revision 0.52



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