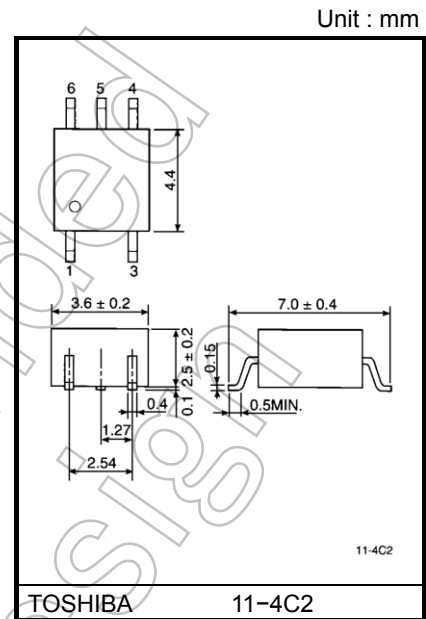


TLP115A

High Speed, Long Distance Isolated Line Receiver
 Microprocessor System Interfaces
 Digital Isolation For A / D, D / A Conversion
 Computer-Peripheral Interfaces
 Ground Loop Elimination

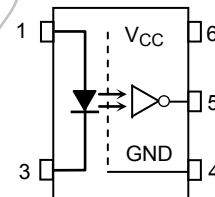
The TOSHIBA mini flat coupler TLP115A is a small outline coupler, suitable for surface mount assembly. TLP115A consists of a high output power GaAlAs light emitting diode, optically coupled to an integrated high gain, high speed shielded photo detector whose output is an open collector schottky clamped transistor. The shield, which shunts capacitively coupled common noise to ground, provides a guaranteed transient immunity specification of 1000V / μ s. TLP115A : Mini Flat Package, 5Pin, one circuit.

- Input current thresholds: $I_F = 5\text{mA}$ (max)
- Switching speed: 10MBd (typ.)
- Common mode transient immunity: $\pm 1000\text{V} / \mu\text{s}$ (min)
- Guaranteed performance over temp. : 0 to 70°C
- Isolation voltage: 2500Vrms (min)
- UL recognized: UL1577, file no. E67349
- c UL approved :CSA Component Acceptance Service No. 5A, File No.E67349



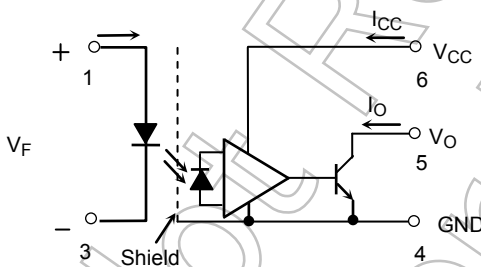
Weight: 0.09 g (typ.)

Pin Configuration (top view)



- 1 : Anode
- 3 : Cathode
- 4 : GND
- 5 : V_O (Open Collector Output)
- 6 : V_{CC}

Schematic



Note. A 0.1 μ F bypass capacitor must be connected between pins 4 and 6.

Truth Table (positive logic)

Input	Output
H	L
L	H

Start of commercial production
 1990-02

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I _F	20	mA
	Forward current derating (Ta ≥ 70 °C)	ΔIF/°C	0.36	mA/°C
	Pulse forward current (Note 1)	I _{FP}	40	mA
	Peak transient forward current (Note 2)	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
	Input power dissipation	PD	40	mW
	Input power dissipation derating (Ta ≥ 70 °C)	ΔPD/°C	-0.73	mW/°C
Detector	Output current	I _O	25	mA
	Output voltage	V _O	7	V
	Supply voltage(60 s maximum)	V _{CC}	7	V
	Output power dissipation	P _o	40	mW
	Output power dissipation derating (Ta ≥ 85 °C)	ΔP _o /°C	-2.6	mW/°C
Operating temperature range		T _{opr}	-40 to 85	°C
Storage temperature range		T _{stg}	-55 to 125	°C
Lead solder temperature(10 s.)		T _{sol}	260	°C
Isolation voltage(AC, 60 s., RH≤ 60%) (Note 3)		BV _S	2500	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1): 50% duty cycle, 1ms pulse width. Derate 0.72mA / °C above 70°C.

(Note 2): Pulse width ≤ 1μs, 300pps.

(Note 3): Device considered a two-terminal device: Pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Input voltage, low level	V _{FL}	-3	0	1.0	V
Input current, high level	I _{FH}	6.3*	8	20	mA
Supply voltage	V _{CC}	4.5	5	5.5	V
Fan out (TTL load)	N	—	—	8	—
Operating temperature	T _{opr}	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

*: 6.3mA is a value considering 20% CTR deterioration.

Initial input current threshold value is 5mA or less.

Electrical Characteristics (unless otherwise specified, Ta = 0 to 70°C, VCC = 4.5 to 5.5V, VFL ≤ 1.0V)

Characteristic	Symbol	Test Condition	Min	Typ.*	Max	Unit
Forward voltage	V _F	I _F = 10mA, Ta = 25°C	1.2	1.4	1.7	V
Forward voltage temperature coefficient	ΔV _F /ΔTa	I _F = 10mA	—	-2.0	—	mV/°C
Reverse current	I _R	V _R = 3V, Ta = 25°C	—	—	10	μA
Capacitance between terminals	C _T	V _F = 0V, f = 1MHz, Ta = 25°C	—	30	—	pF
High level output voltage	I _{OH}	V _F = 1.0, V _O = 5.5V	—	—	250	μA
		V _F = 1.0, V _O = 5.5V, Ta = 25°C	—	0.5	10	
Low level output current	V _{OL}	I _F = 5mA, I _{OL} = 13mA (sinking)	—	0.4	0.6	V
"H level output→L level output" input current	I _{FH}	I _{OL} = 13mA (sinking) V _{OL} = 0.6V	—	—	5	mA
High level supply current	I _{CCH}	V _{CC} = 5.5V, I _F = 0mA	—	7	15	mA
Low level supply current	I _{CCL}	V _{CC} = 5.5V, I _F = 10mA	—	12	19	mA
Isolation resistance	R _S	R.H. ≤ 60%, V _S = 500V DC Ta = 25°C (Note 1)	5×10 ¹⁰	10 ¹⁴	—	Ω
Stray capacitance between input to output	C _S	V _S = 0V, f = 1MHz, Ta = 25°C	—	0.8	—	pF

* All typical values are V_{CC} = 5V, Ta = 25°C.

(Note): The V_{CC} supply voltage to each TLP115A isolator must be bypassed by 0.1μF capacitor. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to package V_{CC} and GND pins of each device.

(Note 1): Device considered a two-terminal device: Pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.

Switching Characteristics (VCC = 5V, Ta = 25°C)

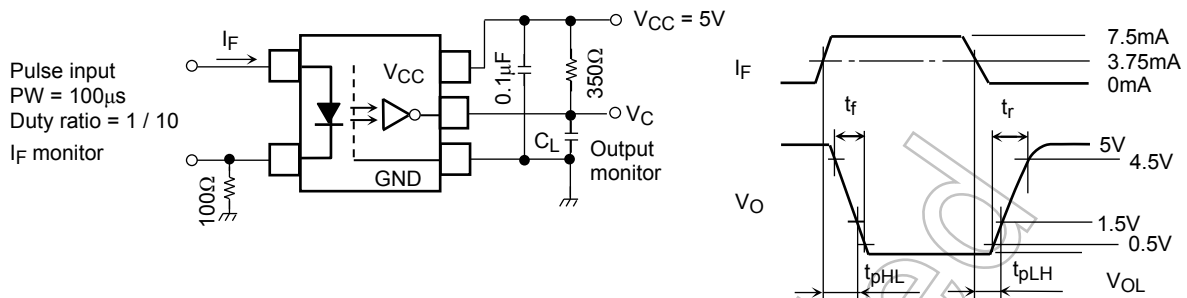
Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t _{pHL}	1	I _F = 0→7.5mA C _L = 15pF, R _L = 350Ω	—	60	120	ns
Propagation delay time (L→H)	t _{pLH}	1	I _F = 7.5mA→0 C _L = 15pF, R _L = 350Ω	—	60	120	ns
Output rise fall time(10~90%)	t _r , t _f	1	R _L = 350, C _L = 15pF I _F = 0 ⇄ 7.5mA	—	30	—	ns
Common mode transient immunity at high output level	CM _H	2	I _F = 0 mA, V _{CM} = 400V _{p-p} , V _{O(MIN)} =2V R _L = 350Ω (Note 1)	1000	—	—	V / μs
Common mode transient immunity at low output level	CM _L	2	I _F = 7.5 mA, V _{CM} = 400V _{p-p} V _{O(MAX)} = 0.8V, R _L = 350Ω (Note 2)	-1000	—	—	V / μs

(Note): Maximum electrostatic discharge voltage for any pins: 180V(C = 200pF, R = 0)

(Note 1): CM_H is the maximum rising common mode voltage waveform (voltage/time) that can keep high level (V_O > 2.0 V).

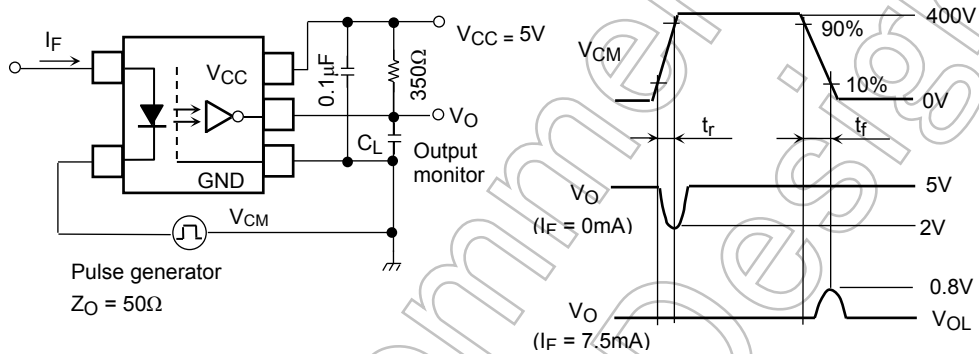
(Note 2): CM_L is the maximum falling common mode voltage waveform (voltage/time) that can keep low level (V_O < 0.8 V).

Test Circuit 1: Switching Time Test Circuit



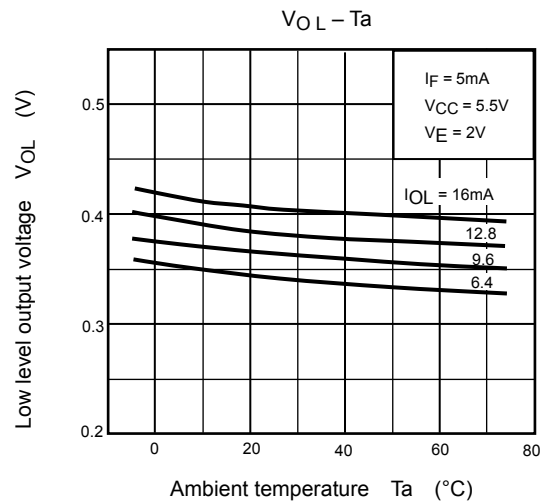
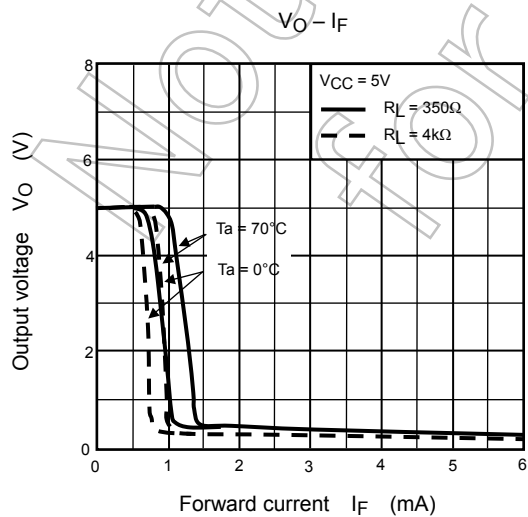
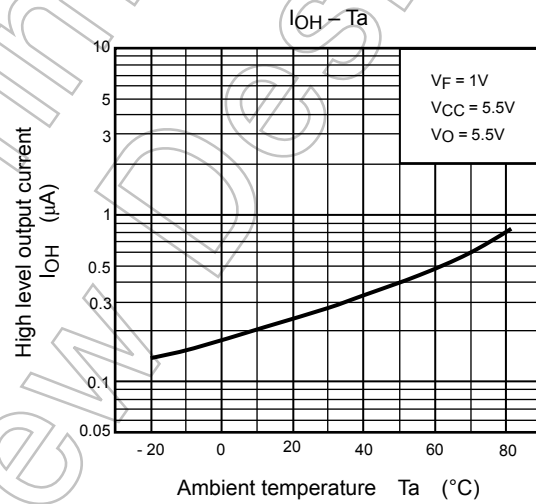
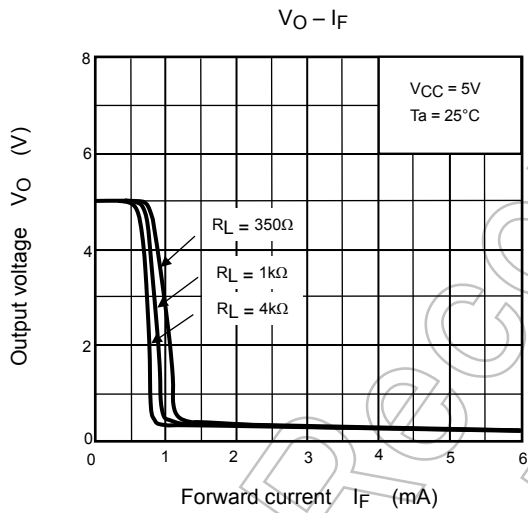
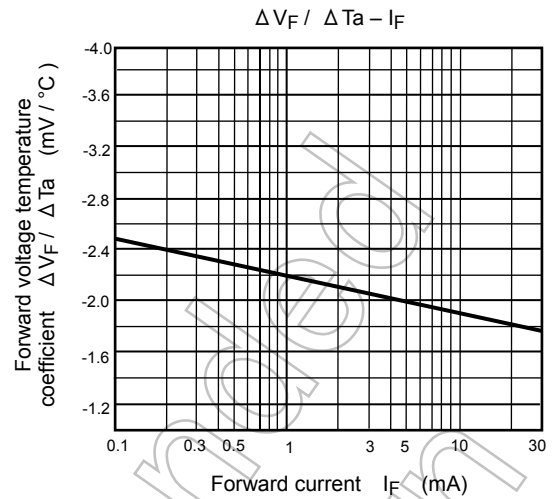
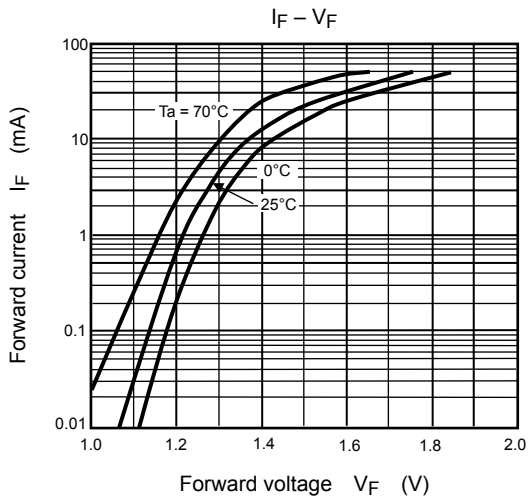
C_L is approximately 15pF which includes probe and stray wiring capacitance.

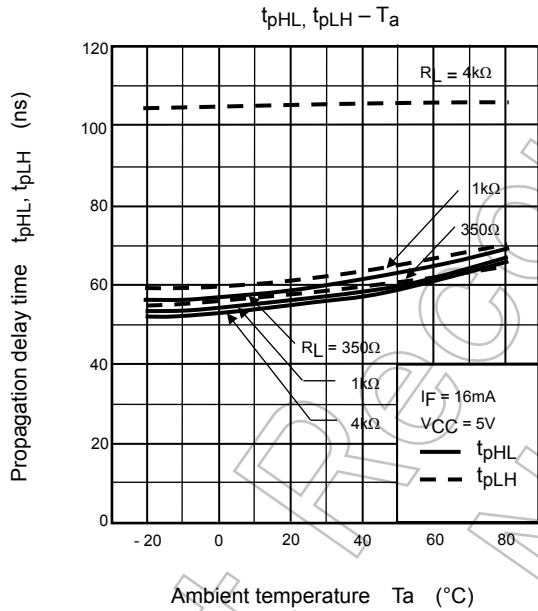
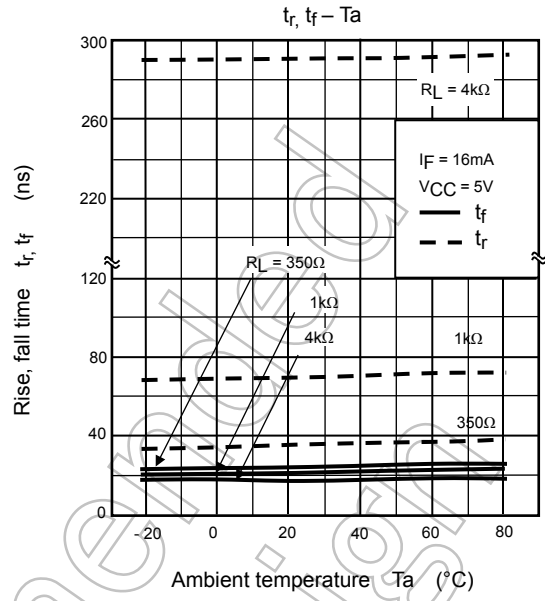
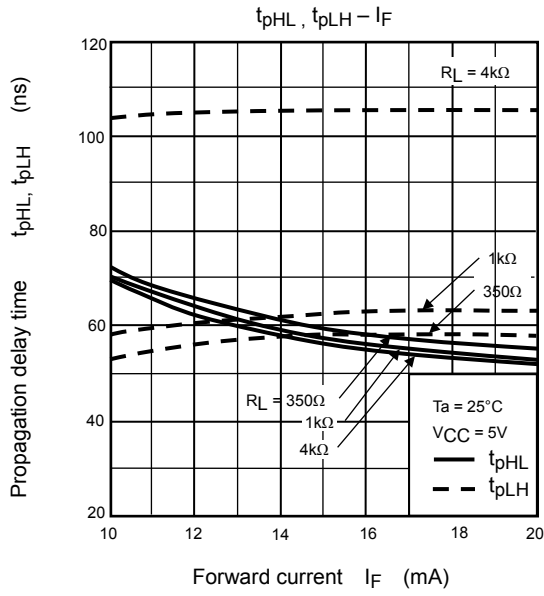
Test Circuit 2: Common Mode Transient Immunity Test Circuit



$$CM_H = \frac{320 \text{ (V)}}{t_r \text{ (}\mu\text{s)}}, CM_L = \frac{320 \text{ (V)}}{t_f \text{ (}\mu\text{s)}}$$

C_L is approximately 15pF which includes probe and stray wiring capacitance.





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