

# MMDF2N02E

## Power MOSFET 2 Amps, 25 Volts N-Channel SO-8, Dual

These miniature surface mount MOSFETs feature ultra low  $R_{DS(on)}$  and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain-to-source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc-dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

### Features

- Ultra Low  $R_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- $I_{DSS}$  Specified at Elevated Temperatures
- Avalanche Energy Specified
- Mounting Information for SO-8 Package Provided
- Pb-Free Package is Available

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	25	Vdc
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	Vdc
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ – Continuous @ $T_A = 100^\circ\text{C}$ – Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_D$	3.6	A dc
	$I_D$	2.5	
	$I_{DM}$	18	A pk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)	$P_D$	2.0	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 20 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , Peak $I_L = 9.0 \text{ Apk}$ , $L = 6.0 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	245	mJ
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 0.0625" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

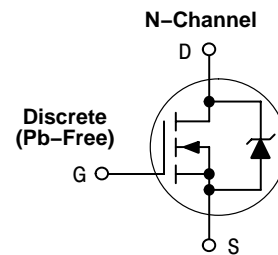


ON Semiconductor®

<http://onsemi.com>

**2 AMPERES, 25 VOLTS**

**$R_{DS(on)} = 100 \text{ m}\Omega$**

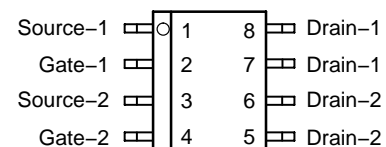


### MARKING DIAGRAM



F2N02 = Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
MMDF2N02ER2	SO-8	2500 Tape & Reel
MMDF2N02ER2G	SO-8 (Pb-Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MMDF2N02E

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc)	V <sub>(BR)DSS</sub>	25	–	–	Vdc
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	–	–	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	–	–	100	nAdc

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc)	V <sub>GS(th)</sub>	1.0	2.0	3.0	Vdc
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 2.2 Adc) (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 1.0 Adc)	R <sub>DS(on)</sub>	–	0.083 0.110	0.100 0.200	Ω
Forward Transconductance (V <sub>DS</sub> = 3.0 Vdc, I <sub>D</sub> = 1.0 Adc)	g <sub>FS</sub>	1.0	2.6	–	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 16 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	–	380	532	pF
Output Capacitance		C <sub>oss</sub>	–	235	329	
Transfer Capacitance		C <sub>rss</sub>	–	55	110	

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	(V <sub>DD</sub> = 10 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	–	7.0	21	ns
Rise Time		t <sub>r</sub>	–	17	30	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	27	48	
Fall Time		t <sub>f</sub>	–	18	30	
Turn-On Delay Time	(V <sub>DD</sub> = 10 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 4.5 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	–	10	30	ns
Rise Time		t <sub>r</sub>	–	35	70	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	19	38	
Fall Time		t <sub>f</sub>	–	25	50	
Gate Charge	(V <sub>DS</sub> = 16 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	–	10.6	30	nC
		Q <sub>1</sub>	–	1.3	–	
		Q <sub>2</sub>	–	2.9	–	
		Q <sub>3</sub>	–	2.7	–	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (Note 2)	(I <sub>S</sub> = 2.0 Adc, V <sub>GS</sub> = 0 Vdc)	V <sub>SD</sub>	–	1.0	1.4	Vdc
Reverse Recovery Time See Figure 11	(I <sub>S</sub> = 2.0 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	–	34	66	ns
		t <sub>a</sub>	–	17	–	
		t <sub>b</sub>	–	17	–	
Reverse Recovery Storage Charge		Q <sub>RR</sub>	–	0.03	–	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

# M MDF2N02E

## TYPICAL ELECTRICAL CHARACTERISTICS

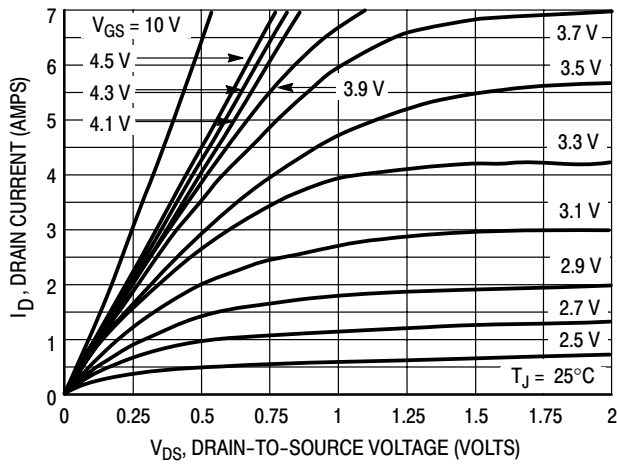


Figure 1. On-Region Characteristics

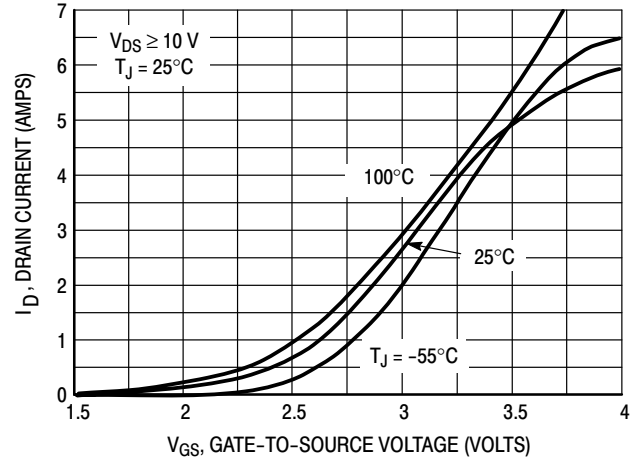


Figure 2. Transfer Characteristics

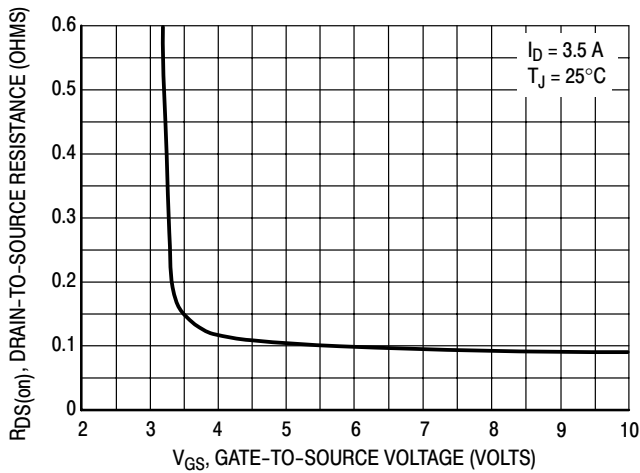


Figure 3. On-Resistance versus Gate-to-Source Voltage

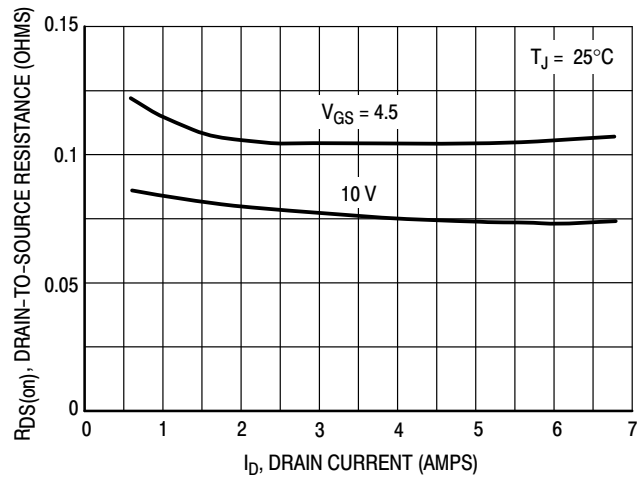


Figure 4. On-Resistance versus Drain Current and Gate Voltage

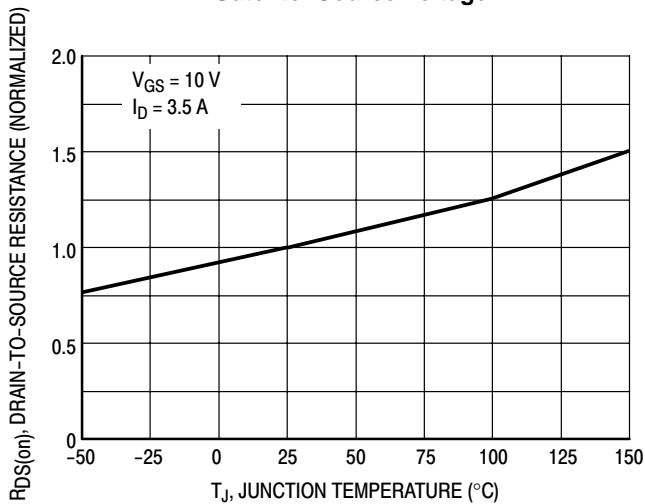


Figure 5. On-Resistance Variation with Temperature

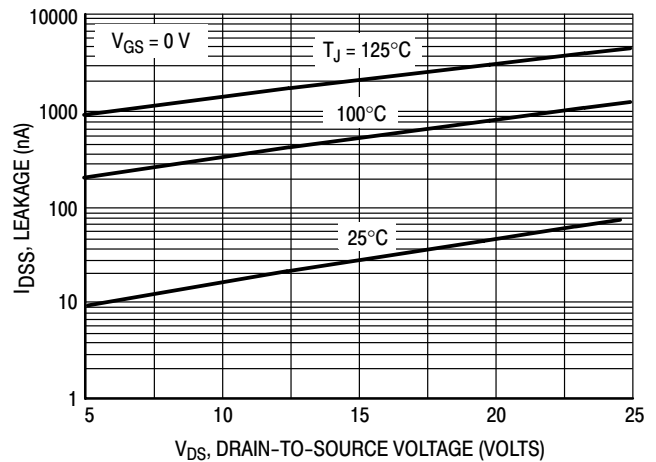


Figure 6. Drain-to-Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that:

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{GS(P)}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{GS(P)})$$

$$t_f = Q_2 \times R_G / V_{GS(P)}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance and  $Q_2$  and  $V_{GS(P)}$  are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG} / (V_{GG} - V_{GS(P)})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG} / V_{GS(P)})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on-state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $L di/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

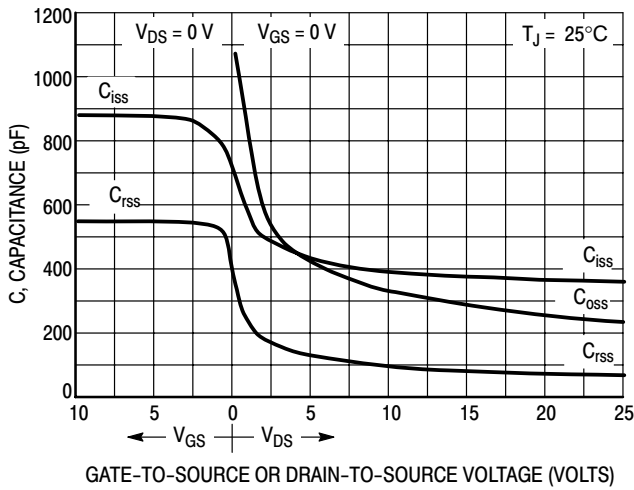


Figure 7. Capacitance Variation

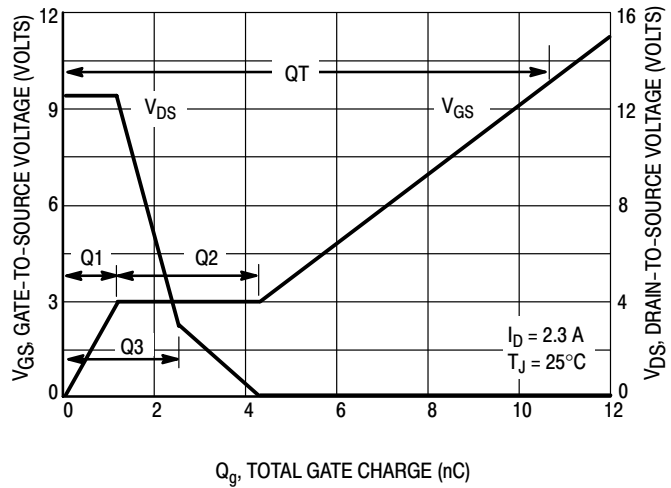
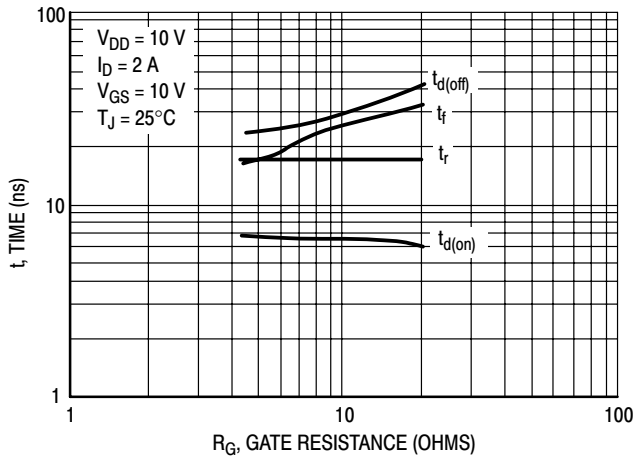
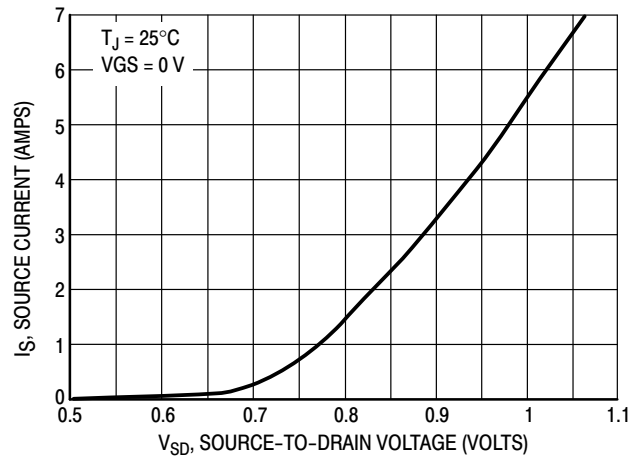


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

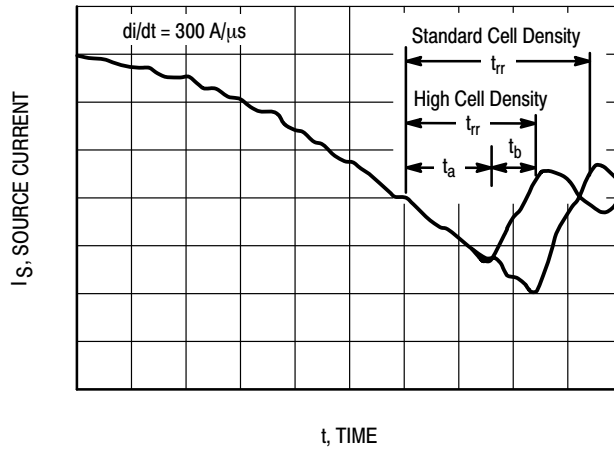
# MMDF2N02E



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**



**Figure 11. Reverse Recovery Time ( $t_{rr}$ )**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of  $25^\circ\text{C}$ . Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded, and that the transition time ( $t_r$ ,  $t_f$ ) does not exceed  $10\ \mu\text{s}$ . In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(MAX)} - T_C)/(R_{\theta JC})$ .

A power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For

reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

# MMDF2N02E

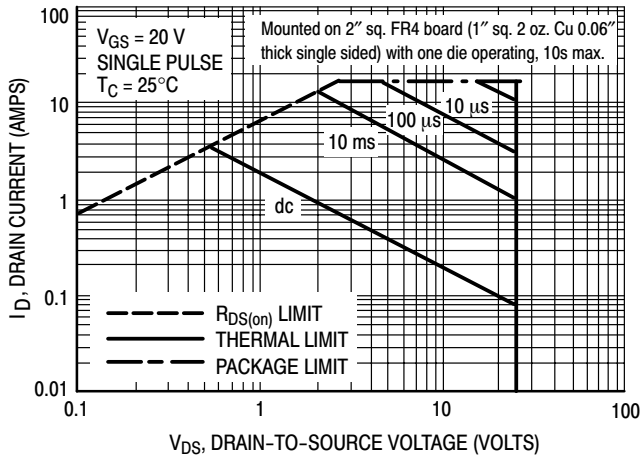


Figure 12. Maximum Rated Forward Biased Safe Operating Area

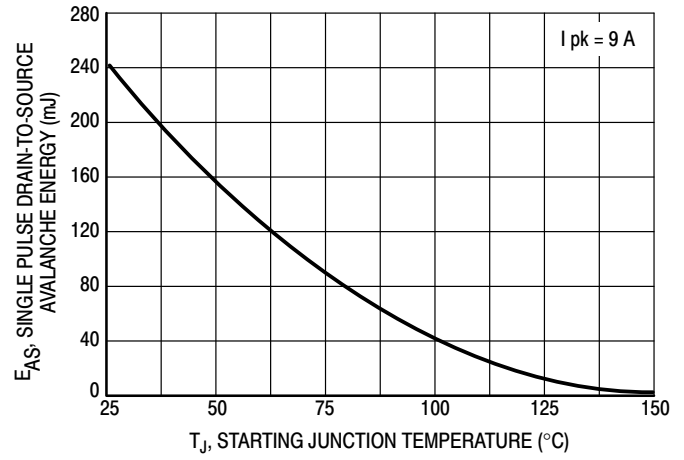


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

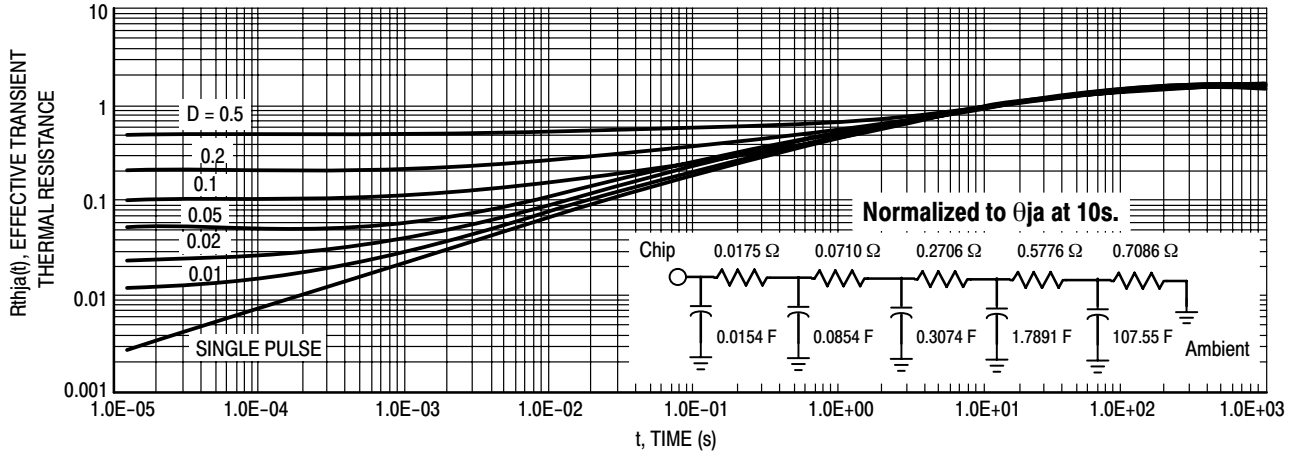


Figure 14. Thermal Response

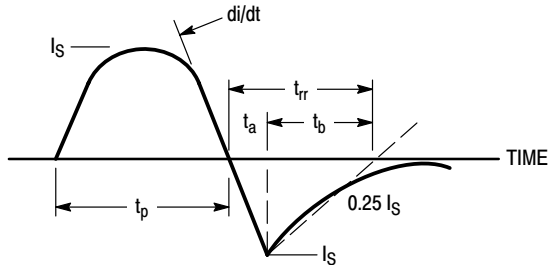
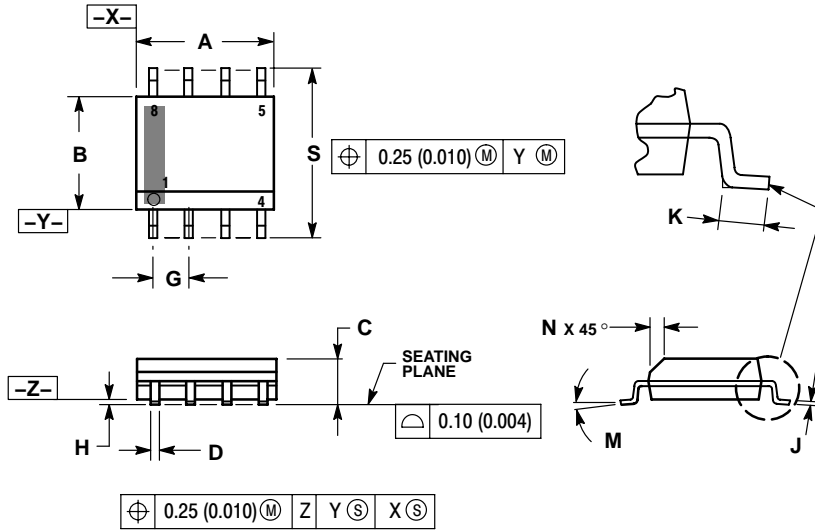


Figure 15. Diode Reverse Recovery Waveform

# MMDF2N02E

## PACKAGE DIMENSIONS

SOIC-8  
CASE 751-07  
ISSUE AG



### NOTES:

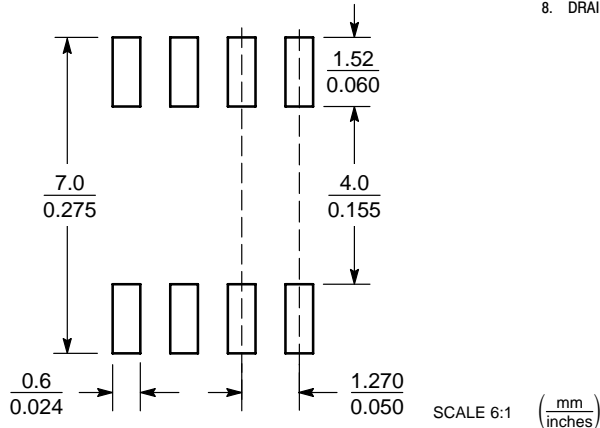
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### STYLE 11:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MiniMOS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.