

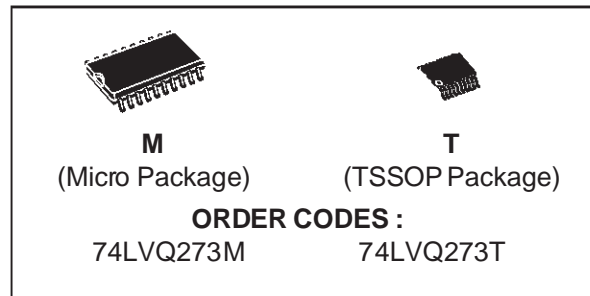


## OCTAL D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:  
 $f_{MAX} = 150 \text{ MHz (TYP.) at } V_{CC} = 3.3\text{V}$
- COMPATIBLE WITH TTL OUTPUT
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C}$
- LOW NOISE:  
 $V_{OLP} = 0.4 \text{ V (TYP.) at } V_{CC} = 3.3\text{V}$
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 12 \text{ mA (MIN)}$
- PCI BUS LEVELS GUARANTEED AT 24mA
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \equiv t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 2\text{V to } 3.6\text{V (1.2V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 273
- IMPROVED LATCH-UP IMMUNITY

### DESCRIPTION

The LVQ273 is a low voltage CMOS OCTAL D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and low noise 3.3V applications.



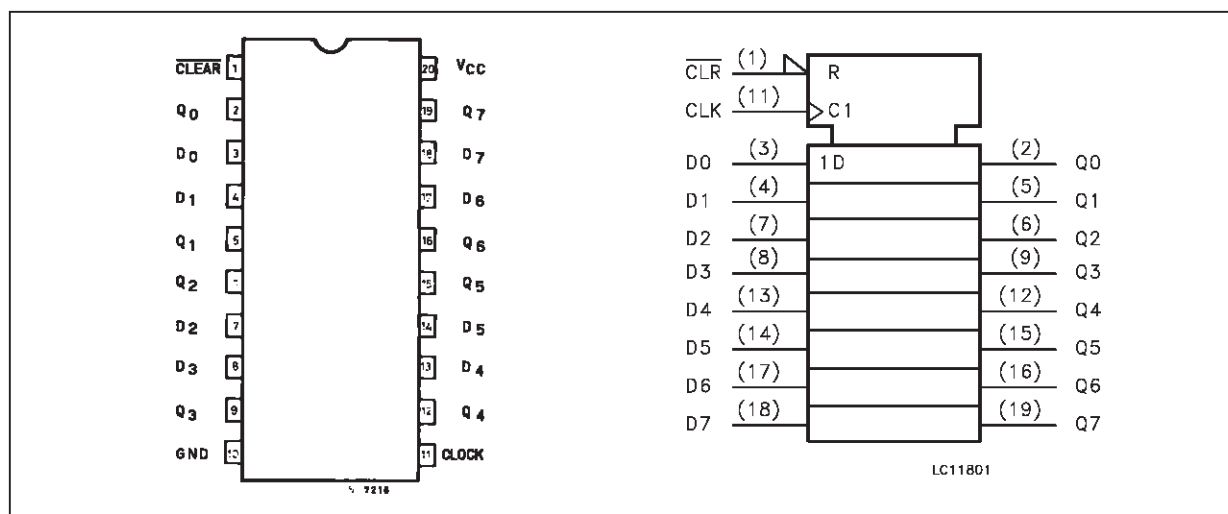
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the CLEAR inputs is held low, the Q outputs are held low independently of the other inputs .

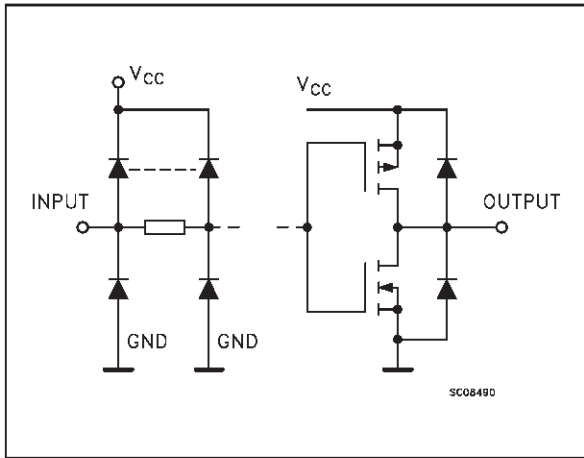
It has better speed performance at 3.3V than 5V LS-TTL family combined with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

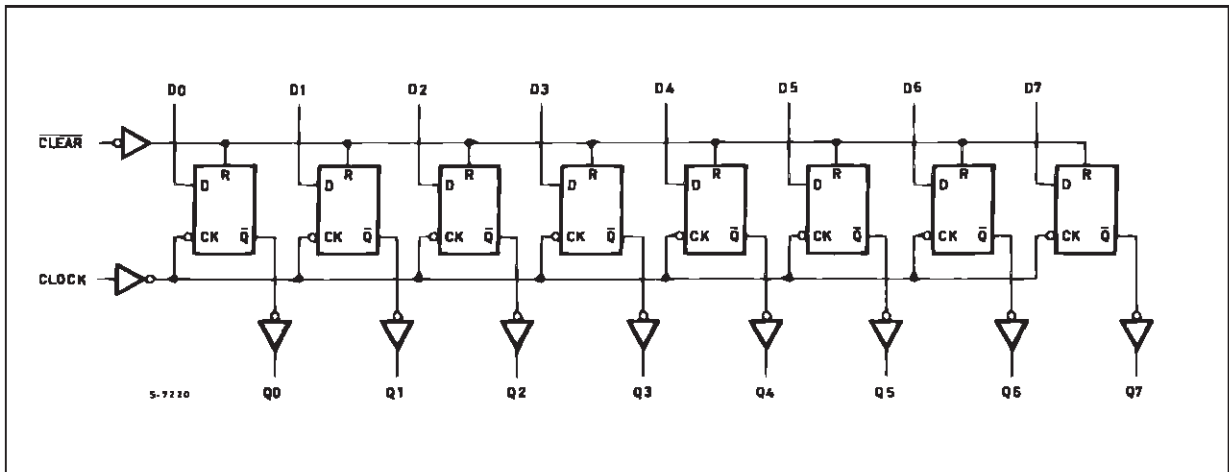
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Master Reset (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	Flip-Flop Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CLOCK	Clock Input (LOW-to-HIGH, Edge-Triggered)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

$\overline{\text{CLEAR}}$	INPUTS		OUTPUTS	FUNCTION
	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q <sub>n</sub>	NO CHANGE

X: Don't Care

LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (note 1)	2 to 3.6	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature:	-40 to +85	°C
dt/dv	Input Rise and Fall Time ( $V_{CC} = 3V$ ) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2)  $V_{IN}$  from 0.8V to 2V

## DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit		
				V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			-40 to 85 °C			
					Min.	Typ.	Max.	Min.		Max.	
V <sub>IH</sub>	High Level Input Voltage	3.0 to 3.6		2.0			2.0		V		
V <sub>IL</sub>	Low Level Input Voltage					0.8		0.8		V	
V <sub>OH</sub>	High Level Output Voltage	3.0	V <sub>I</sub> <sup>(*)</sup> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> =-50 μA	2.9	2.99		2.9		V	
				I <sub>O</sub> =-12 mA	2.58			2.48			
				I <sub>O</sub> =-24 mA				2.2			
V <sub>OL</sub>	Low Level Output Voltage	3.0	V <sub>I</sub> <sup>(*)</sup> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> =50 μA		0.002	0.1		0.1	V	
				I <sub>O</sub> =12 mA		0	0.36		0.44		
				I <sub>O</sub> =24 mA					0.55		
I <sub>I</sub>	Input Leakage Current	3.6	V <sub>I</sub> = V <sub>CC</sub> or GND				±0.1		±1	μA	
I <sub>CC</sub>	Quiescent Supply Current	3.6	V <sub>I</sub> = V <sub>CC</sub> or GND				4		40	μA	
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	3.6	V <sub>OLD</sub> = 0.8 V max						36		mA
I <sub>OHD</sub>				V <sub>OHD</sub> = 2 V min					-25		

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(\*) All outputs loaded.

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit	
				V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C <sub>L</sub> = 50 pF		0.4	0.8			V	
V <sub>OLV</sub>				-0.8	-0.5					
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	3.3				2				
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	3.3		0.8						

1) Worst case package

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND

3) max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). f=1MHz

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50$  pF,  $R_L = 500$   $\Omega$ , Input  $t_r = t_f = 3$  ns)

Symbol	Parameter	Test Condition		Value					Unit	
				V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CK to Q	2.7 3.3 <sup>(*)</sup>			7.5 6.0	17.0 12.0		20.0 14.0	ns	
t <sub>PHL</sub>	Propagation Delay Time CLR to Q	2.7 3.3 <sup>(*)</sup>			10.0 9.0	18.0 13.0		20.0 14.0	ns	
t <sub>w(L)</sub>	CLR pulse Width, LOW	2.7 3.3 <sup>(*)</sup>			2.5 2.0	7.0 5.5		8.5 6.0	ns	
t <sub>w</sub>	CK pulse Width	2.7 3.3 <sup>(*)</sup>			2.0 1.5	7.0 5.5		8.5 6.0	ns	
t <sub>sL</sub> t <sub>sH</sub>	Setup Time D to CK HIGH or LOW	2.7 3.3 <sup>(*)</sup>			-0.4 -0.3	6.5 5.0		8.5 6.0	ns	
t <sub>hL</sub> t <sub>hH</sub>	Hold Time D to CK HIGH or LOW	2.7 3.3 <sup>(*)</sup>			0.4 0.3	3.0 2.0		3.5 2.5	ns	
t <sub>REM</sub>	Recovery Time CLR to CK	2.7 3.3 <sup>(*)</sup>			-0.1 0.0	5.0 4.0		6.5 4.5	ns	
f <sub>MAX</sub>	Maximum Clock Frequency	2.7 3.3 <sup>(*)</sup>		60 90	150 190		50 70		MHz	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew Time (note 1, 2)	2.7 3.3 <sup>(*)</sup>			0.5 0.5	1.0 1.0		1.5 1.5	ns	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ( $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ )

2) Parameter guaranteed by design

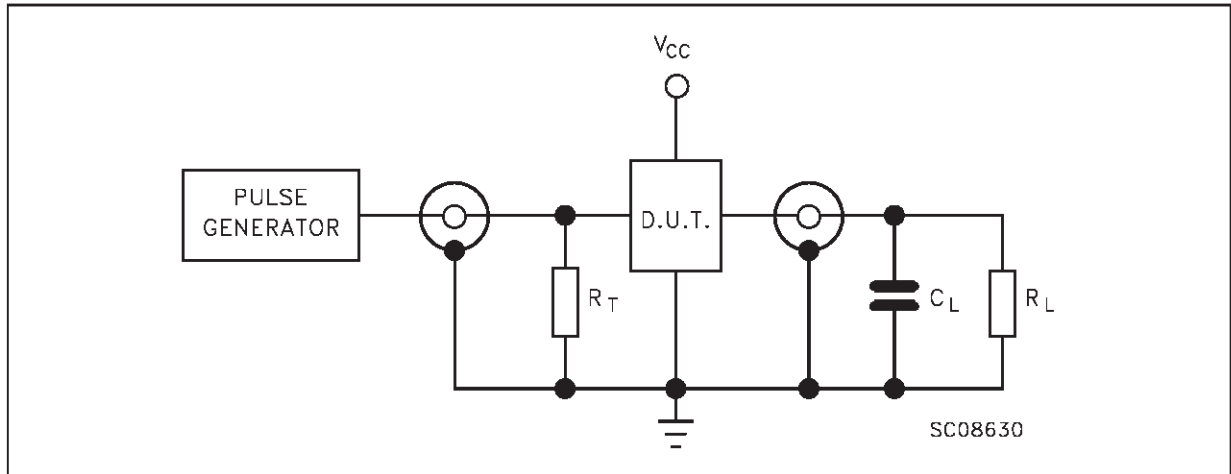
(\*) Voltage range is 3.3V  $\pm$  0.3V

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions		Value					Unit	
				V <sub>CC</sub> (V)	T <sub>A</sub> = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	3.3			5				pF	
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	3.3	f <sub>IN</sub> = 10 MHz		30				pF	

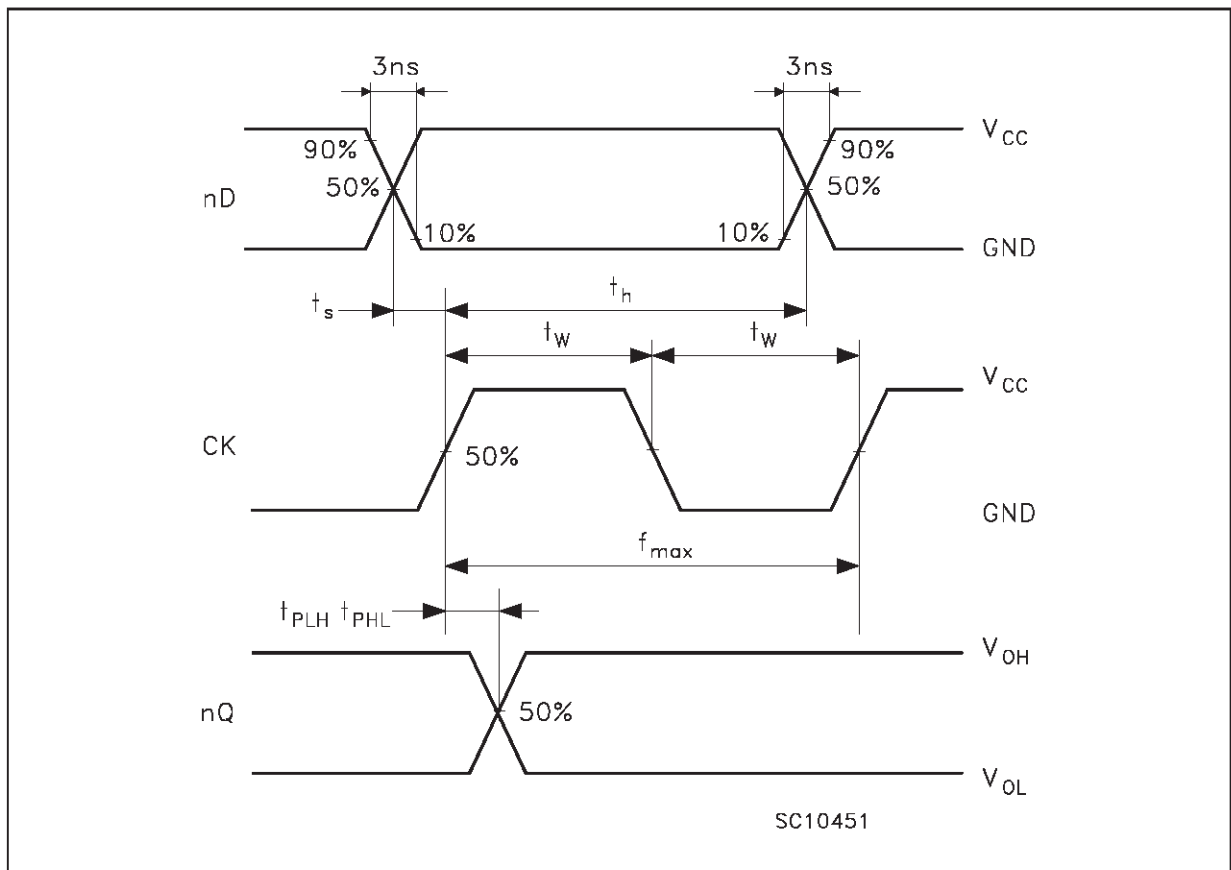
1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$  (per FlipFlop)

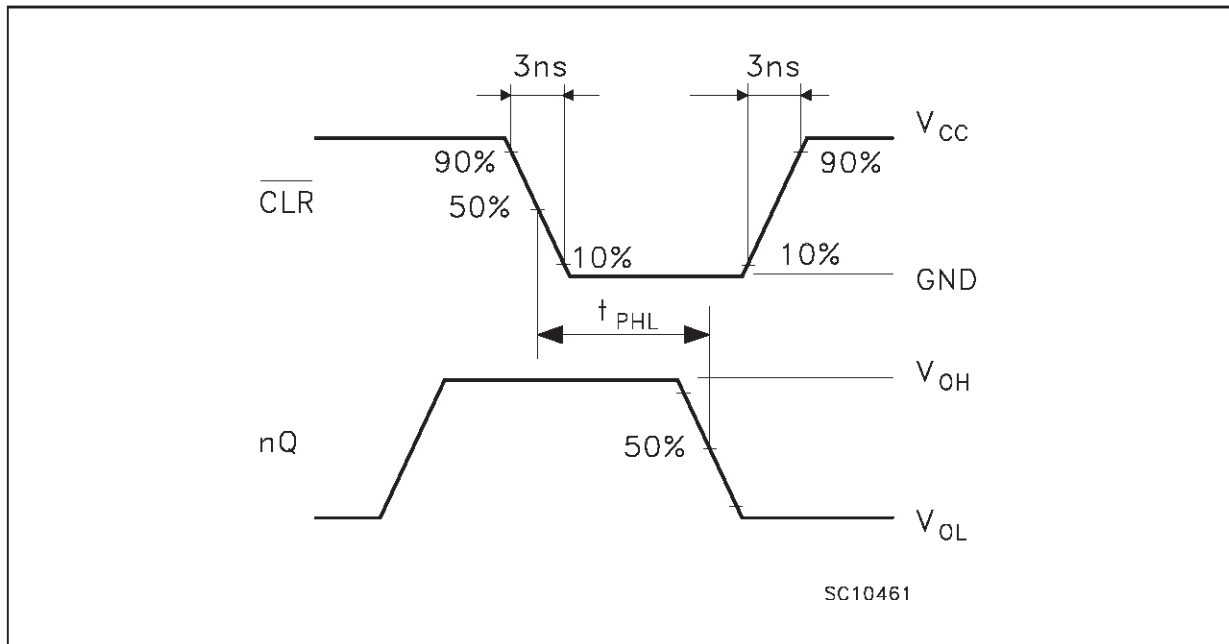
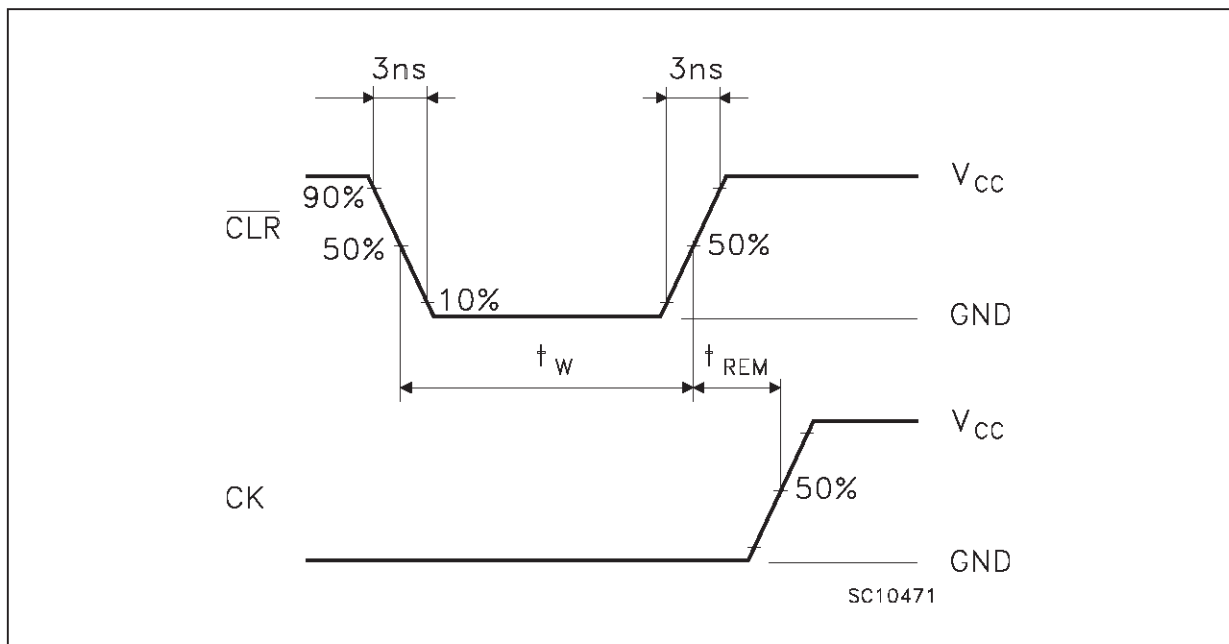
TEST CIRCUIT



$C_L = 50 \text{ pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = R_T = 500\Omega$  or equivalent  
 $R_T = Z_{out}$  of pulse generator (typically  $50\Omega$ )

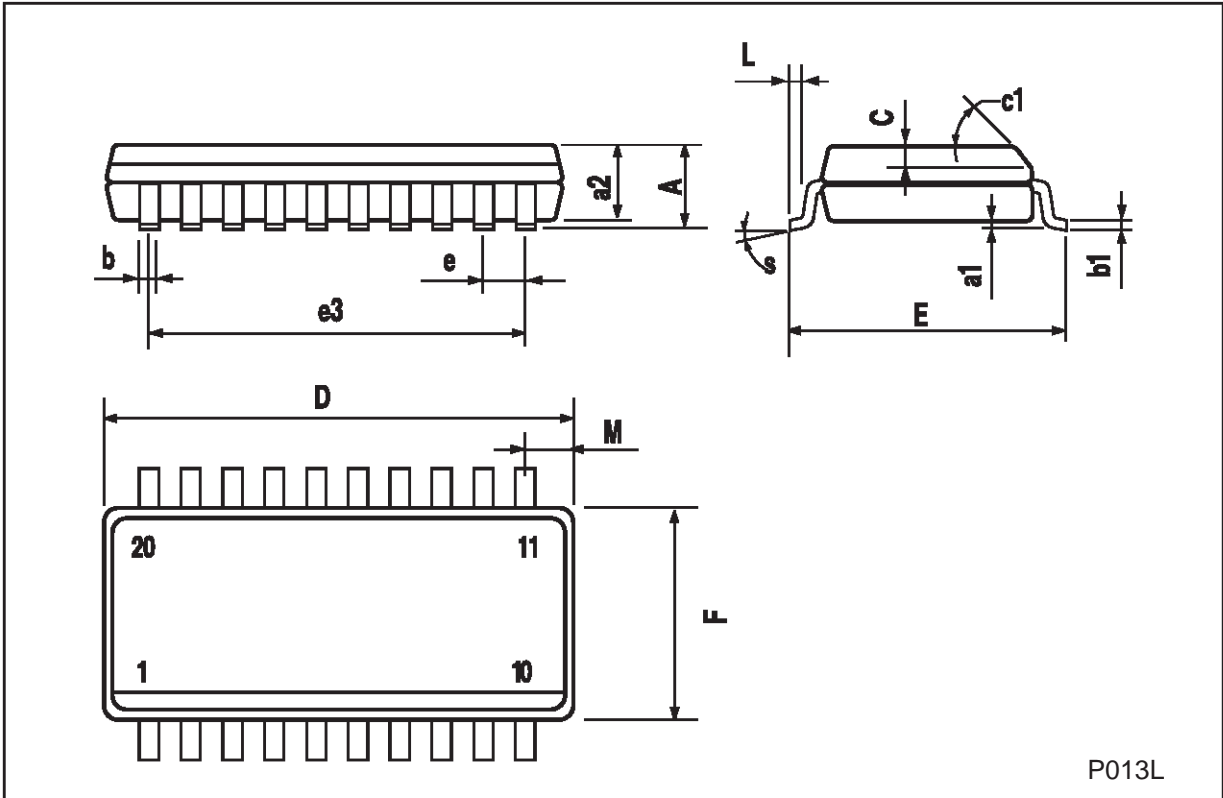
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES, CLOCK PULSE WIDTH  
 ( $f=1\text{MHz}$ ; 50% duty cycle)



**WAVEFORM 2: PROPAGATION DELAYS** (f=1MHz; 50% duty cycle)**WAVEFORM 3: RECOVERY TIME, CLEAR PULSE WIDTH** (f=1MHz; 50% duty cycle)

**SO-20 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					

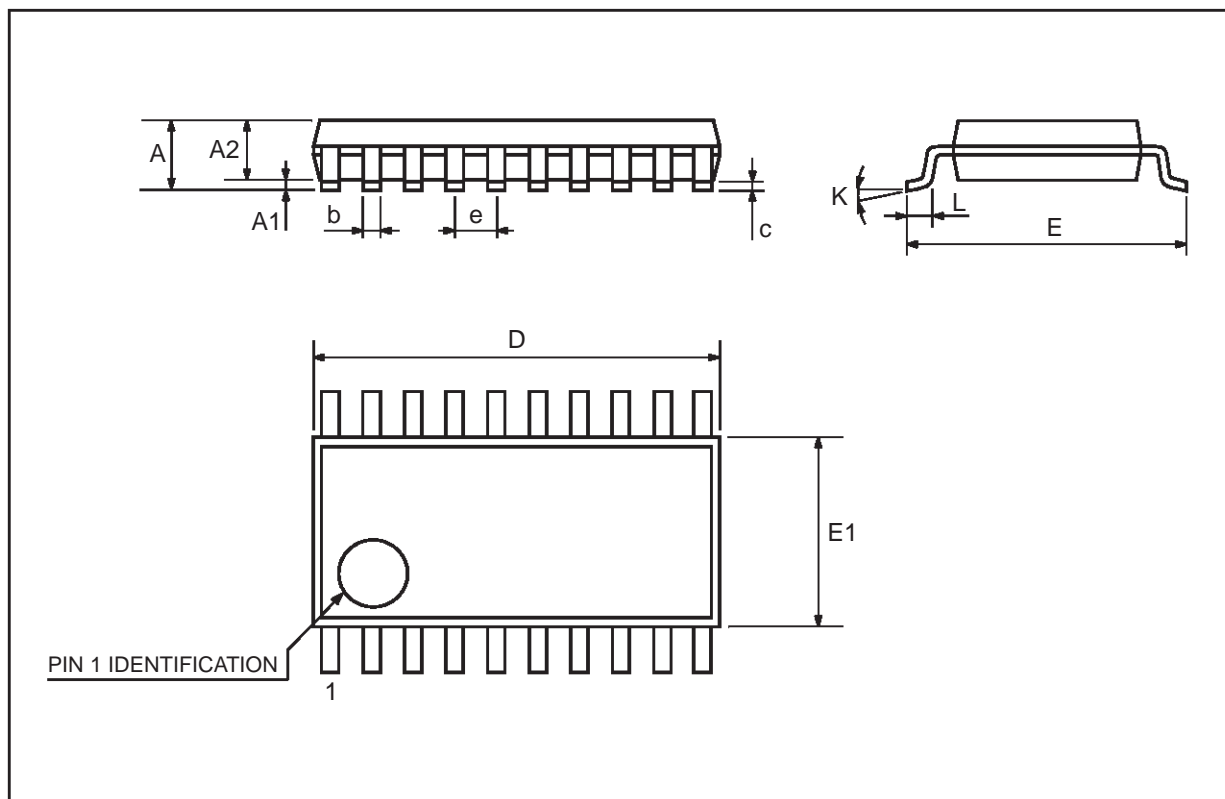


P013L



## TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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