TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC4511AP, TC74HC4511AF

BCD-to-7 Segment Latch/Decoder/Driver

The TC74HC4511A is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The segment output driver, which is of CMOS construction, has a large I_{OH} capability which permits the device to drive cathode common LED directly.

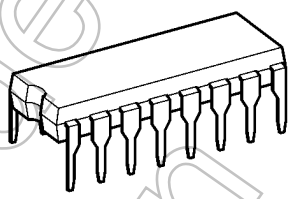
When lamp test (LT) is held low, all segment outputs will go high, and when the blanking input (BI) is held low and LT is held high, all segment outputs will go low. These functions are independent of other inputs and used to test the display.

BI is used to pulse - modulate the brightness of the display.

When error code (over 10) is applied to BCD inputs, all segment outputs will go to low (turn off).

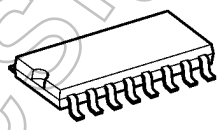
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC4511AP



DIP16-P-300-2.54A

TC74HC4511AF



SOP16-P-300-1.27A

Weight

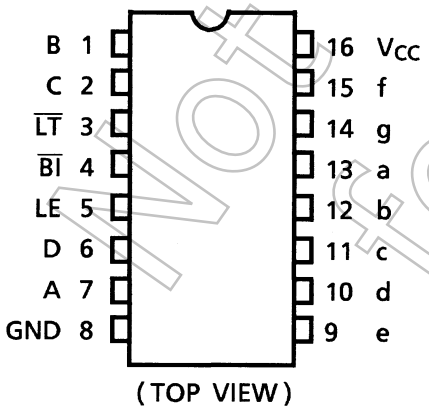
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

Features

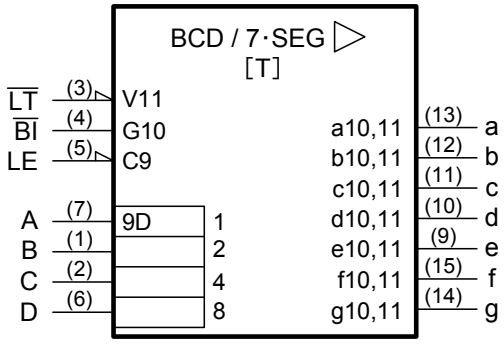
- High speed: t_{pd} = 28 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}|$ = 20 mA
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with TC4511B

Pin Assignment



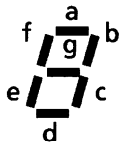
Start of commercial production
1988-05

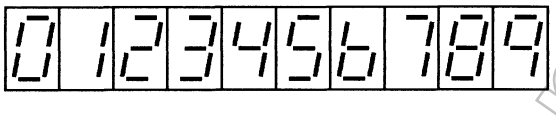
IEC Logic Symbol



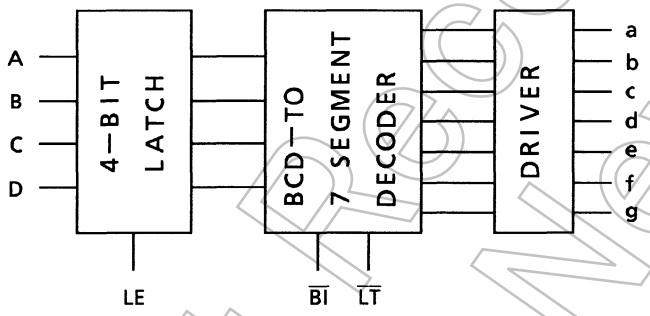
[T]: Truth Table

Display Mode





Block Diagram

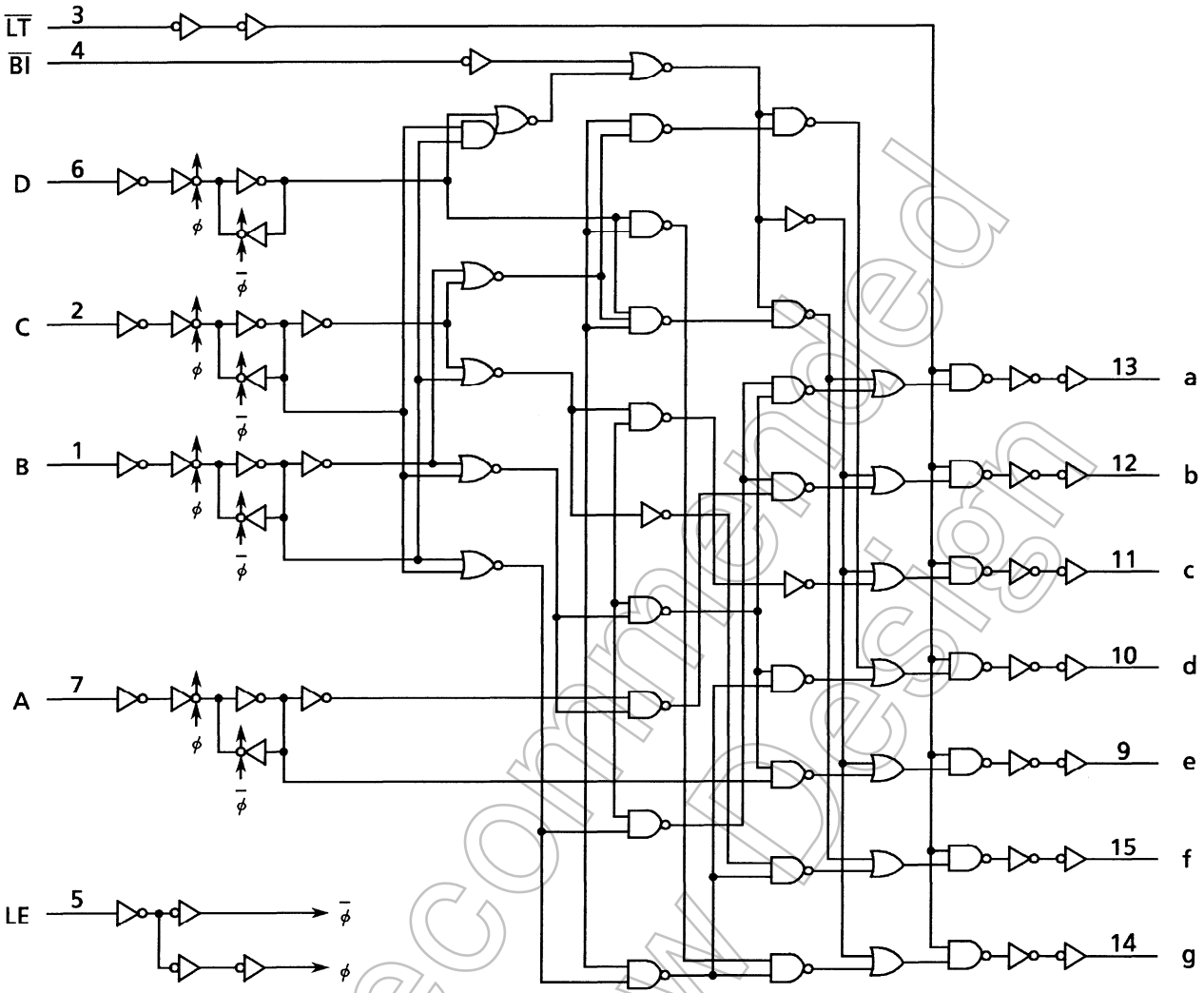


Truth Table

Inputs							Outputs							Display Mode
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
*	*	L	*	*	*	*	H	H	H	H	H	H	H	8
*	L	H	*	*	*	*	L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	*	L	L	L	L	L	L	L	Blank
L	H	H	H	H	*	*	L	L	L	L	L	L	L	Blank
H	H	H	*	*	*	*	Hold the stage at the leading edge of LE							

*: Don't care

Logic Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	+25 (sinc)/−35 (source)	mA
DC V_{CC}/ground current	I_{CC}	+150 (I_{CC})/−50 (I_{GND})	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	—	2.0	1.50	—	—	1.50	—	V
			4.5	3.15	—	—	3.15	—	
			6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—	2.0	—	—	0.50	—	0.50	V
			4.5	—	—	1.35	—	1.35	
			6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	2.0	1.9	2.0	—	1.9	—	V
		I_{OH} = −20 μA	4.5	4.4	4.5	—	4.4	—	
			6.0	5.9	6.0	—	5.9	—	
		I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	
		I_{OH} = −20 mA	4.5	3.20	3.80	—	2.90	—	
		I_{OH} = −7.8 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	2.0	—	0.0	0.1	—	0.1	V
		I_{OL} = 20 μA	4.5	—	0.0	0.1	—	0.1	
			6.0	—	0.0	0.1	—	0.1	
		I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
		I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND	6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND	6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (LE)	$t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t_s	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH}	—	—	4	8	ns
Output transition time	t_{THL}	—	—	4	8	ns
Propagation delay time (BCD-segment)	t_{pLH} t_{pHL}	—	—	28	45	ns
Propagation delay time ($\overline{BI}$ -segment)	t_{pLH} t_{pHL}	—	—	18	31	ns
Propagation delay time ($\overline{LT}$ -segment)	t_{pLH} t_{pHL}	—	—	12	21	ns
Propagation delay time (LE-segment)	t_{pLH} t_{pHL}	—	—	26	44	ns

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = −40 to 85°C		Unit
		V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time low to high	t_{TLH}	2.0	—	25	60	—	75	ns
		4.5	—	7	12	—	15	
		6.0	—	6	11	—	13	
Output transition time high to low	t_{THL}	2.0	—	30	75	—	95	ns
		4.5	—	8	15	—	19	
		6.0	—	7	13	—	16	
Propagation delay time (BCD-segment)	t_{pLH} t_{pHL}	2.0	—	125	255	—	320	ns
		4.5	—	33	51	—	64	
		6.0	—	23	43	—	54	
Propagation delay time ($\overline{BI}$ -segment)	t_{pLH} t_{pHL}	2.0	—	70	175	—	220	ns
		4.5	—	22	35	—	44	
		6.0	—	17	30	—	37	
Propagation delay time ($\overline{LT}$ -segment)	t_{pLH} t_{pHL}	2.0	—	60	120	—	150	ns
		4.5	—	15	24	—	30	
		6.0	—	12	20	—	26	
Propagation delay time (LE-segment)	t_{pLH} t_{pHL}	2.0	—	95	240	—	300	ns
		4.5	—	32	48	—	60	
		6.0	—	23	41	—	51	
Input capacitance	C_{IN}	—	—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—	—	95	—	—	—	pF

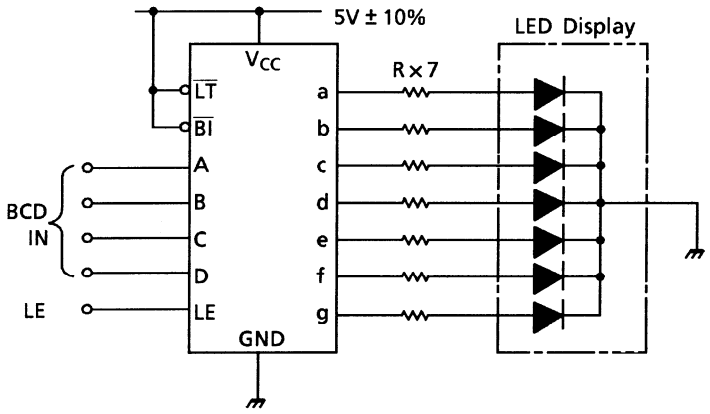
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Application Circuit

Static Display Circuit

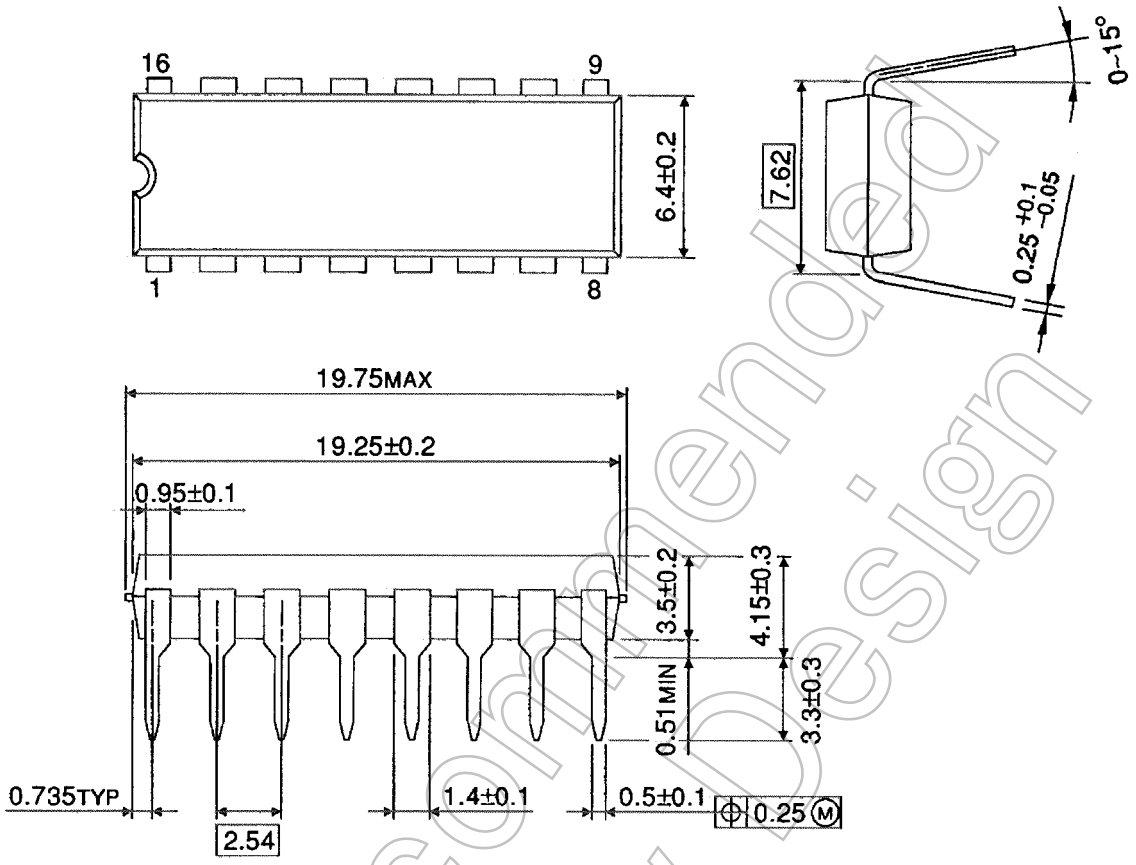


Recommended Resistance R

Display	Color	Letter Hight	R
TLR358T	Red	13.4 mm	390 Ω
TLR362T	Red	14.2	390 Ω
TLR332T	Red	7.6	390 Ω
TLR342T	Red	10.9	390 Ω
TLG358T	Green	13.4 mm	160 Ω
TLG362T	Green	14.2	160 Ω
TLG332T	Green	7.6	160 Ω
TLG342T	Green	10.9	160 Ω

Package Dimensions

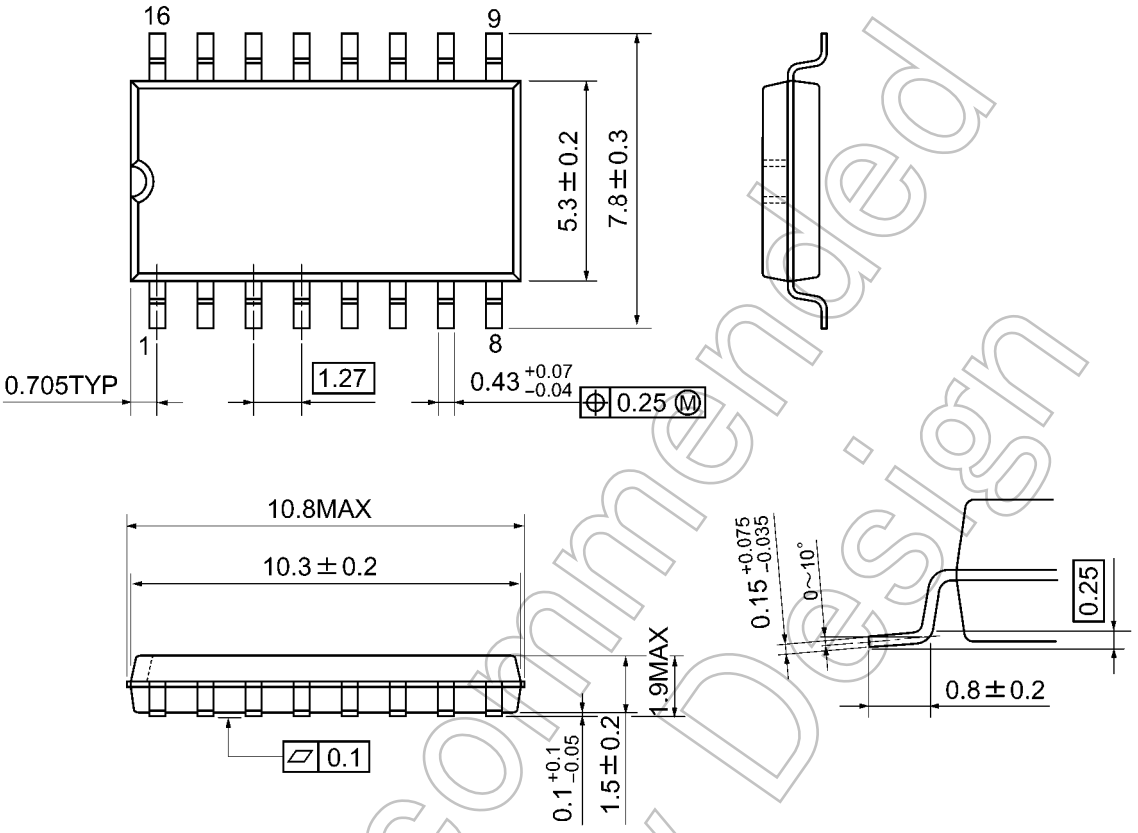
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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