Dynax

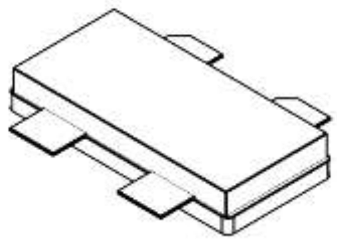
Preliminary Datasheet
V2, Nov. 2019

DXG1CH27A-140EF

RF POWER GaN Transistor for Wireless Infrastructure

2515 – 2675 MHz, 140 W,
RF POWER GaN Transistor

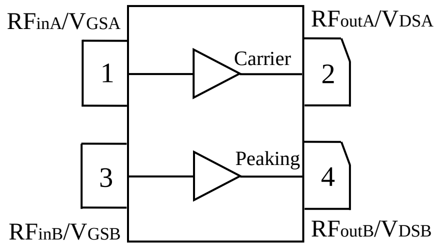
DXG1CH27A-140EF is a 140 W RF GaN HEMT Transistor with first generation RF GaN technology from Dynax, which is ideal for 2515 MHz to 2675 MHz cellular base station applications. It features input matching, wide instantaneous bandwidth and a thermally-enhanced package.



Package Type: 780P2GB

Features

- High Efficiency, High Gain
- Internally Matched for Broadband Performance
- Designed for Digital Pre-Distortion Error Correction Systems
- Optimized for Doherty Applications



(Top View)

Figure 1. Pin Connection

Typical RF Performance [1]

- Frequency: 2515 – 2675 MHz
- Peak Output Power: 140 W
- Linear Efficiency: > 51 %
- Linear Gain: > 13 dB
- ACPR: < - 28 dBc

Note:

[1] Typical Doherty Performance in Dynax DXG1CH27A-140EF Doherty Demo with the device soldered to the heatsink, test condition: V_{DD} = 48 V, I_{DQA} = 100 mA, V_{GSB} = -3.5 V, Pout = 14 W Avg., 1-Carrier W-CDMA, Input Signal PAR = 7.5 dB @ 0.01 % Probability on CCDF.

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Table 1. Maximum Ratings

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	-10 ~ +2	V
Maximum Forward Gate Current	I_{GMAX}	13.6	mA
Storage Temperature Range	T_{STG}	-65 ~ +150	℃
Operating Junction Temperature	T_J	225	℃
Absolute Maximum Channel Temperature [2]	T_{MAX}	275	℃

[2] Functional operation above 225℃ has not been characterized and is not implied.Operation at T_{MAX} (275℃) reduces median time to failure by an order of magnitude; operation beyond T_{MAX} could cause permanent damage.

Table 2. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case Case Temperature 85℃, P_D = 13.5 W	$R_{thjc(IR)}$	2.1	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case Case Temperature 85℃, P_D = 13.5 W	$R_{thjc(FEA)}$	2.8	℃/W

Table 3. Ruggedness Characteristics

VSWR 10:1 at V_{DD} = 48 V, 140 W Pulsed CW Output Power, Pulse Width = 100 us, Duty = 10%	No Device Damage

Table 4. Ordering Information

Device	Package Number	Marking
DXG1CH27A-140EF	780P2GB	DXG1CH27A-140EF

Table 5. Bias Sequences

Bias-up Sequence	Bias-down Sequence
Set V_{GS} to -5 V	Turn off RF power
Turn on V_{DS} to 48 V	Reduce V_{DS} down to 0 V
Increase V_{GS} until I_{DS} current is attained	Turn off V_{GS}
Apply RF input power	

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Table 6. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
DC Characteristics (measured on wafer prior to packaging)					
Side A, Carrier					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	5.0	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 5.0 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 5.0 mA)	$V_{GS(th)}$	-4.0	-2.1	-1.0	V
Gate Quiescent Voltage (V_{DD} = 48 V, I_D = 125 mA)	$V_{GS(Q)}$	-	-1.7	-	V
Side B, Peaking					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	8.6	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 8.6 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 8.6 mA)	$V_{GS(th)}$	-4.0	-2.1	-1.0	V
Gate Quiescent Voltage (V_{DD} = 48 V, I_D = 200 mA)	$V_{GS(Q)}$	-	-1.7	-	V
RF Characteristics					
Typical Doherty Performance [3]					
Power Gain	G_p	-	13	-	dB
Drain Efficiency	η_D	-	51	-	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	-	7.5	-	dB
Adjacent Channel Power Ratio	ACPR	-	-28	-	dBc

[3] Typical Doherty Performance in Dynax DXG1CH27A-140EF Doherty Demo with the device soldered to the heatsink, test condition: V_{DD} = 48 V, I_{DQA} = 100 mA, V_{GSB} = -3.5 V, Pout = 14 W Avg., f = 2515 - 2675 MHz, 1-Carrier W-CDMA, IQ Magnitude Clipping, input signal PAR = 7.5 dB @ 0.01 % Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

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Typical RF Performance in Load Pull System

Table 7. Side A, Carrier Load Pull Performance

V_{DD} = 48 V, I_{DQA} = 125 mA, Pulsed CW, Pulse Width = 100 us, Duty Cycle = 10 %

Maximum Output Power						
Freq (MHz)	**Zsource (Ω)**	**Zload (Ω)**	**Gain (dB)**	**Psat (dBm)**	**Psat (W)**	**η_D (%)**
2500	4.0 - j16.7	11.6 - j0.4	18.2	47.7	57	69.7
2600	4.0 - j16.4	11.1 - j0.6	18.3	47.5	56	69.3
2700	3.6 - j15.5	11.8 - j0.6	18.3	47.4	55	68.0
Maximum Drain Efficiency						
Freq (MHz)	**Zsource (Ω)**	**Zload (Ω)**	**Gain (dB)**	**Psat (dBm)**	**Psat (W)**	**η_D (%)**
2500	4.0 - j16.7	4.7 + j3.1	20.2	46.1	41	79.6
2600	4.0 - j16.4	4.6 + j2.7	20.4	46.0	40	80.9
2700	3.6 - j15.5	4.1 + j2.3	20.8	45.7	37	79.7

Table 8. Side B, Peaking Load Pull Performance

V_{DD} = 48 V, I_{DQB} = 200 mA, Pulsed CW, Pulse Width = 100 us, Duty Cycle = 10 %

Maximum Output Power						
Freq (MHz)	**Zsource (Ω)**	**Zload (Ω)**	**Gain (dB)**	**Psat (dBm)**	**Psat (W)**	**η_D (%)**
2500	6.3 - j20.0	7.2 - j3.0	19.1	50.1	102	67.1
2600	9.6 - j23.5	6.5 - j3.0	19.6	50.0	100	70.9
2700	11.3 - j23.0	6.0 - j3.6	19.7	50.0	100	70.9
Maximum Drain Efficiency						
Freq (MHz)	**Zsource (Ω)**	**Zload (Ω)**	**Gain (dB)**	**Psat (dBm)**	**Psat (W)**	**η_D (%)**
2500	6.3 - j20.0	3.8 + j0.7	21.3	48.4	69	79.4
2600	9.6 - j23.5	3.8 + j0.3	21.7	48.2	66	78.6
2700	11.3 - j23.0	3.2 - j0.8	21.7	48.2	66	78.7

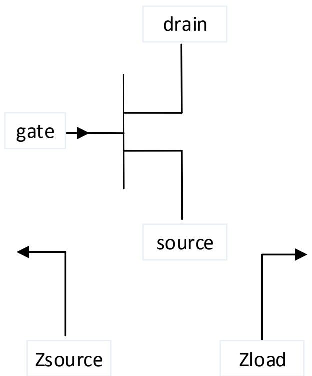

Figure 2. Definition of Transistor Impedance

Zsource: Measured impedance presented to the input of the device at the package plane
Zload: Measured impedance presented to the output of the device at the package plane

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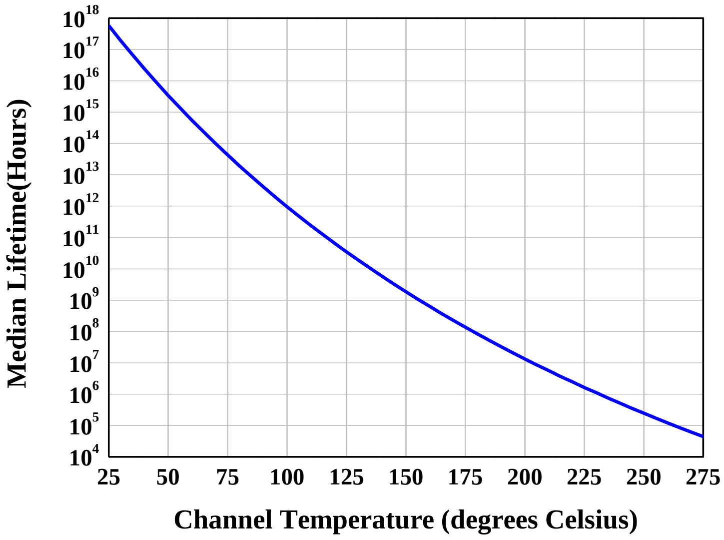

Figure 3. Median Lifetime vs. Channel Temperature

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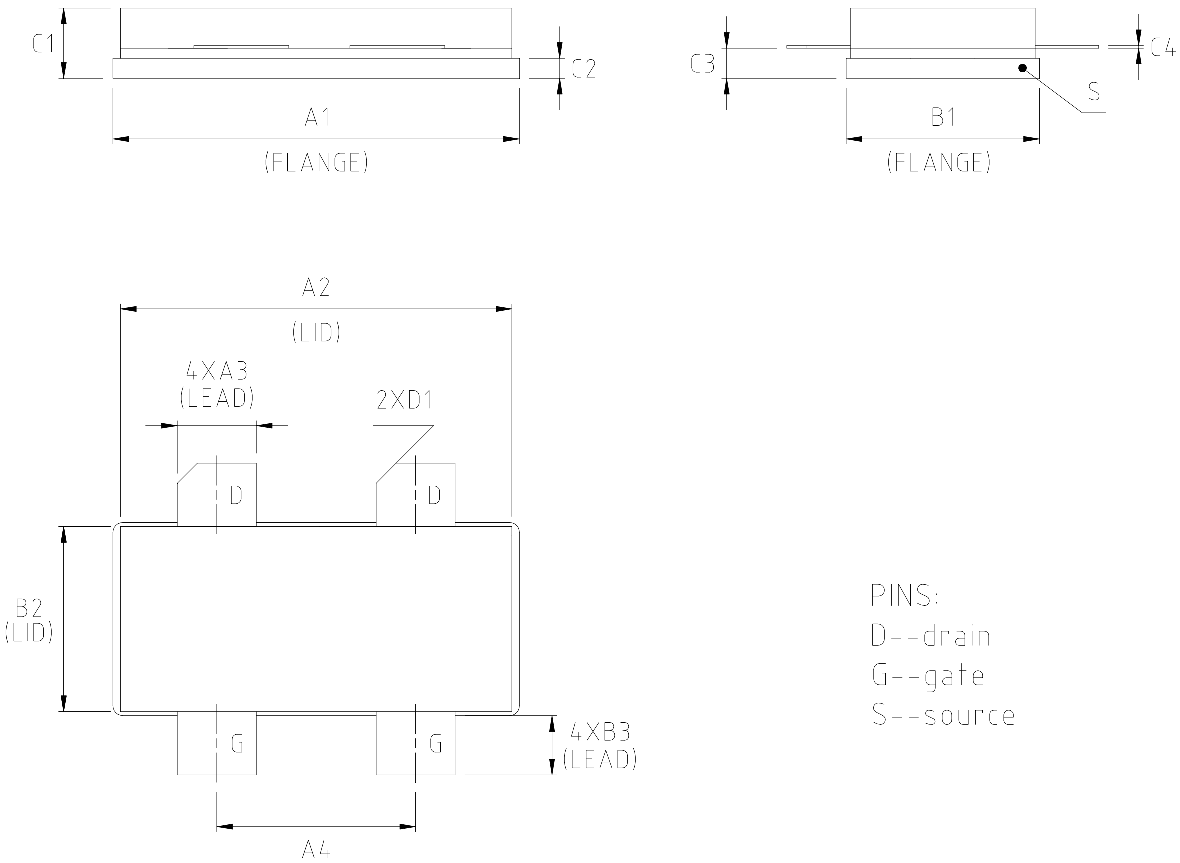
Package Dimensions

Package Type: 780P2GB



PINS:
D--drain
G--gate
S--source

DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX
A1	0.805	0.815	20.45	20.70
A2	0.772	0.788	19.61	20.02
A3	0.153	0.162	3.87	4.13
A4	0.385	0.395	9.77	10.03
B1	0.380	0.390	9.65	9.91
B2	0.365	0.375	9.27	9.53
B3	0.108	0.128	2.75	3.25
C1	0.130	0.170	3.30	4.32
C2	0.035	0.045	0.89	1.14
C3	0.057	0.067	1.45	1.70
C4	0.003	0.006	0.08	0.15
D1	0.040 45° REF		1.02 45° REF	

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Product Documentation and Software

Refer to the following resources to aid your design process.

Application Notes

- AN_04: Referential design of bias circuits of GaN HEMT transistor

Document Revision History

The following table summarizes revisions to this document.

Revision	Date	Status	Description
V1	20190726	Preliminary datasheet	Initial version.
V2	20191120	Preliminary datasheet	Update performance data.

Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	Electro-Static Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing-Wave Ratio

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Contact Information

For sales or technical support:

Home Page: www.dynax-semi.com

Tel: +86-512-36886888

Email: sales@dynax-semi.com

Zip Code: 215300

Company Address: No.18 Chenfeng Road, Kunshan, Jiangsu Province, China

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