IN-PLUG® series: IPS201

Push-Pull Controller
Voltage-Mode or Current Mode

DESCRIPTION

The IN-PLUG® IPS201 Integrated Circuit is a low-voltage PWM controller that contains all the features needed to implement Push-Pull, Half-Bridge, and Full-Bridge topologies. It is used in switch mode power supplies to provide pulse width modulation to a pair of high voltage/high current MOSFETs.

It includes an oscillator, error amplifier, current sensing, and a regulated voltage reference output.

It is presented in voltage mode or current mode versions. Both the frequency and the dead time are set by the user by choosing the appropriate external RC components.

FEATURES

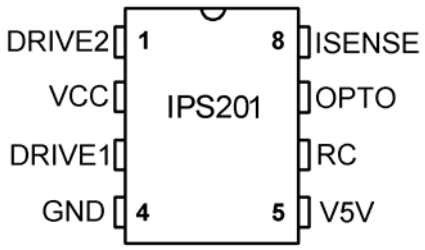
- Dual output drivers (200mA rating)
- Oscillator set by an R and C
- Adjustable dead time
- Adjustable switching frequency
- 5V reference
- Optoisolator/feedback input
- Shunt regulator for VCC input
- Overtemperature shutdown
- Voltage Mode (IPS201A) or Current Mode (IPS201B)
- Commercial (0°C to +70°C) or Industrial (-40°C to +85°C) Temperature Range
- Targetted topologies:
  Center-Tap – Half H-Bridge – Full H-Bridge

APPLICATIONS

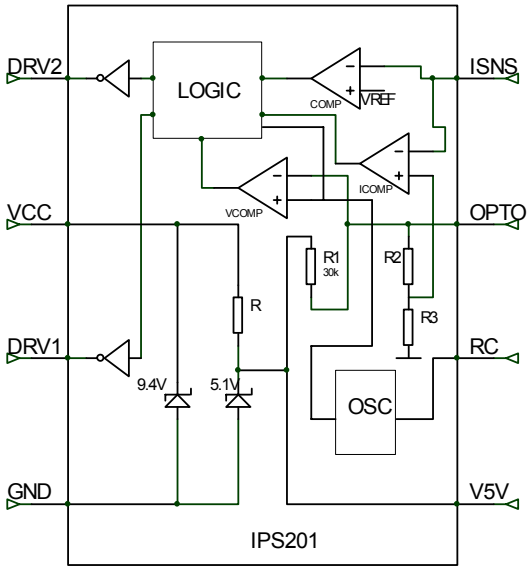
- AC/DC power supplies
- DC/DC power supplies
- Fluorescent lamp driver
- Distributed power systems
- Inverters

REVISION 4

PIN CONFIGURATION: DIP-8 / SOIC-8



FUNCTIONAL BLOCK DIAGRAM



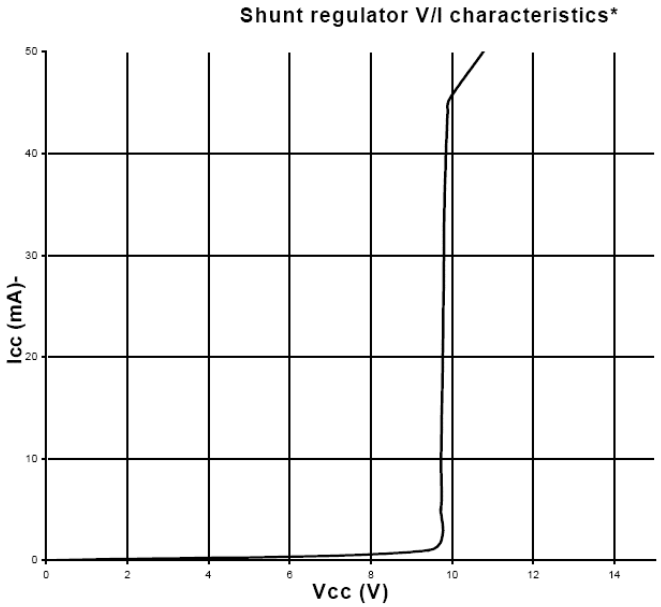
ORDERING INFORMATION

For detailed ordering information, refer to the second-to-last page of this document.

PIN DESCRIPTION

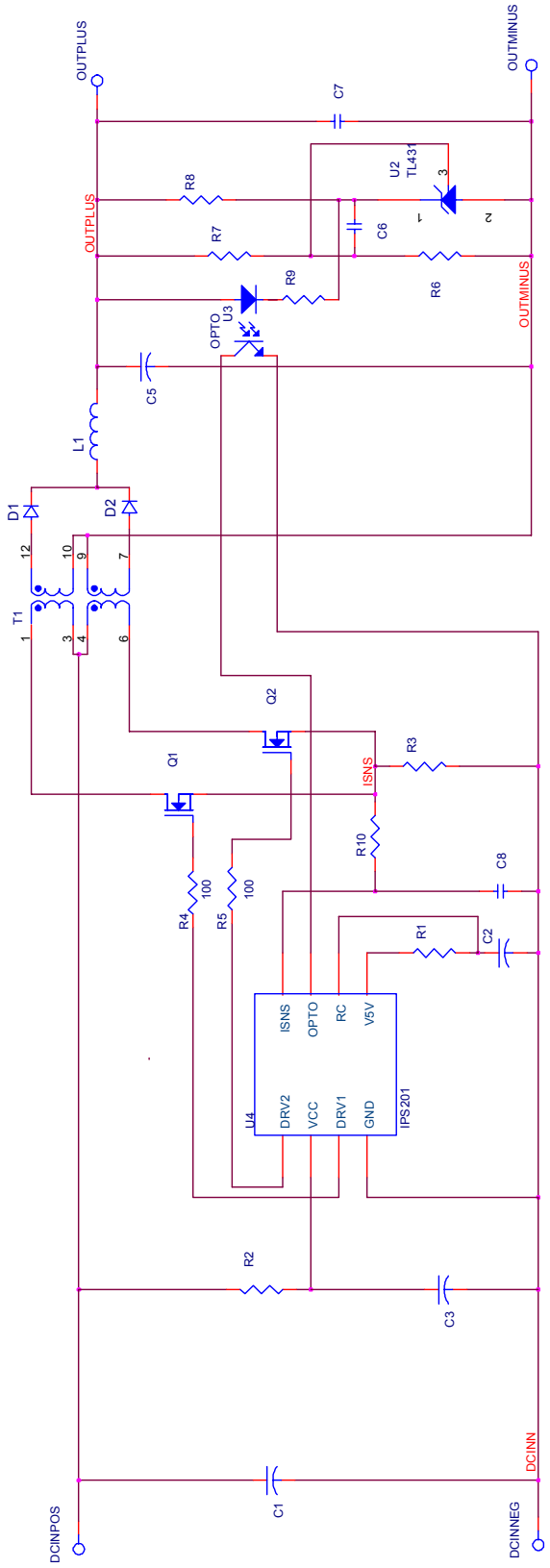
PIN	Description
1- DRV2	Second FET gate drive
2- VCC	Power/current input
3- DRV1	First FET gate drive
4- GND	Lowest chip voltage, voltage reference
5- V5V	Reference voltage output
6- RC	Resistor/capacitor connection for oscillator
7- OPTO	Feedback input
8- ISNS	Current sense resistor input

SHUNT REGULATOR V-I CURVE



*** Note: Do not attempt to force more than 1mA into Vcc pin during start-up.**

TYPICAL PUSH-PULL APPLICATION



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING		
Characteristics	**Value**	**UNITS**
IPS 201 Max I_{CC} (shunt regulator)	**50**	**mA**
Peak DRV1 and DRV2 current (sink or source)	**200**	**mA**
Operating junction temperature	**- 40 to 150**	**°C**
Storage temperature range	**- 55 to 150**	
Lead temperature (3 mm from case for 5 sec.)	**260**	

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
Supply, Bias		**MIN.**	**TYP.**	**MAX.**	
Shunt regulator voltage	**ICC = 1 to 30 mA**	**9.2**	**9.4**	**9.7**	**V**
Shunt regulator dynamic resistance	**1 to 30 mA**	**2**	**3**	**5**	**Ω**
Shunt regulator max peak repetitive current		**-**	**35**	**-**	**mA**
Min I_{CC} to ensure operation (internal current)		**-**	**-**	**200**	μA
Other pins					
ISNS threshold (note 2)		**-**	**700**		**mV**
Output impedance of OPTO		**-**	**30**	**-**	**KΩ**
V5V voltage	**1mA load**	**-**	**5.1**	**-**	**V**
Max OPTO pin current sourcing			**160**	**-**	μA
Thermal shutdown trip temperature		**-**	**140**	**-**	**°C**
Thermal shutdown temperature hysteresis			**5**		**°C**

Note1: Tighter tolerance of V5V available upon request.

Note2: All values are @ 25℃ unless otherwise specified.

Note3: Electrical parameters, although guaranteed, are not all 100% tested in production.

APPLICATION INFORMATION

PIN DESCRIPTIONS

The IPS201 chip is intended to provide feedback control and current limiting on the primary side of switching power supplies.

Powering the chip (Pin 2 – VCC and Pin 4 – GND)

The VCC pin acts like a 9.4 volt zener. The GND pin is the lowest voltage the chip sees. It is recommended as good engineering practice to have a decoupling capacitor from VCC-to-GND of at least 10uF. The intended design implementation for powering the chip is to have a resistor from VCC to either the input voltage and/or a separate supply. This resistor should be sized such that at minimum supply voltage (and subtracting 9.5 volts for the VCC voltage), there is enough current to operate the chip.

The IPS201 is fabricated in a low-voltage IC process. This means that they can be damaged with pin voltages greater than 12 volts. When testing designs using an IPS201, it is typical to perform debug with a laboratory current-limited external power supply attached to the VCC pin. This external supply should be set for around 12 volts and 10 milliamps. It is possible to damage an IPS201 if one of these lab supplies is set for (say) 20 volts and 10 milliamps, the lab supply is powered-on, and then the lab supply is connected to the IPS201, because the VCC voltage will be 20 volts (in this example) until the IPS201 starts conducting current and discharges any output capacitance in the lab supply.

DRV1 (Pin 3), DRV2 (Pin 1)

The drivers for the FETs should have a 100 ohm resistor in series with the gate to limit the transient current and protect those pins from ESD and latch-up effects. The drivers are sized such that no additional components should be needed to get acceptable turn-on/turn-off performance driving FETs rated up to 10 amps. The turn-on current for the FET gates comes through the VCC pin, so the user needs to have sufficient decoupling and source current on the VCC pin to adequately provide this. To drive larger FETs or to operate at high frequencies, a pair of transistors (NPN/PNP) might need to be added to each gate to provide additional gate current drive (see example shown below for more information).

OPTO (Pin 7)

The OPTO pin is a current source. The intended connection for the voltage feedback network is to connect the OPTO pin to the anode of the photodiode in an optoisolator, with the cathode of the photodiode connected to ground. The IPS201 uses very little current to operate, but the user is reminded that the OPTO current being sourced comes through the VCC pin. The pin electrically looks like a 30k ohm resistor pulling up to an internal 5.1 volts. The voltage range for affecting the PWM function should be considered to be zero to 4 volts to go from 0% to near 100% driver on-time ("near" because the dead time must be subtracted out).

V5V (Pin 5)

The V5V provides a regulated 5.1V voltage source for use by the oscillator pin. The total load on this pin should not exceed 1.7 milliamps. A small ceramic capacitor to ground, 1uf/10V suggested, should be connected here for decoupling the internal and external functions using this voltage source.

RC - (Pin 6)

The internal oscillator has its frequency set by an external resistor connected from this pin to the V5V pin, and by an external capacitor from this pin to ground. The waveform at this pin looks like an exponential rise from zero to 5.1 volts followed by a linear fall back down to zero. The fall time sets the dead time when neither driver output is active/high. The operation of this pin is similar to that of the industry standard UC3842 current-mode-PWM chip. The RC-pin rise time (maximum output on-time) is the time it takes for the timing capacitor to charge from 0.5 volts to 4 volts through the timing resistor (which is connected to VCC [5.1 volts]. This time is approximately

Ton = (1.4 * R * C) -0.7e-6

The RC-pin fall time (output dead time) is the time it takes for the timing capacitor to discharge from 4 volts to 0.5 volts through an internal current sink (of 6 milliamps). This time is approximately

Toff = (583*R*C)/(R-458)

The oscillator frequency is the inverse of the sum of these two times,

Freq = 1/(Ton+Toff)

As an example, for a 2k resistor and 3900pF capacitor, Ton = 10.3 microseconds, Toff = 3.0 microseconds, Freq = 75 kiloHertz. Note that this 13.3 microseconds is the time from the rising edge of DRV1 to the rising edge of DRV2. The total cycle time from DRV1 rising to DRV1 rising again will be twice this, or 26.6 microseconds. The user should remember that the charging current comes through the VCC pin to the V5V pin. A lower timing resistor value will increase the charging current, and this will increase the necessary current into VCC. The dead time sets the maximum duty cycle available from the chip. Using the above example, the maximum duty cycle is 10.3usec/13.3usec = 77%.

ISNS – (Pin 8)

The ISNS pin provides a latched over-current function and access to the ISENSE amplifier. In this context, "latched" means that the overcurrent is latched 'on' for the remainder of that cycle of that output phase. The threshold voltage is fixed at 700 millivolts. In current mode operation the operating current threshold is variable, based on the feedback appearing at the OPTO pin. Current mode devices still have the latched overcurrent function, always at 0.700 volts (referring to the Functional Block Diagram: R1 is about 30k, R2 is about 500k, and R3 is about 100k ohms. The variable voltage from the OPTO pin that is divided-down and going to the ICOMP comparator is therefore going to be between about 0.000 and 0.700 volts, providing a PWM current threshold.) Referring again to the Functional Block Diagram: for voltage-mode devices, the PWM control comes from the VCOMP comparator (while for current mode devices the PWM

control comes from the ICOMP comparator). Referring to the Typical Push-Pull Application Schematic: in most applications, it is expected that a small RC filter will need to be put between the current sense resistor and the ISNS pin to reduce false triggerring due to the sensing of the gate-turn on current. When using current mode control, is is manytimes necessary to provide slope compensation. Refer to the example below for more information how this can be done with an added connection to the ISNS pin.

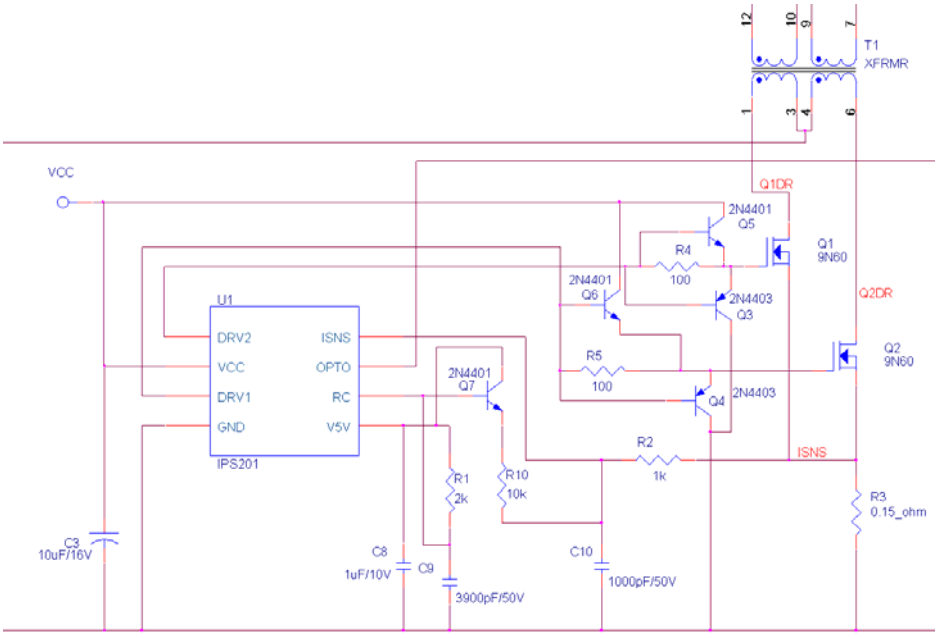
EXTERNAL COMPONENTS

DRIVE BOOST

For applications with large, high-gate-capacitance FETs, or for highest efficiency by having the fastest gate turn-on and turn-off, adding a pair of small bipolar transistors to the FET drive is useful. An example of how this can be done is shown below

SLOPE COMPENSATION

For current mode applications, it is often necessary to have slope compensation for stability reasons. This can be implemented by adding an NPN transistor plus a resistor to the V5V, RC, and ISNS pins as shown below. The sawtooth on the RC pin is buffered by the transistor to feed a variable, sloping current through the rolloff resistor and the current sense resistor, thereby adding a voltage slope to the signal seen at the ISNS pin. The amount of slope compensation is controlled by the ratio of the added resistor to the rolloff resistor (assuming the current sense resistor is small in comparison to these). The transistor reduces the load on the RC pin, but since some base current is being pulled out, the resistor and capacitor values setting the operating frequency and dead time may need a small adjustment to bring the design to the desired operating point. In most applications, there needs to be frequency compensation (R2, C10 below) to roll-off the high frequency loop gain, even if the duty cycle is low enough such that slope compensation isn't necessary

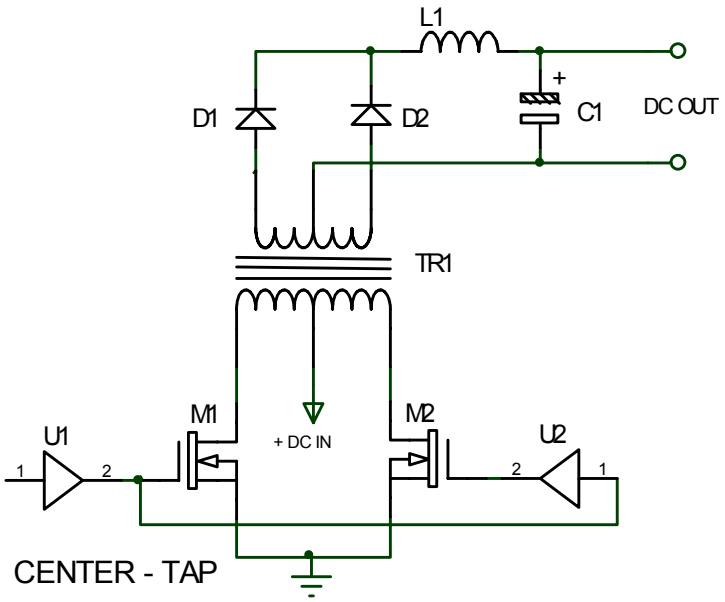


TARGETTED PUSH-PULL CONFIGURATIONS

The most frequently used Push-Pull configurations are shown below

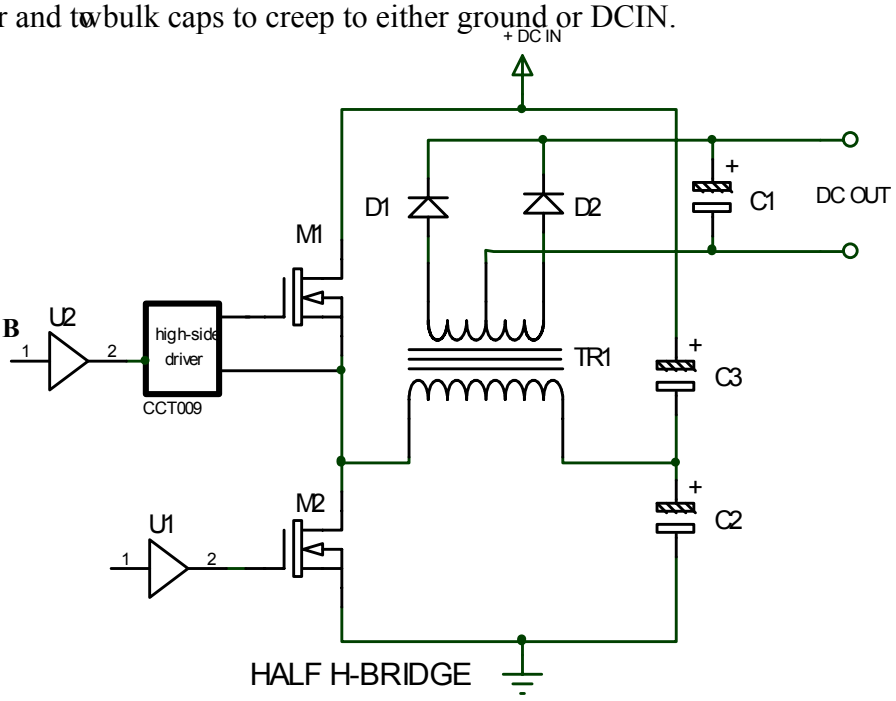
Center-tapped Configuration: This is the simplest and the cheapest possible Push-Pull configuration which is especially well suited when the input voltage does not exceed 250VDC (175VAC). At higher input voltages, this solution will require MOSFETs with high breakdown voltages and therefore becomes less economical and less efficient.

Figure 1A



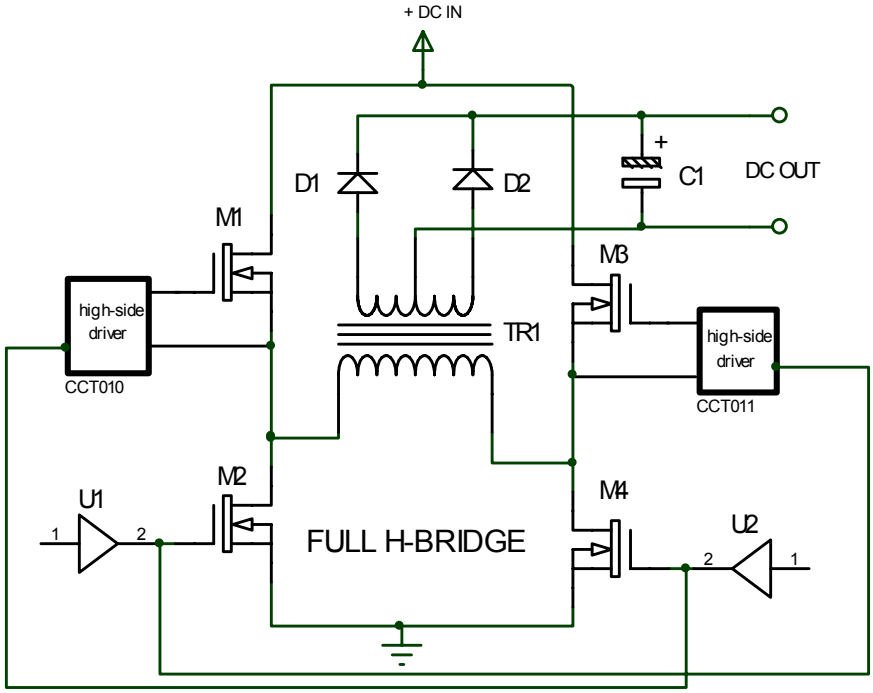
Half H-Bridge Configuration: This solution allows the utilization of low-cost 600V Mosfets up to 450V of DC input (320VAC), which is very economical. Also, the transformer is driven by a lower Peak-to-Peak voltage which considerably reduces and allows this configuration to achieve a very high efficiency. A reminder that simple current mode control will cause the connection point between the transformer and two bulk caps to creep to either ground or DCIN.

Figure 1B



Full H-Bridge Configuration: This configuration is essentially used in very high power applications.

Figure 1C



ORDERING INFORMATION/PART NUMBERS

Part Number	Temp. Range	Package	Packing	Packing Qty.
IPS201A C-D-G-LF	0°C to +70°C	DIP	Tube	50
IPS201A I-D-G-LF	-40°C to +85°C	DIP	Tube	50
IPS201A C-SO-G-LF	0°C to +70°C	SOIC	Tube	98
IPS201A I-SO-G-LF	-40°C to +85°C	SOIC	Tube	98
IPS201A C-SO-G-LF-TR	0°C to +70°C	SOIC	Tape and Reel	2500
IPS201A I-SO-G-LF-TR	-40°C to +85°C	SOIC	Tape and Reel	2500
IPS201B C-D-G-LF	0°C to +70°C	DIP	Tube	50
IPS201B I-D-G-LF	-40°C to +85°C	DIP	Tube	50
IPS201B C-SO-G-LF	0°C to +70°C	SOIC	Tube	98
IPS201B I-SO-G-LF	-40°C to +85°C	SOIC	Tube	98
IPS201B C-SO-G-LF-TR	0°C to +70°C	SOIC	Tape and Reel	2500
IPS201B I-SI-G-LF-TR	-40°C to +85°C	SOIC	Tape and Reel	2500

PACKAGE DIMENSIONS AND MARKING

The IPS201 is available in plastic 8-pin DIP and plastic 8-pin SOIC packages. Only ROHS-Lead Free is normally offered. Refer to the latest version of specification AAPS001 (ASIC Advantage's "Package Numbering, Marking, and Outline Standard," available at www.asicadvantage.com) for specific information concerning the package dimensions and package marking.

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