

TMC2249A

Digital Mixer

12 x 12 Bit, 60 MHz

Features

- 60 MHz input and computation rate
- Two 12-bit multipliers
- Separate data and coefficient inputs
- Independent, user-selectable pipeline delays of 1 to 16 clocks on all input ports
- Separate 16-bit input port allows cascading or addition of a constant
- User-selectable rounded output
- Internal 1/2 LSB rounding of products
- Fully registered, pipelined architecture
- Available in 120-Pin CPGA, PPGA, MPGA or MQFP

Applications

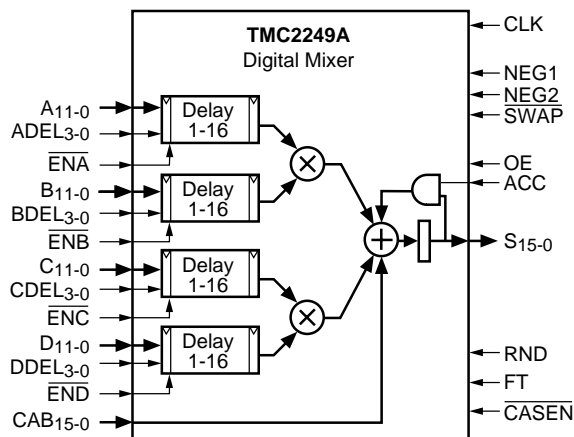
- Video switching
- Image mixing
- Digital signal modulation
- Complex frequency synthesis
- Digital filtering
- Complex arithmetic functions

Description

The TMC2249A is a high-speed digital arithmetic circuit consisting of two 12-bit multipliers, an adder and a cascade-able accumulator. All four multiplier inputs are simultaneously accessible to the user, and each includes a user-programmable pipeline delay of up to 16 clocks in length. The 24-bit adder/subtractor is followed by an accumulator and 16-bit input port which allows the user to cascade multiple TMC2249As. A new 16-bit accumulated output is available every clock, up to the maximum rate of 60 MHz. All inputs and outputs are registered except the three-state output enable, and all are TTL compatible.

The TMC2249A utilizes a pipelined, bus-oriented structure offering significant flexibility. Input register clock enables and programmable input data pipeline delays on each port offer an adaptable input structure for high-speed digital systems. Following the multipliers, the user may perform addition or subtraction of either product, arithmetic rounding to 16 bits, and accumulation and summation of products with a cascading input. The output port allows access to all 24 bits of the internal accumulator by switching between overlapping least and most-significant 16-bit words, and a three-state output enable simplifies connection to an external system bus.

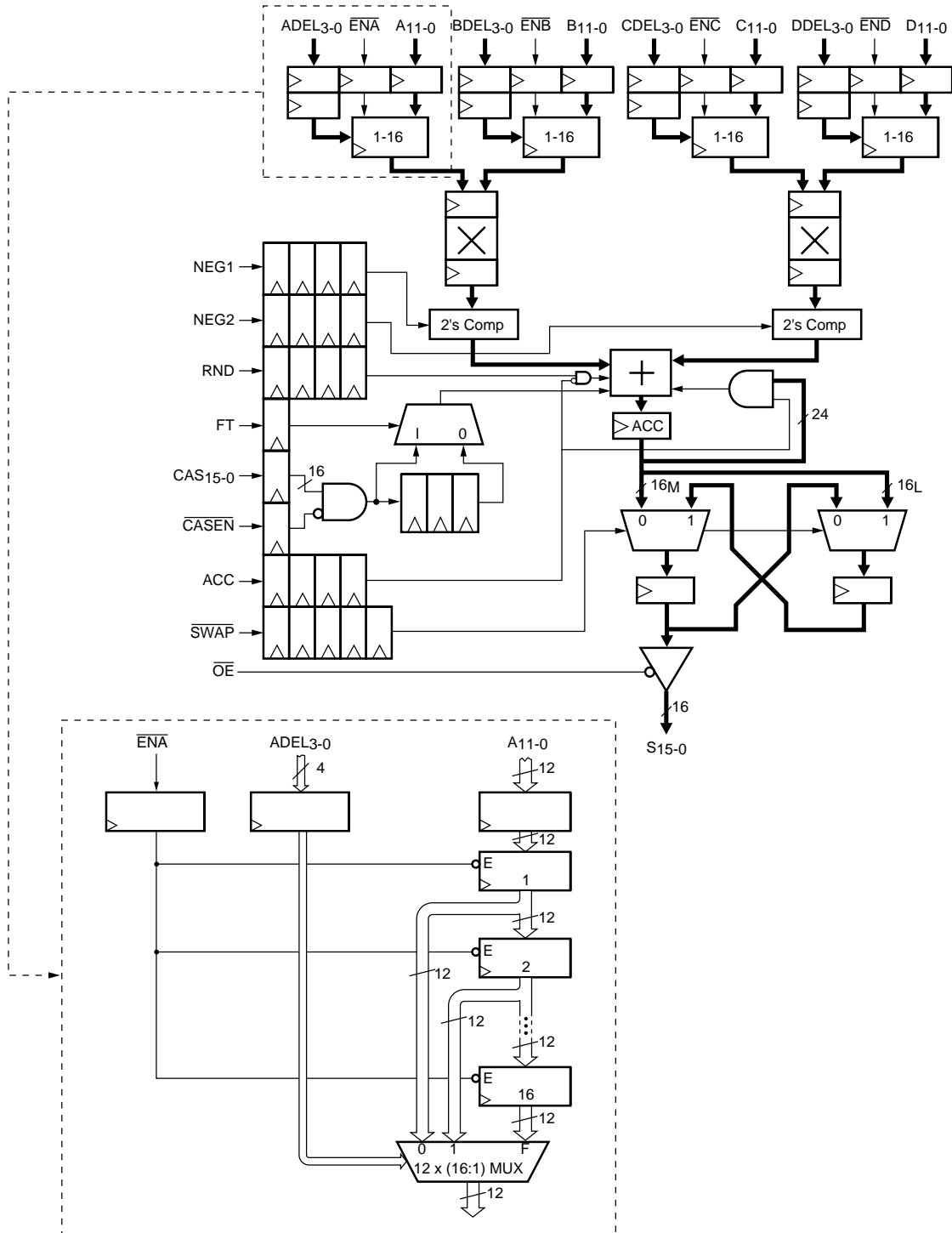
Logic Symbol



The TMC2249A has numerous applications in digital processing algorithms, from executing simple image mixing and switching, to performing complex arithmetic functions and complex waveform synthesis. FIR filters, digital quadrature mixers and modulators, and vector arithmetic functions may also be implemented with this device.

Fabricated in a submicron CMOS process, the TMC2249A operates at guaranteed clock rates of up to 60 MHz over the full temperature and supply voltage ranges. It is pin- and function-compatible with Fairchild's TMC2249, while providing higher speed operation and lower power dissipation. It is available in a 120 pin Ceramic Pin Grid Array (CPGA), 120 pin Plastic Pin Grid Array (PPGA), 120 lead MQFP to PPGA package (MPGA), and a 120 lead Metric Quad Flat-Pack (MQFP).

Block Diagram



Functional Description

The TMC2249A performs the summation of products described by the formula:

$$S(N+5) = A(N-ADEL) \times B(N-BDEL) \times (-1^{NEG1(N)}) + C(N-CDEL) \times D(N-DDEL) \times (-1^{NEG2(N)}) + CAS(N+3 \times FT)$$

where ADEL through DDEL range from 1 to 16 pipe delays.

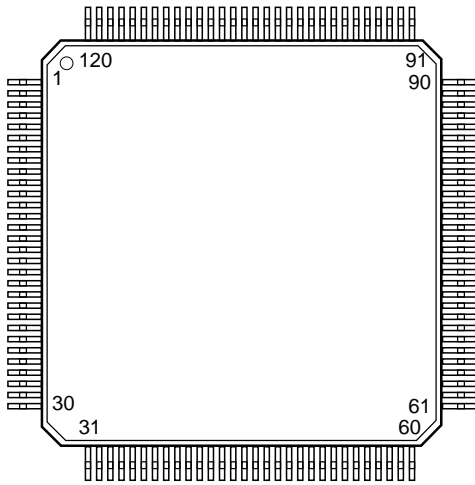
All inputs and controls utilize pipeline delay registers to maintain synchronicity with the data input during that clock,

except when the Cascade data input is routed directly to the accumulator by use of the Feedthrough control. One-half LSB rounding to 16 bits may be performed on the sum of products while summing with the cascade input data.

The user may access either the upper or lower 16 bits of the 24-bit accumulator by swapping overlapping registers. The output bus has an asynchronous high-impedance enable, to simplify interfacing to complex systems.

Pin Assignments

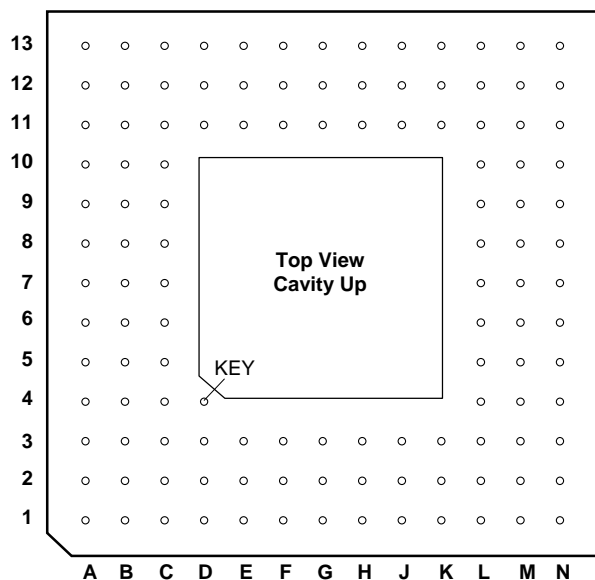
120 Pin Metric Quad Flat Pack, KE Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CLK	31	BDEL ₂	61	ADEL ₃	91	C ₁
2	ACC	32	BDEL ₃	62	ADEL ₂	92	C ₂
3	NEG1	33	ENB	63	ADEL ₁	93	C ₃
4	NEG2	34	B ₀	64	ADEL ₀	94	C ₄
5	RND	35	B ₁	65	NC	95	C ₅
6	S ₁₅	36	B ₂	66	CAS ₁₅	96	C ₆
7	S ₁₄	37	B ₃	67	CAS ₁₄	97	C ₇
8	GND	38	B ₄	68	CAS ₁₃	98	C ₈
9	S ₁₃	39	B ₅	69	CAS ₁₂	99	C ₉
10	S ₁₂	40	B ₆	70	CAS ₁₁	100	C ₁₀
11	S ₁₁	41	B ₇	71	CAS ₁₀	101	C ₁₁
12	VDD	42	GND	72	GND	102	VDD
13	S ₁₀	43	B ₈	73	CAS ₉	103	D ₁₁
14	S ₉	44	B ₉	74	CAS ₈	104	D ₁₀
15	S ₈	45	B ₁₀	75	CAS ₇	105	D ₉
16	GND	46	VDD	76	CAS ₆	106	GND
17	S ₇	47	B ₁₁	77	CAS ₅	107	D ₈
18	S ₆	48	A ₁₁	78	CAS ₄	108	D ₇
19	S ₅	49	A ₁₀	79	CAS ₃	109	D ₆
20	VDD	50	A ₉	80	CAS ₂	110	D ₅
21	S ₄	51	A ₈	81	CAS ₁	111	D ₄
22	S ₃	52	A ₇	82	CAS ₀	112	D ₃
23	S ₂	53	A ₆	83	CAS _{EN}	113	D ₂
24	GND	54	A ₅	84	FT	114	D ₁
25	S ₁	55	A ₄	85	CDEL ₀	115	D ₀
26	S ₀	56	A ₃	86	CDEL ₁	116	END
27	OE	57	A ₂	87	CDEL ₂	117	DDEL ₃
28	SWAP	58	A ₁	88	CDEL ₃	118	DDEL ₂
29	BDEL ₀	59	A ₀	89	ENC	119	DDEL ₁
30	BDEL ₁	60	ENA	90	C ₀	120	DDEL ₀

Pin Assignments

120 Pin Plastic Pin Grid Array, H5 Package, 120 Pin Ceramic Pin Grid Array, G1 Package, and 120 Pin Metric Quad FlatPack to 120 Pin Plastic Pin Array, H6 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	DDEL ₀	C5	D1	G11	CAS ₆	L10	A ₁
A2	DDEL ₃	C6	D5	G12	CAS ₇	L11	ADEL ₃
A3	END	C7	GND	G13	CAS ₅	L12	NC
A4	D2	C8	VDD	H1	S ₆	L13	CAS ₁₅
A5	D4	C9	C ₈	H2	S ₅	M1	OE
A6	D7	C10	C ₄	H3	VDD	M2	BDEL ₃
A7	D8	C11	C ₁	H11	GND	M3	B ₁
A8	D10	C12	ENC	H12	CAS ₉	M4	B ₃
A9	C11	C13	CDEL ₁	H13	CAS ₈	M5	B ₆
A10	C9	D1	S ₁₃	J1	S ₄	M6	B ₈
A11	C6	D2	S ₁₄	J2	S ₃	M7	B ₁₀
A12	C3	D3	GND	J3	GND	M8	A ₁₀
A13	C0	D11	CDEL ₃	J11	CAS ₁₃	M9	A ₇
B1	NEG1	D12	CDEL ₀	J12	CAS ₁₁	M10	A ₄
B2	ACC	D13	CASEN	J13	CAS ₁₀	M11	A ₀
B3	DDEL ₁	E1	S ₁₁	K1	S ₂	M12	ADEL ₂
B4	D0	E2	S ₁₂	K2	S ₁	M13	ADEL ₁
B5	D3	E3	GND	K3	SWAP	N1	BDEL ₁
B6	D6	E11	FT	K11	ADEL ₀	N2	ENB
B7	D9	E12	CAS ₀	K12	CAS ₁₄	N3	B ₂
B8	D11	E13	CAS ₁	K13	CAS ₁₂	N4	B ₅
B9	C10	F1	S ₉	L1	S ₀	N5	B ₇
B10	C7	F2	S ₁₀	L2	BDEL ₀	N6	B ₉
B11	C5	F3	VDD	L3	BDEL ₂	N7	B ₁₁
B12	C2	F11	CAS ₂	L4	B ₀	N8	A ₁₁
B13	CDEL ₂	F12	CAS ₃	L5	B ₄	N9	A ₈
C1	S ₁₅	F13	CAS ₄	L6	GND	N10	A ₆
C2	RND	G1	S ₇	L7	VDD	N11	A ₃
C3	CLK	G2	S ₈	L8	A ₉	N12	A ₂
C4	DDEL ₂	G3	GND	L9	A ₅	N13	ENA

Pin Descriptions

Pin Name	Pin Number		Pin Function Description
	CPGA/PPGA/MPGA	MQFP	
Power			
V _{DD}	F3, H3, L7, C8	12, 20, 46, 102	Supply Voltage. The TMC2249A operates from a single +5V supply. All power and ground pins must be connected.
GND	E3, G3, J3, L6, H11, C7	8, 16, 24, 42, 72, 106	Ground. The TMC2249A operates from a single +5V supply. All power and ground pins must be connected.
Clock			
CLK	C3	1	System Clock. The TMC2249A operates from a single master clock input. The rising edge of clock strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.
Inputs			
A ₁₁₋₀	N8, M8, L8, N9, M9, N10, L9, M10, N11, N12, L10, M11	48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59	A-D Input. A through D are the four 12-bit registered data input ports. A ₀ -D ₀ are the LSBs (see Table 1). Data presented to the input ports is clocked in to the top of the 16-stage delay pipeline on the next clock when enabled, "pushing" data down the register stack.
B ₁₁₋₀	N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, L4	47, 45, 44, 43, 41, 40, 39, 38, 37, 36, 35, 34	
C ₁₁₋₀	A9, B9, A10, C9, B10, A11, B11, C10, A12, B12, C11, A13	101, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90	
D ₁₁₋₀	B8, A8, B7, A7, A6, B6, C6, A5, B5, A4, C5, B4	103, 104, 105, 107, 108, 109, 110, 111, 112, 113, 114, 115	
ADEL ₃₋₀	L11, M12, M13, K11	61, 62, 63, 64	A-D Delay. ADEL through DDEL are the four-bit registered input data pipe delay select word inputs. Data to be presented to the multipliers is selected from one of sixteen stages in the input data delay pipe registers, as indicated by the delay select word presented to the respective input port during that clock. The minimum delay is one clock (select word=0000), and the maximum delay is 16 clocks (select word=1111). Following powerup these values are indeterminate and must be initialized by the user.
BDEL ₃₋₀	M2, L3, N1, L2	32, 31, 30, 29	
CDEL ₃₋₀	D11, B13, C13, D12	88, 87, 86, 85	
DDEL ₃₋₀	A2, C4, B3, A1	117, 118, 119, 120	
CAS ₁₅₋₀	L13, K12, J11, K13, J12, J13, H12, H13, G12, G11, G13, F13, F12, F11, E13, E12	66, 67, 68, 69, 70, 71, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82	Cascade Input. CAS is the 16-bit Cascade data input port. CAS ₀ is the LSB. See Table 1.
Controls			
S ₁₅₋₀	C1, D2, D1, E2, E1, F2, F1, G2, G1, H1, H2, J1, J2, K1, K2, L1	6, 7, 9, 10, 11, 13, 14, 15, 17, 18, 19, 21, 22, 23, 25, 26	Sum Output. The current 16-bit result is available at the Sum output. The output may be the most or least significant 16 bits of the current accumulator output, as determined by SWAP. S ₀ is the LSB. See Table 1.

Pin Descriptions (continued)

Pin Name	Pin Number		Pin Function Description
	CPGA/PPGA/MPGA	MQFP	
Controls			
EN \bar{A} -EN \bar{D}	N13, N2, C12, A3	60, 33, 89, 116	Input Enables. Input data presented to port i11-0 (i=A,B,C, or D) are latched into delay pipeline i, and data already in pipeline i advance by one register position, on each rising edge of CLK for which EN \bar{i} is LOW. When EN \bar{i} is HIGH, the data in pipeline i do not move and the value at the input port i will be lost before it reaches the multiplier.
NEG1,2	B1, D3	3, 4	Negate. The products of the multipliers are negated causing a subtraction to be performed during the internal summation of products, when the NEGate controls are HIGH, NEG1 negates the product A x B, while NEG2 acts on the output of the multiplier which generates the product C x D. When the length controls ADEL-DDEL are set to zero, these controls indicate the operation to be performed on data input during the same clock. As nonzero values for ADEL-DDEL do not affect the pipelining of these controls, their effect is not synchronous with the data input in these cases.
RND	C2	5	Round. When the rounding control is HIGH, the 24-bit sum of products resulting from data input during that clock is rounded to 16 bits. When enabled rounding is automatically performed only during the first cycle of each accumulation sequence, to avoid the accumulation of roundoff errors.
FT	E11	84	Feedthrough. When the Feedthrough control is HIGH, the pipeline delay through the cascade data path is minimized to simplify the cascading of multiple devices. When FT is LOW and ADEL through DDEL are all set to 0, the data inputs are aligned, such that $S(n+6) = CAS(n) + A(n)B(n) + C(n)D(n)$. See Table 2.
CASEN	D13	83	Cascade Enable. Data presented at the cascade data input port are latched and accumulated internally when the input enable CASEN during that clock is LOW. When CASEN is HIGH, the cascade input port is ignored.
ACC	B2	2	Accumulate. When the registered ACCumulator control is LOW, no internal accumulation will be performed on the data input during the current clock, effectively clearing the prior accumulated sum. When ACC is HIGH, the internal accumulator adds the emerging product to the sum of the previous products and RND is disabled.
SWAP	K3	28	Swap Output Words. The user may access both the most and least-significant 16 bits of the 24-bit accumulator by utilizing SWAP. Normal operation of the device, with SWAP = HIGH, outputs the most significant word. Setting SWAP = LOW puts a double-register structure into "toggle" mode, allowing the user to examine the LSW on alternate clocks. New output data will not be clocked into the output registers until SWAP returns HIGH.
OE	M1	27	Output Enable. Data currently in the output registers is available at the output bus S ₁₅₋₀ when the asynchronous Output Enable is LOW. When OE is HIGH, the outputs are in the high-impedance state.
No Connect			
	L12	65	Do Not Connect
	D4		Index Pin (optional)

Table 1. Data Formats and Bit Weighting

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
				-2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	DATA (A_{11-0} - D_{11-0})
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	CASCADE INPUT (CAS_{15-0})
SUM (S_{15-0})																
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	LSW
-2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	MSW

Notes:

- A minus sign indicates the two's complement sign bit.
- RND adds 1 to the 2^7 position if ACC is low.

Equivalent Circuits and Threshold Levels

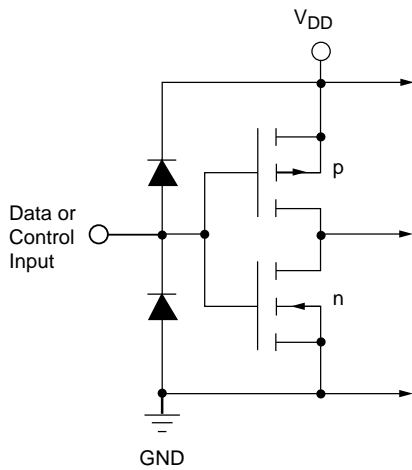


Figure 1. Equivalent Digital Input Circuit

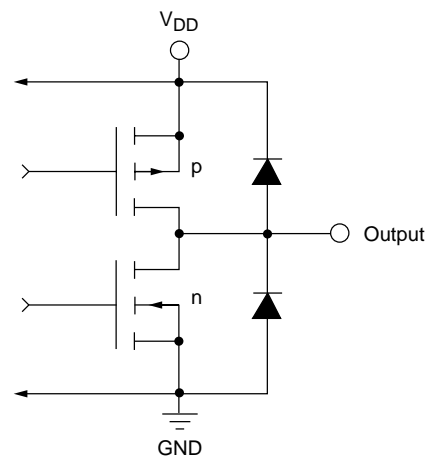


Figure 2. Equivalent Digital Output Circuit

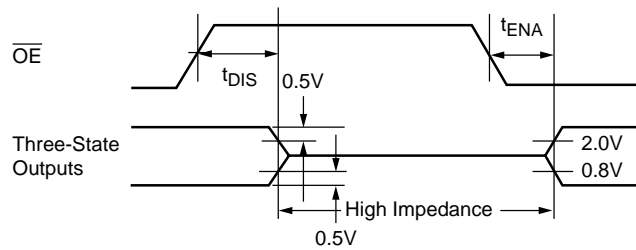


Figure 3. Threshold Levels for Three-State Measurement

Absolute Maximum Ratings (beyond which the device may be damaged)¹

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	$V_{DD} + 0.5$	V
Applied Voltage (Output) ²	-0.5	$V_{DD} + 0.5$	V
Externally Forced Current (Output) ^{3,4}	-3.0	6.0	mA
Output Short Circuit Duration (single output in HIGH state to ground)		1	sec
Operating, Ambient Temperature	-20	110	°C
Operating, Junction Temperature		140	°C
Storage Temperature	-65	150	°C
Lead, Soldering (10 seconds)		300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter			Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2249A			25	MHz
		TMC2249A-1			40	MHz
		TMC2249A-2			60	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		7			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1.5			ns
V_{IH}	Input Voltage, Logic HIGH	Data Inputs	2.0			V
		CLK Input	2.2			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

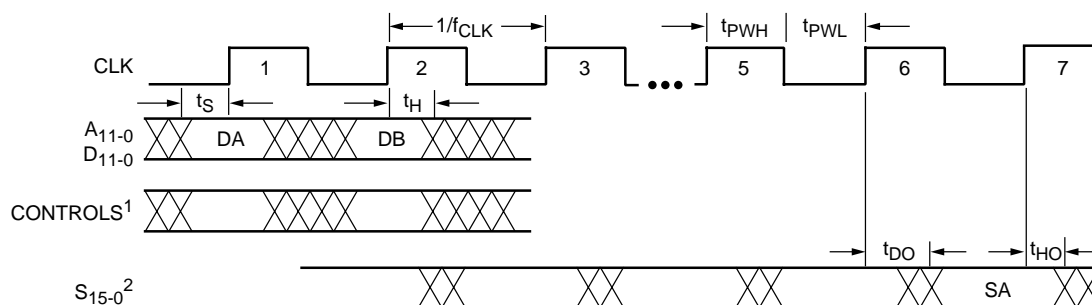
Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	$V_{DD} = \text{Max}$, $C_{LOAD} = 25\text{pF}$, $f_{CLK} = \text{Max}$				
		TMC2249A			75	mA
		TMC2249A-1			105	mA
		TMC2249A-2			145	mA
I_{DDU}	Power Supply Current, Unloaded	$V_{DD} = \text{Max}$, $\overline{OE} = \text{HIGH}$, $f_{CLK} = \text{Max}$				
		TMC2249A			68	mA
		TMC2249A-1			92	mA
		TMC2249A-2			124	mA
I_{DDQ}	Power Supply Current, Quiescent	$V_{DD} = \text{Max}$, $\text{CLK} = \text{LOW}$			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD}$			± 10	μA
I_{IL}	Input Current, LOW	$V_{DD} = \text{Max}$, $V_{IN} = 0\text{V}$			± 10	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	$V_{DD} = \text{Max}$, $V_{IN} = V_{DD}$			± 10	μA
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	$V_{DD} = \text{Max}$, $V_{IN} = 0\text{V}$			± 10	μA
I_{OS}	Short-Circuit Current		-20		-80	mA
V_{OH}	Output Voltage, HIGH	S_{15-0} , $I_{OH} = \text{Max}$	2.4			V
V_{OL}	Output Voltage, LOW	S_{15-0} , $I_{OL} = \text{Max}$			0.4	V

Switching Characteristics

Parameter	Conditions ¹	Min	Typ	Max	Units
t_{DO}	Output Delay Time	$C_{LOAD} = 25\text{pF}$		14	ns
t_{HO}	Output Hold Time	$C_{LOAD} = 25\text{pF}$	2.5		ns
t_{ENA}	Three-State Output Enable Delay	$C_{LOAD} = 0\text{pF}$		12	ns
t_{DIS}	Three-State Output Disable Delay	$C_{LOAD} = 0\text{pF}$		12	ns

Note:

- All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS} .



¹Except \overline{OE} .

²Assumes $\overline{OE} = \text{LOW}$ and ADEL-DDEL set to 0.

Figure 4. Timing Diagram

Application Notes

The TMC2249A is a flexible signal and image processing building block with numerous user-selectable functions which expand its usefulness. Table 2 clarifies the operation of the device, demonstrating the various feature available to the user and the timing delays incurred.

Table 2. TMC2249A Operation Sequence

CLK	ADEL	A ₁₁₋₀	BDEL	B ₁₁₋₀	CDEL	C ₁₁₋₀	DDEL	D ₁₁₋₀	NEG1	NEG2	CAS ₁₅₋₀	FT	ACC	RND	SWAP	S ₁₅₋₀
1	0	A(1)	0	B(1)	0	C(1)	0	D(1)	L	L	0	L	L	H	H	—
2	0	A(2)	0	B(2)	0	C(2)	0	D(2)	L	H	0	L	L	H	H	—
3	0	A(3)	0	B(3)	0	C(3)	0	D(3)	H	L	0	L	L	L	H	—
4	0	A(4)	0	B(4)	0	C(4)	0	D(4)	L	L	CAS(4)	L	L	L	H	—
5	0	A(5)	0	B(5)	0	C(5)	0	D(5)	L	L	0	L	L	L	H	—
6	0	A(6)	0	B(6)	0	C(6)	0	D(6)	L	L	0	L	L	H	H	$(A(1) \times B(1)+C(1) \times D(1)+2^7)$ ms
7	0	A(7)	0	B(7)	0	C(7)	0	D(7)	L	L	0	L	H	X	H	$(A(2) \times B(2)-C(2) \times D(2)+2^7)$ ms
8	0	A(8)	0	B(8)	0	C(8)	0	D(8)	L	L	CAS(8)	H	L	L	L	$(-A(3) \times B(3)+C(3) \times D(3))$ ms
9	0	A(9)	0	B(9)	0	C(9)	0	D(9)	L	L	0	L	L	H	H	$(A(4) \times B(4)+C(4) \times D(4)+CAS(4))$ ms
10																$(A(5) \times B(5)+C(5) \times D(5)+CAS(8))$ ms
11																$(A(6) \times B(6)+C(6) \times D(6)+2^7)$ ms
12																$(A(7) \times B(7)+C(7) \times D(7)+S(11))$ ms
13																$(S(12))_{ls}$
14																$(A(9) \times B(8)+C(7) \times D(6)+2^7)$ ms

CASEN = 0, H=HIGH, L=LOW, “ms” indicates most significant output word (bits 23-8), “ls” indicates least significant word (bits 15-0). The appropriate enables for the indicated data are assumed, otherwise ‘-’ indicates that port not enabled. Note that the output data summations including A(8)-D(8) is lost, since the output on cycle 13 is swapped to the LSW of S(12) on cycle 8. In general, RND may be left high unless the ls output is to be used, as on line 8 above.

Digital Filtering

The input structure of the TMC2249A demonstrates great versatility when all four multiplier inputs and the programmable delay registers are utilized.

Table 3 and Table 4 illustrate how a direct-form symmetric FIR filter of up to 32 taps can be implemented. By utilizing

the four input delay registers as pipelined storage banks, the user can store up to 32 coefficient-data word pairs, split into alternate "even" and "odd" halves. Two taps of the filter are calculated on each clock, and the user then increments/decrements the delay words (ADEL-DDEL). The sums of products are successively added to the global sum in the internal accumulator.

Table 3. FIR Filtering with the TMC2249A—Initial Data Loading

Register Position (Hex)	Even Data A	Odd Data C	Coefficient B	Storage D
0	x(31)	x(30)	h(0)	h(1)
1	x(29)	x(28)	h(2)	h(3)
2	x(27)	x(26)	h(4)	h(5)
3	x(25)	x(24)	h(6)	h(7)
4	x(23)	x(22)	h(8)	h(9)
5	x(21)	x(20)	h(10)	h(11)
6	x(19)	x(18)	h(12)	h(13)
7	x(17)	x(16)	h(14)	h(15)
8	x(15)	x(14)	h(15)	h(14)
9	x(13)	x(12)	h(13)	h(12)
A	x(11)	x(10)	h(11)	h(10)
B	x(9)	x(8)	h(9)	h(8)
C	x(7)	x(6)	h(7)	h(6)
D	x(5)	x(4)	h(5)	h(4)
E	x(3)	x(2)	h(3)	h(2)
F	x(1)	x(0)	h(1)	h(0)

Once all of the products of the desired taps have been summed, the result is available at the output. The user then "pushes" a new time-data sample on to the appropriate even or odd data register "stack" and reiterates the summation. Note that the coefficient bank "pointers", the BDEL and DDEL delay words, are alternately incremented and decremented on successive filter passes to maintain alignment between the incoming data samples and their respective coefficients.

The effective filter speed is calculated by dividing the clock rate by one-half the number of taps implemented.

Alternatively, non-symmetric FIR filters can be implemented using the TMC2249A in a similar fashion. Here, a shift register is used to delay the incoming data fed to the A input by an amount equal to one-half the length of the filter (the length of the A delay register).

As shown in Figure 5, the data is then sent to the C input, thus "stacking" the A and C delay registers to create a single N-tap FIR filter. The incremented delay words (ADEL-DDEL) for all four inputs are identical. Again, the filter throughput is equal to the clock speed divided by one-half the number of taps implemented.

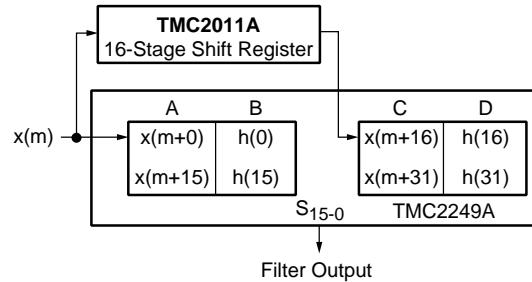


Figure 5. Non-Symmetric 32-Tap FIR Filtering Using the TMC2249A

Table 4. FIR Filtering – Operation Sequence

Cycle	Push A	B	Push C	D	ADEL	CDEL	BDEL	DDEL	ACC	ENA	ENB	ENC	END	Convolutional Sum	Resultant Output
1	-	-	-	-	0	0	0	0	L	H	H	H	H	$x(31) \bullet h(0) + x(30) \bullet h(1)$	See Note 2
2	-	-	-	-	1	1	1	1	H	H	H	H	H	$+x(29) \bullet h(2) + x(28) \bullet h(3)$	
3	-	-	-	-	2	2	2	2	H	H	H	H	H	$+x(27) \bullet h(4) + x(26) \bullet h(5)$	
4	-	-	-	-	3	3	3	3	H	H	H	H	H	$+x(25) \bullet h(6) + x(24) \bullet h(7)$	
5	-	-	-	-	4	4	4	4	H	H	H	H	H	$+x(23) \bullet h(8) + x(22) \bullet h(9)$	
6	-	-	-	-	5	5	5	5	H	H	H	H	H	$+x(21) \bullet h(10) + x(20) \bullet h(11)$	
7	-	-	-	-	6	6	6	6	H	H	H	H	H	$+x(19) \bullet h(12) + x(18) \bullet h(13)$	
8	-	-	-	-	7	7	7	7	H	H	H	H	H	$+x(17) \bullet h(14) + x(16) \bullet h(15)$	
9	-	-	-	-	8	8	8	8	H	H	H	H	H	$+x(15) \bullet h(15) + x(14) \bullet h(14)$	
10	-	-	-	-	9	9	9	9	H	H	H	H	H	$+x(13) \bullet h(13) + x(12) \bullet h(12)$	
11	-	-	-	-	A	A	A	A	H	H	H	H	H	$+x(11) \bullet h(11) + x(10) \bullet h(10)$	
12	-	-	-	-	B	B	B	B	H	H	H	H	H	$+x(9) \bullet h(9) + x(8) \bullet h(8)$	
13	-	-	-	-	C	C	C	C	H	H	H	H	H	$+x(7) \bullet h(7) + x(6) \bullet h(6)$	
14	-	-	-	-	D	D	D	D	H	H	H	H	H	$+x(5) \bullet h(5) + x(4) \bullet h(4)$	
15	-	-	-	-	E	E	E	E	H	H	H	H	H	$+x(3) \bullet h(3) + x(2) \bullet h(2)$	
16	-	-	x(32)	-	F	F	F	F	H	H	H	L	H	$+x(1) \bullet h(1) + x(0) \bullet h(0)$	
17	-	-	-	-	0	0	F	F	H	H	H	H	H	$+x(31) \bullet h(1) + x(32) \bullet h(0)$	
18	-	-	-	-	1	1	E	E	H	H	H	H	H	$+x(29) \bullet h(3) + x(30) \bullet h(2)$	
19	-	-	-	-	2	2	D	D	H	H	H	H	H	$+x(27) \bullet h(5) + x(28) \bullet h(4)$	
20	-	-	-	-	3	3	C	C	H	H	H	H	H	$+x(25) \bullet h(7) + x(26) \bullet h(6)$	
21	-	-	-	-	4	4	B	B	H	H	H	H	H	$+x(23) \bullet h(9) + x(24) \bullet h(8)$	
.															
.															

Notes:

1. If only the 16 MSBs of the result are used, the user may leave RND HIGH and SWAP low. If the 16 LSBs or all 24 bits of the result are used, then RND should be set low.

$$s = \sum_{K=0}^{15} (x(k)h(k) + x(k+16)h(k))$$

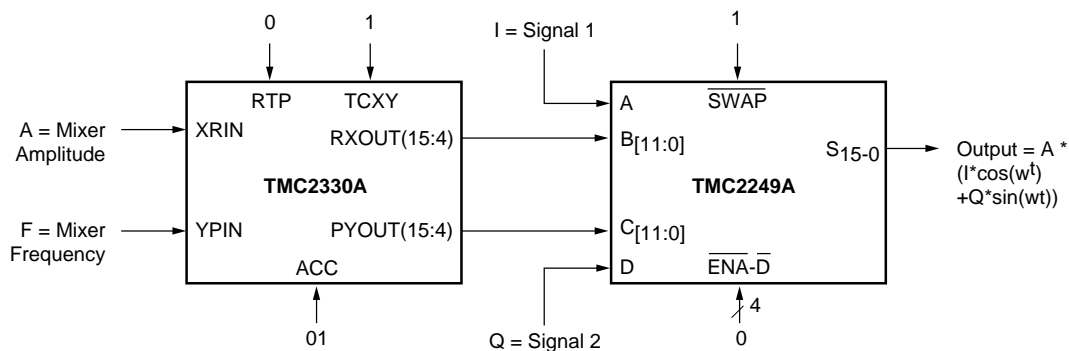


Figure 7. Direct Quadrature Waveform Synthesizer using the TMC2249A and TMC2330A

Related Products

- TMC2301 Image Resampling Sequencer
- TMC2302A Image Manipulation Sequencer
- TMC2246A Image Filter
- TMC2242B Half-Band Filter

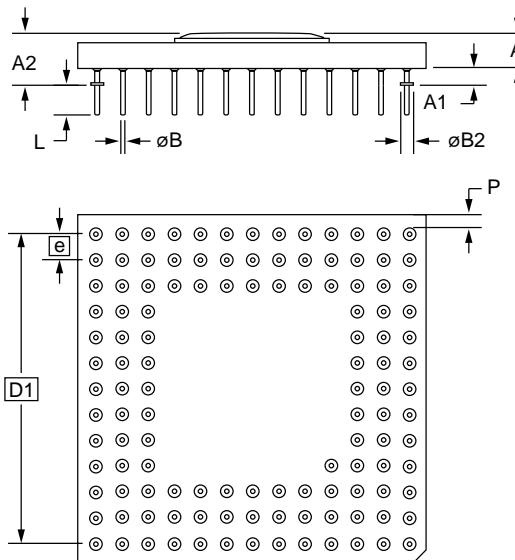
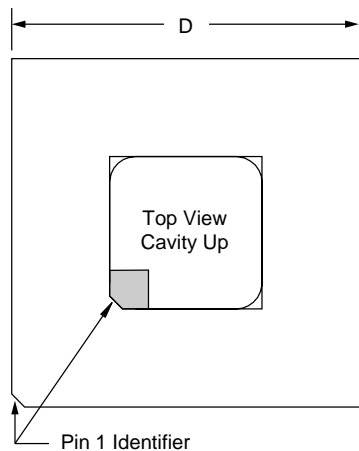
Mechanical Dimensions

120-Lead CPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



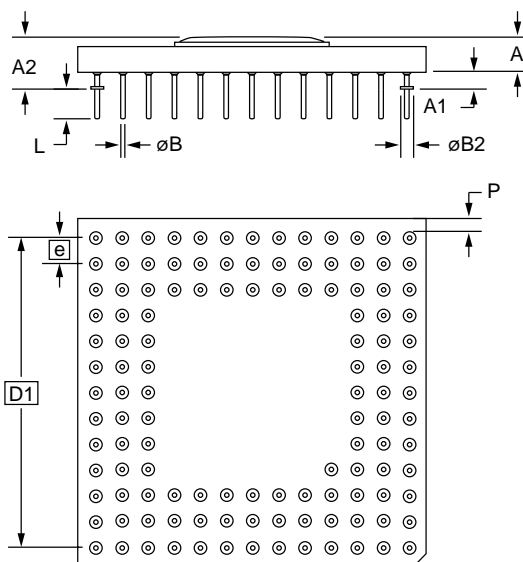
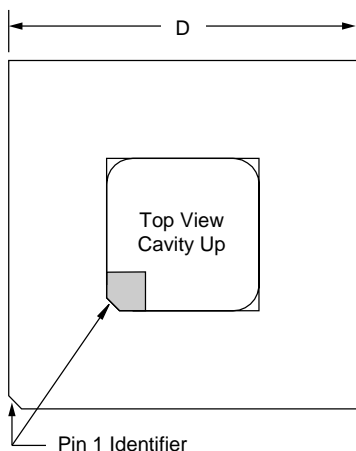
Mechanical Dimensions

120-Lead PPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



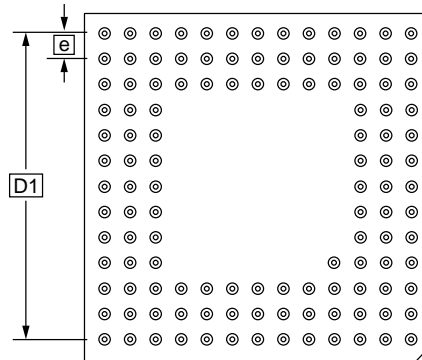
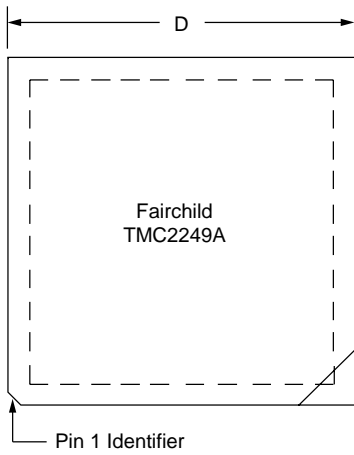
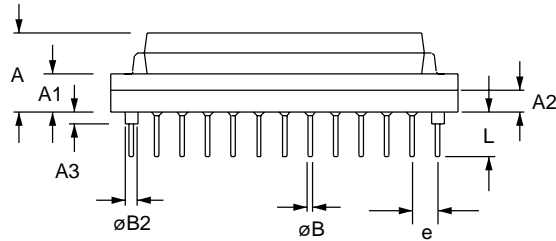
Mechanical Dimensions

120-Lead Metric Quad Flat Package to Pin Grid Array Package (MPGA)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.309	.311	7.85	7.90	
A1	.145	.155	3.68	3.94	
A2	.080	.090	2.03	2.29	
A3	.050 TYP.		1.27 TYP.		
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.355	1.365	34.42	34.67	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.175	.185	4.45	4.70	
M	13		13		3
N	120		120		4

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



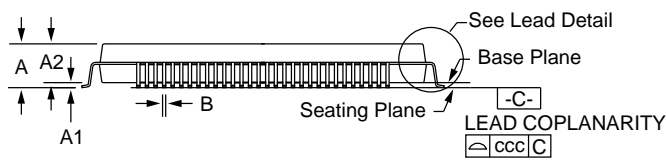
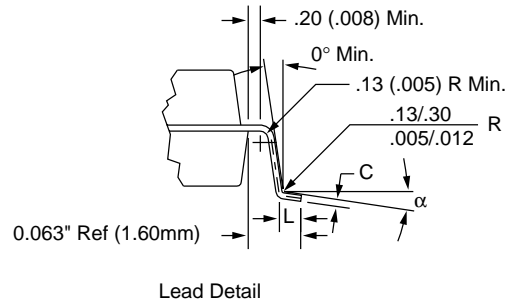
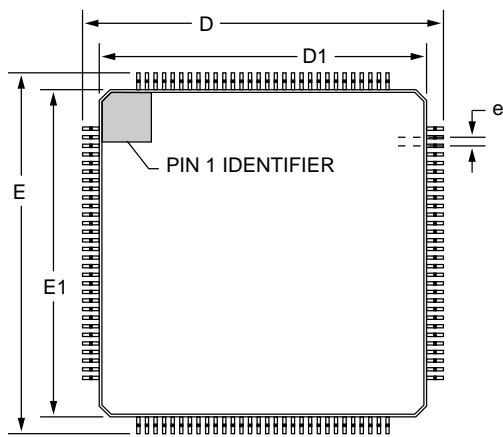
Mechanical Dimensions

120-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2249AG1C	0°C to 70°C	25 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2249AG1C
TMC2249AG1C1	0°C to 70°C	40 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2249AG1C1
TMC2249AG1C2	0°C to 70°C	60 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2249AG1C2
TMC2249AH5C	0°C to 70°C	25 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C
TMC2249AH5C1	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C1
TMC2249AH5C2	0°C to 70°C	60 MHz	Commercial	120 Pin Plastic Pin Grid Array	2249AH5C2
TMC2249AH6C	0°C to 70°C	25 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2249AH6C1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2249AH6C2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad Flat Pack to Pin Grid Array	N/A
TMC2249AKEC	0°C to 70°C	25 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC
TMC2249AKEC1	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC1
TMC2249AKEC2	0°C to 70°C	60 MHz	Commercial	120 Lead Metric Quad Flat Pack	2249AKEC2

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.