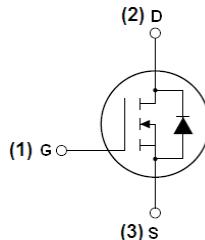


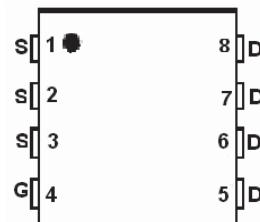
N-Channel Super Trench Power MOSFET

Description

The RM150N100ADF uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.



Schematic diagram



Marking and pin assignment



DFN5X6-8L top view

100% UIS TESTED!
100% ΔV_{ds} TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
FNA	RM150N100ADF	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Package Limited)	I_D	128	A
Drain Current-Continuous($T_c=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	81	A
Pulsed Drain Current	I_{DM}	400	A
Maximum Power Dissipation	P_D	125	W
Derating factor		0.7	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	180	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	R _{θJC}	1.0	°C/W
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Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

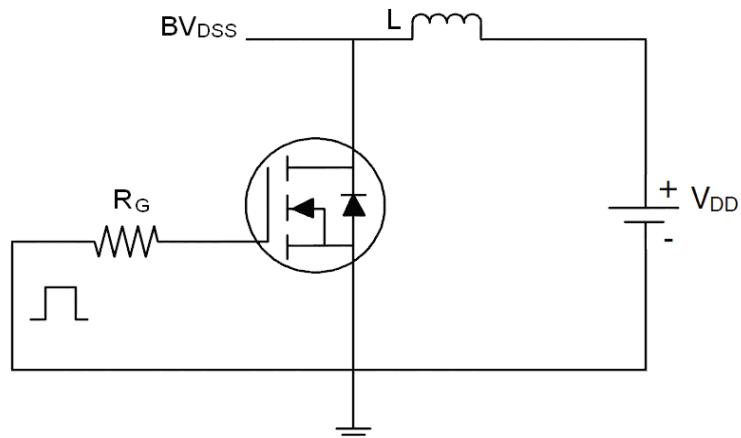
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.4	1.9	2.4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.7	4.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	-	50	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	3650	-	PF
Output Capacitance	C _{oss}		-	1110	-	PF
Reverse Transfer Capacitance	C _{rss}		-	43	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =20A V _{GS} =10V, R _G =10 Ω	-	13	-	nS
Turn-on Rise Time	t _r		-	19	-	nS
Turn-Off Delay Time	t _{d(off)}		-	45	-	nS
Turn-Off Fall Time	t _f		-	27	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =20A, V _{GS} =10V	-	75	-	nC
Gate-Source Charge	Q _{gs}		-	10	-	nC
Gate-Drain Charge	Q _{gd}		-	34	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	0.9	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 500A/μs ^(Note 3)	-	50	-	nS
Reverse Recovery Charge	Q _{rr}		-	275	-	nC

Notes:

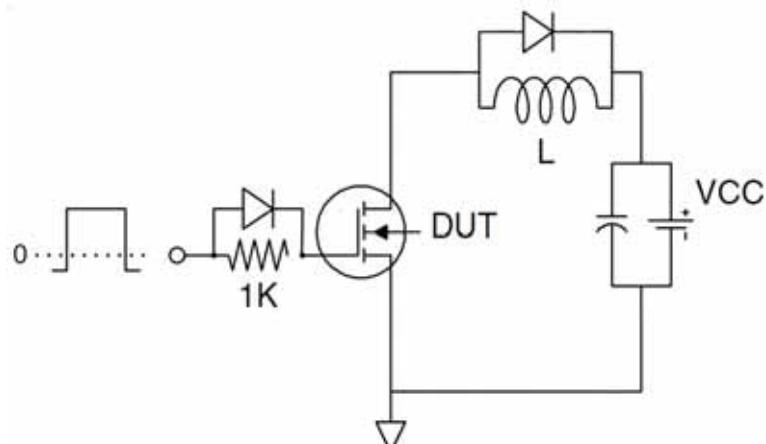
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : T_j=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25Ω

Test Circuit

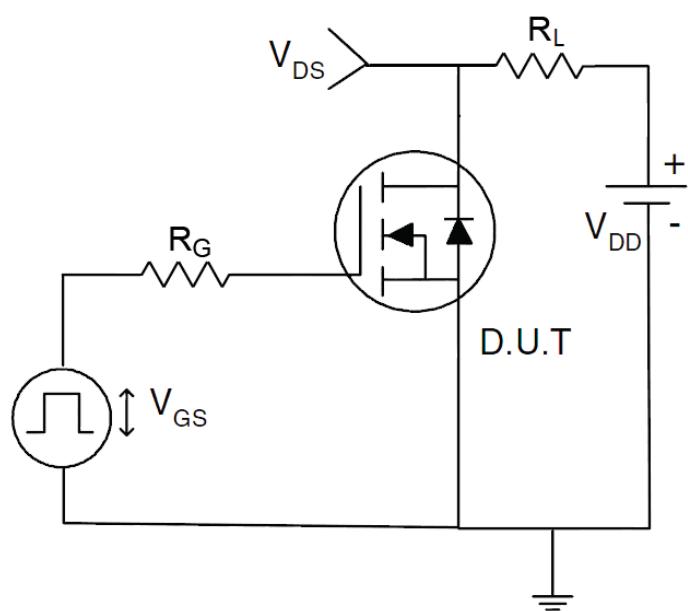
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



RATING AND CHARACTERISTICS CURVES (RM150N100ADF)

Fig 1. Typical Output Characteristics

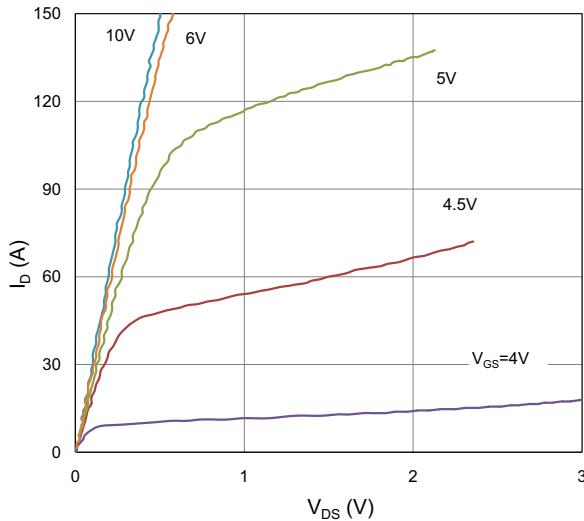


Figure 2. On-Resistance vs. Gate-Source Voltage

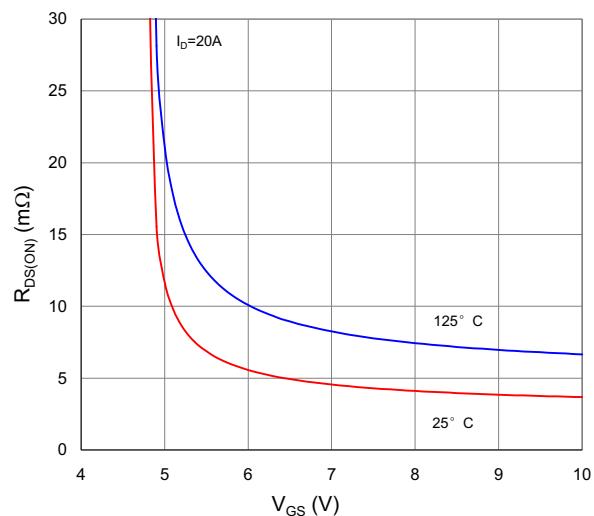


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

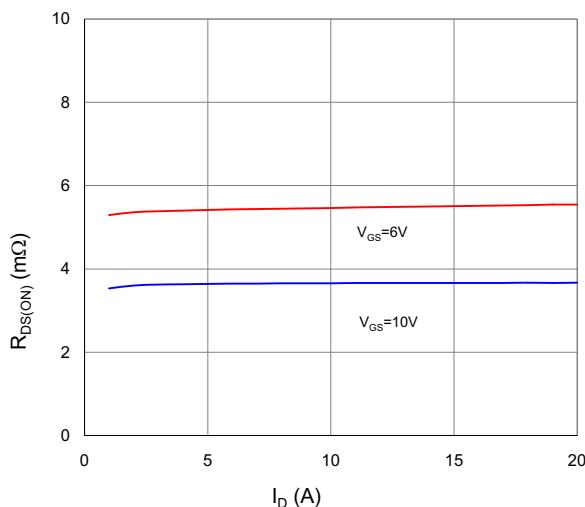


Figure 4. Normalized On-Resistance vs. Junction Temperature

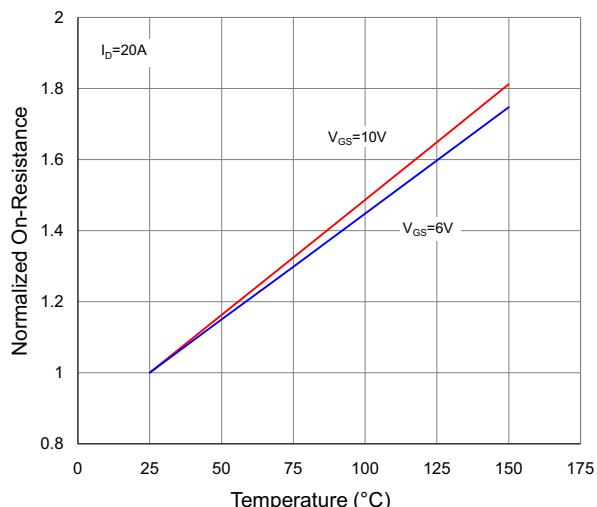


Figure 5. Typical Transfer Characteristics

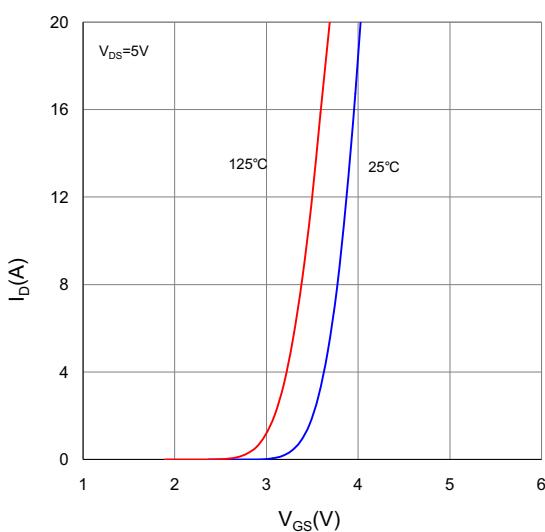
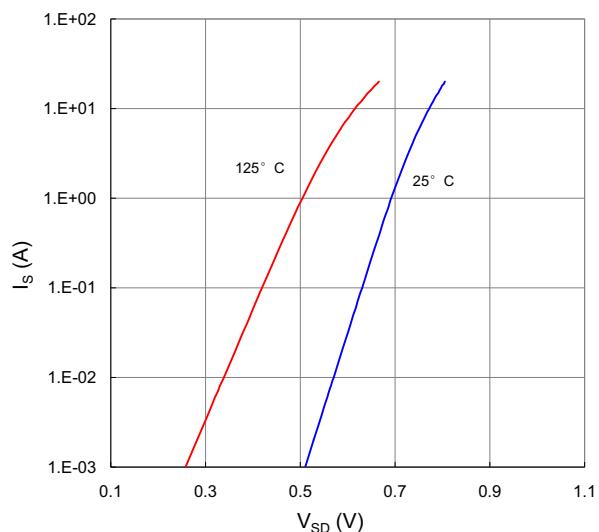


Figure 6. Typical Source-Drain Diode Forward Voltage



RATING AND CHARACTERISTICS CURVES (RM150N100ADF)

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

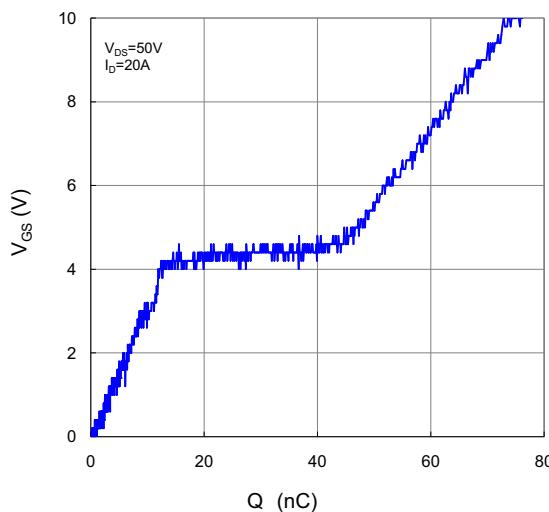


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

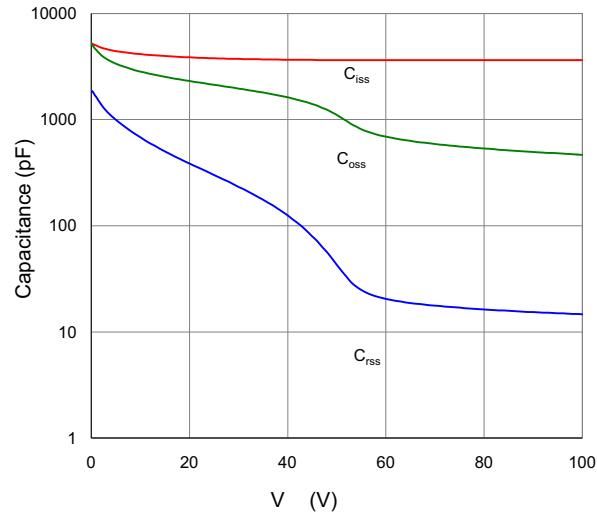


Figure 9. Maximum Safe Operating Area

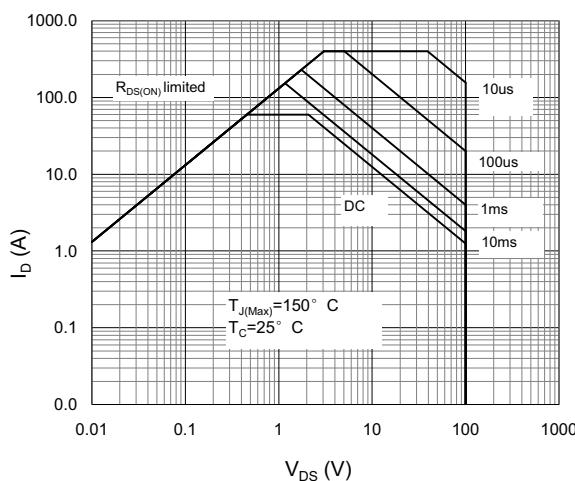


Figure 10. Maximum Drain Current vs. Case Temperature

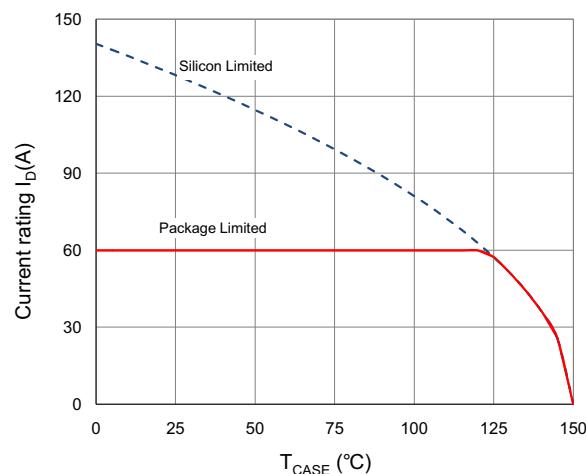
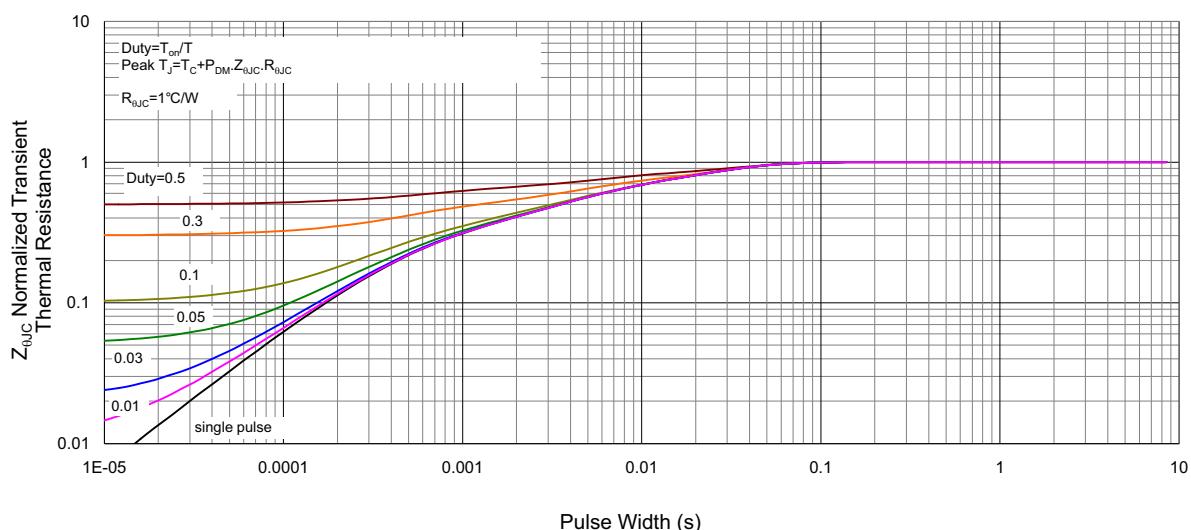
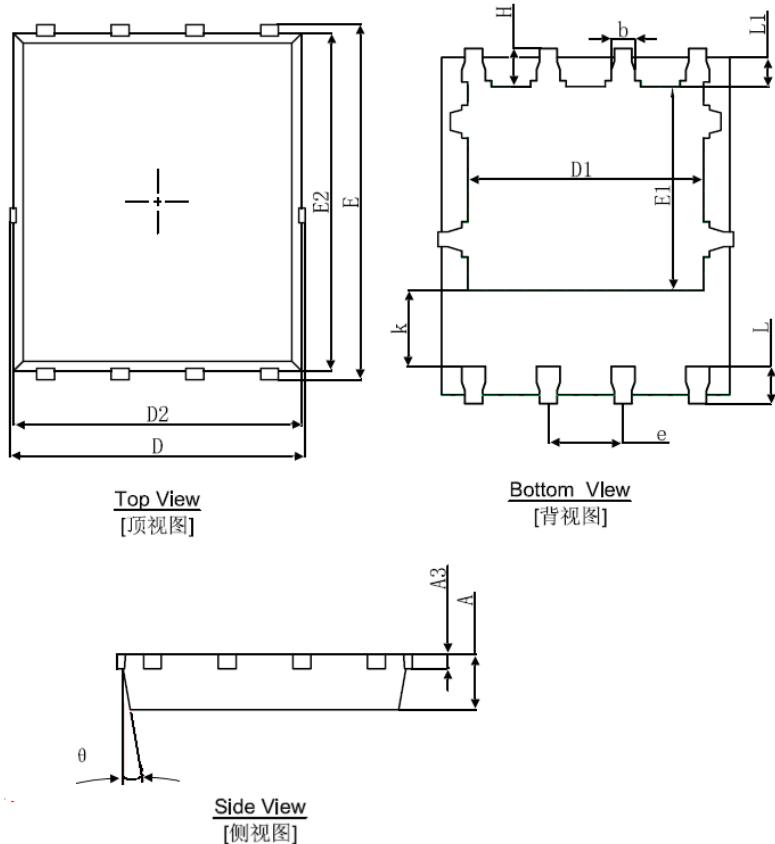


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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