X1000/E

IoT Application Processor

Data Sheet

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Disclaimer

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1 Overview

X1000/E is a low power consumption, high performance and high integrated application processor, the application is focus on IoT devices. And it can match the requirements of many other embedded products.

NAME	SIP LPDDR
X1000	32MB
X1000E	64MB

1.1 Block Diagram

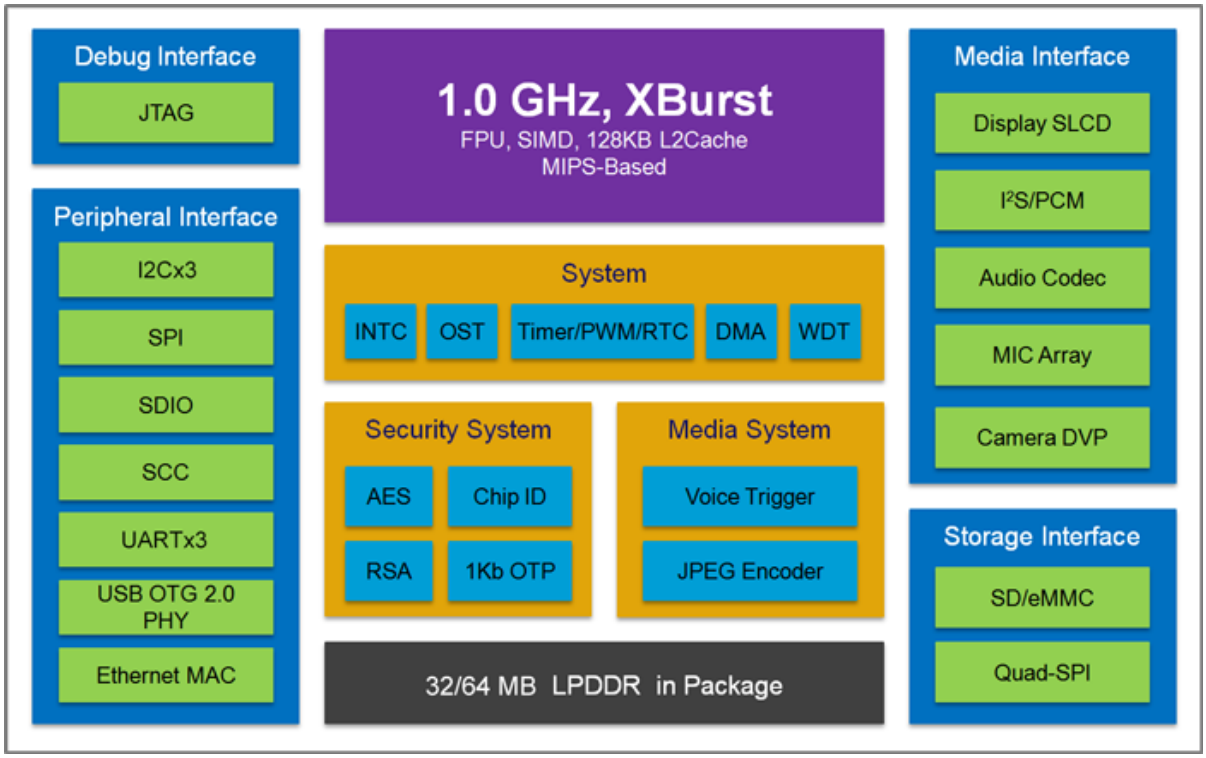


Figure 1-1 X1000/E Diagram

1.2 Features

1.2.1 CPU Core

- MIPS-Based XBurst® cores (up to 1.0GHz)
- MIPS-Based XBurst® CPU
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format

which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture
- MMU
  - 32-entry joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- L1 Cache
  - 16KB instruction cache
  - 16KB data cache
- Hardware debug support
- 16KB tight coupled memory
- L2 Cache
  - 128KB unify cache
- The XBurst® processor system supports little endian only

1.2.2 Image Core

- Hardware JPEG encoder
  - Baseline ISO/IEC 10918-1 JPEG compliant
  - 8-bit pixel depth support
  - Support for YUY2 ([Y0,U0,Y1,V0]) color
  - Up to four programmable Quantization tables
  - Fully programmable Huffman tables
  - Image size up to 2M pixels

1.2.3 Display/Camera/Audio

- LCD controller
  - Basic Features
    - Display size up to 640x480@60Hz,24BPP
  - Colors Supports
    - Support up to 16,777,216 (16M) colors
  - Panel Supports
    - 16bit 8080 once parallel interface
    - 9 bits twice 8080 parallel interface
    - 8 bits twice/third times 8080 parallel
    - Supports different size of display panel
    - Supports internal DMA operation and register operation
- Camera interface module
  - Input image size up to 2M pixels
  - Integrated DMA
  - Supported data format: YCbCr 4:2:2
  - Supports ITU656 (YCbCr 4:2:2) input

- Configurable VSYNC and HSYNC signals: active high/low
- Configurable PCLK: active edge rising/falling
- PCLK max. 80MHz
- Configurable output order

- AIC controller
  - I2S features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
    - Up to 8 channels sample data supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support share clock mode and split clock mode.
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
    - Internal I2S CODEC supported
    - Two FIFOs for transmit and receive respectively
- PCM interface
  - Support master mode and slave mode
  - Data starts with the frame PCMSYN or one PCMCLK later
  - Support three modes of operation for PCM
    - Short frame sync mode
    - Long frame sync mode
    - Multi-slot mode
  - Data is transferred and received with the MSB first
  - The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
  - The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK
  - 8/16 bit sample data sizes supported
  - DMA transfer mode supported
  - Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction
- Internal CODEC
  - 24 bits ADC and DAC(digital output)
  - PWM line out and can load down to 16 Ohm
  - Sample rate supported: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 88.2k, 96k, 176.4k, and 192k
  - Mono line input
  - DAC(digital output and converter to analog by external circuit): SNR: 95dB A-Weighted, THD: -80dB @FS-1dB
  - Line input to ADC path: SNR: 90dB A-Weighted, THD: -80dB @FS-1dB

- Separate power-down modes for ADC and DAC path with several shutdown modes
- Reduction of audible glitches systems: Soft Mute mode
- Embedded low noise Linear Regulator
- 1 MIC in path or 1 line in path Maximum (Total 1 analog input)

- Low power DMIC Controller
  - 16 bits data interface and 20bit precision internal controller.
  - SNR: 90dB, THD: -90dB @ FS -20dB
  - Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz. -36dB@10Hz
  - Low power voice trigger when waiting to start talking.
  - 1 to 4 channel MIC support.
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation.
  - Sample rate supported: 8k, 16k.
  - Support low power mode

1.2.4 Memory Interface

- DDR Controller
  - Support LPDDR, DDR2, DDR3
  - 16 bit data width
  - Support size up to 1GB (1 chip select, 3-bit Bank,15-bit Row, 11-bit Column,)
  - Asynchornize to system bus and each port.
  - Support clock-stop mode
  - Support auto self-refresh mode
  - Support power-down mode and deep-power-down mode
  - Programmable DDR timing parameters
  - Programmable DDR row and column address width and order

- X1000: 32MB SIP LPDDR
  X1000E: 64MB SIP LPDDR

- Serial nand/nor flash interface(SFC)
  - SPI protocol support: Standard, Dual, Quad SPI
  - Standard I/O data transfer up to 80Mbits/s
  - Dual I/O data transfer up to 160Mbits/s
  - Quad I/O data transfer up to 240Mbits/s
  - transmit-only or receive-only operation
  - MSB always be first in intra transfer of one byte. Least Significant Byte first for inter transfer of data bytes, and Most Significant Byte first for inter transfer of command or address bytes.
  - one device select
  - Configurable sampling point for reception
  - Configurable timing parameters: tSLCH, tCHSH and tSHSL
  - Configurable flash address wide are supported

- 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
- two data transfer mode: slave mode and DMA mode
- Configurable 6 phases for software flow

1.2.5 System Functions

- Clock generation and power management
  - On-chip oscillator circuit (support 24MHz, 26MHz)
  - Two phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK frequency can be changed separately for software by setting registers
  - Functional-unit clock gating
  - Supply block power shut down

- Timer and counter unit with PWM output and/or input edge counter
  - Provide 5 channels, all can generate PWM, two of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected

- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected

- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU and PDMA
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA

- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
    - PCLK, EXTAL and RTCCLK can be used as the clock for counter

- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

- PDMA Controller
  - Support up to 8 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode
  - A simple Xburst®-1 CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel

- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32KHz clock generation.
  - RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter

1.2.6 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 4 interrupts, 1 for every group, to INTC

- Three I2C Controller (I2C0, I2C1, I2C2)
  - Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator

- Master or slave I2C operation
- 7-bit addressing/10-bit addressing
- -level transmit and receive FIFOs
- Interrupt operation
- The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF

- One Smart Card Controller (SCC)
  - Supports normal card and UIM card.
  - Supports asynchronous character (T=0) communication modes.
  - Supports asynchronous block (T=1) communication modes.
  - Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.).
  - Supports extra guard time waiting.
  - Auto-error detection in T=0 receive mode.
  - Auto-character repeat in T=0 transmit mode.
  - Transforms inverted format to regular format and vice versa.
  - Support stop clock function in some power consuming sensitive applications.

- One Synchronous serial interfaces (SSI0)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI0_CE0_ / SSI0_CE1_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
  - Data transfer up to 30Mbits/s

- Three UARTs (UART0, UART1, UART2)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification

- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Fully compatible with the MMC System Specification version 4.5

- Support SD Specification 3.0
- Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
- Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
- Maximum data rate is 50MBps
- Both support MMC data width 1bit ,4bit, only MSC0 support 8bit
- Built-in programmable frequency divider for MMC/SD bus
- Built-in Special Descriptor DMA
- Mask-able hardware interrupt for SDIO interrupt, internal status and FIFO status
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt MMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 8 endpoints in device mode, 16 channels for host mode.
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer

- MAC controller
  - 10/100 Mbps operation
  - Supports RMII PHY interfaces
  - Supports VLAN and CRC
  - Station Management Agent (SMA)
  - remote wake-up frame and magic packet frame processing

- OTP Slave Interface
  - Total 1Kb.

1.2.7 Bootrom

16KB Boot ROM memory

2 Pinout Information

2.1 Pin Map

The X1000/E pin to ball assignment is shown in Figure 2-1.

X1000 Ball Assignment Ver1.0

BGA190, 13mm X 13mm X 1.2mm, 0.8pitch, top view

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	0
A		PC17	PC20	PC23	UART0_RTS_PC13	UART0_TXD_PC11	SFC_CLK_SSI0_CLK_PA26	VREF0	MSC0_D6_CIM_D2_PA17	MSC0_D4_CIM_D0_PA19	SD14_SLCD_D14_CIM_D5_PA14	MSC0_CMD_SSI0_CE0_PA25	MSC0_D0_SSI0_DR_PA23	MSC0_D2_SSI0_CE1_PA21	SD10_SLCD_D10_CIM_VSYN_PA10		A
B	PCM_DO_PC07	PC16	PC19	PC22	UART0_CTS_PC12	UART0_RXD_PC10	SFC_DT_SSI0_DT_PA29	SFC_DR_SSI0_DR_PA28	ZQ	MSC0_D5_CIM_D1_PA18	SD15_SLCD_D15_CIM_D4_PA15	MSC0_CLK_SSI0_CLK_PA24	MSC0_D1_SSI0_DT_PA22	MSC0_D3_SSI0_GPC_PA20	SD9_SLCD_D9_CIM_HSYN_PA09	SD7_SLCD_D7_PA07	B
C	PCM_CLK_PC06	PCM_SYN_PC09	PC18			SFC_HOLD_SSI0_GPC_PA31	SFC_CE_SSI0_CE0_PA27			MSC0_D7_CIM_D3_PA16	SD13_SLCD_D13_CIM_D6_PA13			SD11_SLCD_D11_CIM_MCLK_PA11	SD8_SLCD_D8_CIM_PCLK_PA08	SD5_SLCD_D5_UART1_TXD_PA05	C
D	MSC1_D0_PC02	PCM_DI_PC08				SFC_WP_SSI0_CE1_PA30					SD12_SLCD_D12_CIM_D7_PA12				WE_SLCD_WR_PB17	SD4_SLCD_D4_UART1_RXD_PA04	D
E	MSC1_CLK_PC00	MSC1_D1_PC03	MSC1_D3_PC05	PC21		LPDDR_VDD	VDDMEM	VDDMEM	VSSMEM	VSSMEM			CS2_SLCD_TE_PB19	WAIT_SLCD_DC_PB20	SD6_SLCD_D6_PA06	SD2_SLCD_D2_UART2_RXD_PA02	E
F	EXCLK_PB27	MSC1_CMD_PC01	MSC1_D2_PC04		LPDDR_VDDQ	LPDDR_VDD	VDDMEM	VDDMEM	VSSMEM	VSSMEM	VDD			CS1_SLCD_CE_PB18	SD3_SLCD_D3_UART2_TXD_PA03	SD0_SLCD_D0_SMB1_SCK_PA00	F
G	TDO_UART2_TXD	TDI_UART2_RXD	DMIC0_IN_PB22		LPDDR_VDDQ	LPDDR_VDD	VDDMEM	VDDMEM	VSSMEM	VSSMEM	VDD	VDD		RD_SLCD_RD_PB16	SD1_SLCD_D1_SMB1_SDA_PA01	SA14_MAC_MDIO_PB14	G
H	SMB0_SDA_SCC_DATA_PB24	AVDEFUSE			LPDDR_VDDQ	LPDDR_VDDQ	LPDDR_VDDQ			VDD	VDD	VDD			SA15_MAC_REF_CLK_PB15	SA12_MAC_TXD0_PB12	H
J	SMB1_SDA_PWM2_PC27	SMB0_SCK_SCC_CLK_PB23			LPDDR_VSSQ	LPDDR_VSSQ	LPDDR_VSS			VSS	VDD	VDD			SA13_MAC_MDC_PB13	SA11_MAC_TXD1_PB11	J
K	PWM0_PC25	SMB1_SCK_PWM1_PC	pad_TRST_		LPDDR_VSSQ	LPDDR_VSSQ	LPDDR_VSS	VSS	VSS	VSS	VDDIO	VDDIO		SA10_MAC_TXEN_PB10	SA9_MAC_RXD0_PB09	SA8_MAC_RXD1_PB08	K
L	PWM4_PC24	BOOT_SEL1_PB29	TCK			LPDDR_VSSQ	LPDDR_VSS	VSS	VSS	VSS	VSS	VDDIO		SA7_MAC_CRS_DV_PB07	SA6_MAC_PHY_CLK_PWM3_PB06	VDDIO_CODEC	L
M	BOOT_SEL2_PB30	BOOT_SEL0_PB28	TMS					VSS	VSS	VSS				VSSIO_CODEC	CODEC_PWMRP	CODEC_PWMRN	M
N	UART2_RXD_UART1_RTS_PD05	UART2_TXD_UART1_CTS_PD04				VDDIO_5V	VSSRTC								CODEC_PWMLP	CODEC_PWMLN	N
P	SSI0_DR_UART1_TXD_PD03	SSI0_DT_UART1_RXD_PD02	SSI0_CLK_SMB2_SCK_PD00			pad_PPRST_	pad_TEST_TE		PLL_DVSS	PLL_AVSS	OTG_ID		OTG_VBUS	CODEC_AVSS	CODEC_VREFP	CODEC_AVDD	P
R	SSI0_CE0_SMB2_SDA_PD01	SA0_I2S_MCLK_PB00	SA3_I2S_DI_PB03	SA4_I2S_DO_PB04	DMIC_CLK_PB21	WKUP_PB31	PWRON	RTCLK	PLL_AVDD	EXCLK_O	AVSOTG	OTG_DP	OTG_TXR_RKL	MICBIAS	AIN	AIP	R
T		SA1_I2S_BCLK_PB01	SA2_I2S_LRCLK_PB02	SA5_DMIC1_IN_PB05	RTC32K_PB26	VDDRTC	LDOOUT	XRTCLK	PLL_DVDD	EXCLK_I	DRV_VBUS_PB25	OTG_DM	AVDOTG25	AVDOTG	VCAP		T
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	0

Figure 2-1 X1000/E pin to ball assignment

2.2 Pin Descriptions

2.2.1 GPIO Group A

Table 2-1 GPIO Group A Pinmux(32)

Ball No.	Ball Name	In/Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
F16	SD0_SLCD_D0_I2C1_SCK_PA00	IO	PU	Enable	8mA	No		GPA[0]	SD0	SLCD_D0	I2C1_SCK	WKUP	VDDIO
G15	SD1_SLCD_D1_I2C1_SDA_PA01	IO	PU	Enable	8mA	No		GPA[1]	SD1	SLCD_D1	I2C1_SDA	WKUP	VDDIO
E16	SD2_SLCD_D2_UART2_RXD_PA02	IO	PU	Enable	8mA	No		GPA[2]	SD2	SLCD_D2	UART2_RXD	WKUP	VDDIO
F15	SD3_SLCD_D3_UART2_TXD_PA03	IO	PU	Enable	8mA	No		GPA[3]	SD3	SLCD_D3	UART2_TXD	WKUP	VDDIO
D16	SD4_SLCD_D4_UART1_RXD_PA04	IO	PU	Enable	8mA	No		GPA[4]	SD4	SLCD_D4	UART1_RXD	WKUP	VDDIO
C16	SD5_SLCD_D5_UART1_TXD_PA05	IO	PU	Enable	8mA	No		GPA[5]	SD5	SLCD_D5	UART_TXD	WKUP	VDDIO
E15	SD6_SLCD_D6_PA06	IO	PU	Enable	8mA	No		GPA[6]	SD6	SLCD_D6		WKUP	VDDIO
B16	SD7_SLCD_D7_PA07	IO	PU	Enable	8mA	No		GPA[7]	SD7	SLCD_D7		WKUP	VDDIO
C15	SD8_SLCD_D8_CIM_PCLK_PA08	IO	PU	Enable	8mA	No		GPA[8]	SD8	SLCD_D8	CIM_PCLK	WKUP	VDDIO
B15	SD9_SLCD_D9_CIM_HSYN_PA09	IO	PU	Enable	8mA	No		GPA[9]	SD9	SLCD_D9	CIM_HSYN	WKUP	VDDIO
A15	SD10_SLCD_D10_CIM_VSYN_PA10	IO	PU	Enable	8mA	No		GPA[10]	SD10	SLCD_D10	CIM_VSYN	WKUP	VDDIO
C14	SD11_SLCD_D11_CIM_MCLK_PA11	IO	PU	Enable	8mA	No		GPA[11]	SD11	SLCD_D11	CIM_MCLK	WKUP	VDDIO
D11	SD12_SLCD_D12_CIM_D7_PA12	IO	PU	Enable	8mA	No		GPA[12]	SD12	SLCD_D12	CIM_D7	WKUP	VDDIO
C11	SD13_SLCD_D13_CIM_D6_PA13	IO	PU	Enable	8mA	No		GPA[13]	SD13	SLCD_D13	CIM_D6	WKUP	VDDIO
A11	SD14_SLCD_D14_CIM_D5_PA14	IO	PU	Enable	8mA	No		GPA[14]	SD14	SLCD_D14	CIM_D5	WKUP	VDDIO
B11	SD15_SLCD_D15_CIM_D4_PA15	IO	PU	Enable	8mA	No		GPA[15]	SD15	SLCD_D15	CIM_D4	WKUP	VDDIO
C10	MSC0_D7_CIM_D3_PA16	IO	PU	Enable	8mA	No		GPA[16]		MSC0_D7	CIM_D3	WKUP	VDDIO
A9	MSC0_D6_CIM_D2_PA17	IO	PU	Enable	8mA	No		GPA[17]		MSC0_D6	CIM_D2	WKUP	VDDIO
B10	MSC0_D5_CIM_D1_PA18	IO	PU	Enable	8mA	No		GPA[18]		MSC0_D5	CIM_D1	WKUP	VDDIO

A10	MSC0_D4_CIM_D0_PA19	IO	PU	Enable	8mA	No		GPA[19]		MSC0_D4	CIM_D0	WKUP	VDDIO
B14	MSC0_D3_SSI0_GPC_PA20	IO	PU	Enable	8mA	No		GPA[20]		MSC0_D3	SSI0_GPC	WKUP	VDDIO
A14	MSC0_D2_SSI0_CE1_PA21	IO	PU	Enable	8mA	No		GPA[21]		MSC0_D2	SSI0_CE1	WKUP	VDDIO
B13	MSC0_D1_SSI0_DT_PA22	IO	PU	Enable	8mA	No		GPA[22]		MSC0_D1	SSI0_DT	WKUP	VDDIO
A13	MSC0_D0_SSI0_DR_PA23	IO	PU	Enable	8mA	No		GPA[23]		MSC0_D0	SSI0_DR	WKUP	VDDIO
B12	MSC0_CLK_SSI0_CLK_PA24	IO	PU	Enable	8mA	No		GPA[24]		MSC0_CLK	SSI0_CLK	WKUP	VDDIO
A12	MSC0_CMD_SSI0_CE0_PA25	IO	PU	Enable	8mA	No		GPA[25]		MSC0_CMD	SSI0_CE0	WKUP	VDDIO
A7	SFC_CLK_SSI0_CLK_PA26	IO	PU	Enable	8mA	No		GPA[26]		SFC_CLK	SSI0_CLK	WKUP	VDDIO
C7	SFC_CE_SSI0_CE0_PA27	IO	PU	Enable	8mA	No		GPA[27]		SFC_CE	SSI0_CE0	WKUP	VDDIO
B8	SFC_DR_SSI0_DR_PA28	IO	PU	Enable	8mA	No		GPA[28]		SFC_DR	SSI0_DR	WKUP	VDDIO
B7	SFC_DT_SSI0_DT_PA29	IO	PU	Enable	8mA	No		GPA[29]		SFC_DT	SSI0_DT	WKUP	VDDIO
D6	SFC_WP_SSI0_CE1_PA30	IO	PU	Enable	8mA	No		GPA[30]		SFC_WP	SSI0_CE1	WKUP	VDDIO
C6	SFC_HOLD_SSI0_GPC_PA31	IO	PU	Enable	8mA	No		GPA[31]		SFC_HOLD	SSI0_GPC	WKUP	VDDIO

2.2.2 GPIO Group B

Table 2-2 GPIO Group B Pinmux(32)

Ball No.	Ball Name	In/Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
R2	SA0_I2S_MCLK_PB00	IO	PU	Enable	8mA	No		GPB[0]	SA0	I2S_MCLK		WKUP	VDDIO
T2	SA1_I2S_BCLK_PB01	IO	PU	Enable	8mA	No		GPB[1]	SA1	I2S_BCLK		WKUP	VDDIO
T3	SA2_I2S_LRCLK_PB02	IO	PU	Enable	8mA	No		GPB[2]	SA2	I2S_LRCLK		WKUP	VDDIO
R3	SA3_I2S_DI_PB03	IO	PU	Enable	8mA	No		GPB[3]	SA3	I2S_DI		WKUP	VDDIO
R4	SA4_I2S_DO_PB04	IO	PU	Enable	8mA	No		GPB[4]	SA4	I2S_DO		WKUP	VDDIO

T4	SA5_DMIC1_IN_PB05	IO	PU	Enable	8mA	No		GPB[5]	SA5	DMIC1_IN		WKUP	VDDIO
L15	SA6_MAC_PHY_CLK_PWM3_PB06	IO	PU	Enable	8mA	No		GPB[6]	SA6	MAC_PHY_CLK	PWM3	WKUP	VDDIO
L14	SA7_MAC_CRS_DV_PB07	IO	PU	Enable	8mA	No		GPB[7]	SA7	MAC_CRS_DV		WKUP	VDDIO
K16	SA8_MAC_RXD1_PB08	IO	PU	Enable	8mA	No		GPB[8]	SA8	MAC_RXD1		WKUP	VDDIO
K15	SA9_MAC_RXD0_PB09	IO	PU	Enable	8mA	No		GPB[9]	SA9	MAC_RXD0		WKUP	VDDIO
K14	SA10_MAC_TXEN_PB10	IO	PU	Enable	8mA	No		GPB[10]	SA10	MAC_TXEN		WKUP	VDDIO
J16	SA11_MAC_TXD1_PB11	IO	PU	Enable	8mA	No		GPB[11]	SA11	MAC_TXD1		WKUP	VDDIO
H16	SA12_MAC_TXD0_PB12	IO	PU	Enable	8mA	No		GPB[12]	SA12	MAC_TXD0		WKUP	VDDIO
J15	SA13_MAC_MDC_PB13	IO	PU	Enable	8mA	No		GPB[13]	SA13	MAC_MDC		WKUP	VDDIO
G16	SA14_MAC_MDIO_PB14	IO	PU	Enable	8mA	No		GPB[14]	SA14	MAC_MDIO		WKUP	VDDIO
H15	SA15_MAC_REF_CLK_PB15	IO	PU	Enable	8mA	No		GPB[15]	SA15	MAC_REF_CLK		WKUP	VDDIO
G14	RD_SLCD_RD_PB16	IO	PU	Enable	8mA	No		GPB[16]	RD	SLCD_RD		WKUP	VDDIO
D15	WE_SLCD_WR_PB17	IO	PU	Enable	8mA	No		GPB[17]	WE	SLCD_WR		WKUP	VDDIO
F14	CS1_SLCD_CE_PB18	IO	PU	Enable	8mA	No		GPB[18]	CS1	SLCD_CE		WKUP	VDDIO
E13	CS2_SLCD_TE_PB19	IO	PU	Enable	8mA	No		GPB[19]	CS2	SLCD_TE		WKUP	VDDIO
E14	WAIT_SLCD_DC_PB20	IO	PU	Enable	8mA	No		GPB[20]	WAIT	SLCD_DC		WKUP	VDDIO
R5	DMIC_CLK_PB21	IO	PU	Enable	8mA	No		GPB[21]	DMIC_CLK			WKUP	VDDIO
G3	DMIC0_IN_PB22	IO	PU	Enable	8mA	No		GPB[22]	DMIC0_IN			WKUP	VDDIO
J2	I2C0_SCK_SCC_CLK_PB23	IO	PU	Enable	8mA	No		GPB[23]	I2C0_SC	SCC_CLK		WKUP	VDDIO
H1	I2C0_SDA_SCC_DATA_PB24	IO	PU	Enable	8mA	No		GPB[24]	I2C0_SDA	SCC_DATA		WKUP	VDDIO
T11	DRV_VBUS_PB25	IO	PD	Enable	8mA	No		GPB[25]	DRV_VBUS			WKUP	VDDIO
T5	RTC32K_PB26	IO	PU	Enable	8mA	No		GPB[26]	RTC32K			WKUP	VDDRTC
F1	EXCLK_PB27	IO	PU	Enable	8mA	No		GPB[27]	EXCLK			WKUP	VDDIO
M2	BOOT_SEL0_PB28	IO	PU	Disable	8mA	No		GPB[28]	BOOT_SEL0			WKUP	VDDIO
L2	BOOT_SEL1_PB29	IO	PU	Disable	8mA	No		GPB[29]	BOOT_SEL1			WKUP	VDDIO

M1	BOOT_SEL2_PB30	IO	PU	Disable	8mA	No		GPB[30]	BOOT_SEL2			WKUP	VDDIO
R6	WKUP_PB31	IO	PU	Enable	8mA	Yes		GPB[31]	WKUP			WKUP	VDDRTC

2.2.3 GPIO Group C

Table 2-3 GPIO Group C Pinmux(26)

Ball No.	Ball Name	In/Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
E1	MSC1_CLK_PC00	IO	PU	Enable	8mA	No		GPC[0]	MSC1_CLK			WKUP	VDDIO
F2	MSC1_CMD_PC01	IO	PU	Enable	8mA	No		GPC[1]	MSC1_CMD			WKUP	VDDIO
D1	MSC1_D0_PC02	IO	PU	Enable	8mA	No		GPC[2]	MSC1_D0			WKUP	VDDIO
E2	MSC1_D1_PC03	IO	PU	Enable	8mA	No		GPC[3]	MSC1_D1			WKUP	VDDIO
F3	MSC1_D2_PC04	IO	PU	Enable	8mA	No		GPC[4]	MSC1_D2			WKUP	VDDIO
E3	MSC1_D3_PC05	IO	PU	Enable	8mA	No		GPC[5]	MSC1_D3			WKUP	VDDIO
C1	PCM_CLK_PC06	IO	PU	Enable	8mA	No		GPC[6]	PCM_CLK			WKUP	VDDIO
B1	PCM_DO_PC07	IO	PU	Enable	8mA	No		GPC[7]	PCM_DO			WKUP	VDDIO
D2	PCM_DI_PC08	IO	PU	Enable	8mA	No		GPC[8]	PCM_DI			WKUP	VDDIO
C2	PCM_SYN_PC09	IO	PU	Enable	8mA	No		GPC[9]	PCM_SYN			WKUP	VDDIO
B6	UART0_RXD_PC10	IO	PU	Enable	8mA	No		GPC[10]	UART0_RXD			WKUP	VDDIO
A6	UART0_TXD_PC11	IO	PU	Enable	8mA	No		GPC[11]	UART0_TXD			WKUP	VDDIO
B5	UART0_CTS_PC12	IO	PU	Enable	8mA	No		GPC[12]	UART0_CTS			WKUP	VDDIO
A5	UART0_RTS_PC13	IO	PU	Enable	8mA	No		GPC[13]	UART0_RTS			WKUP	VDDIO
B2	PC16	IO	PU	Enable	8mA	Yes		GPC[16]				WKUP	VDDIO
A2	PC17	IO	PU	Enable	8mA	Yes		GPC[17]				WKUP	VDDIO
C3	PC18	IO	PU	Enable	8mA	Yes		GPC[18]				WKUP	VDDIO

B3	PC19	IO	PU	Enable	8mA	Yes		GPC[19]				WKUP	VDDIO
A3	PC20	IO	PU	Enable	8mA	Yes		GPC[20]				WKUP	VDDIO
E4	PC21	IO	PU	Enable	8mA	Yes		GPC[21]				WKUP	VDDIO
B4	PC22	IO	PU	Disable	8mA	Yes		GPC[22]				WKUP	VDDIO
A4	PC23	IO	PU	Disable	8mA	Yes		GPC[23]				WKUP	VDDIO
L1	PWM4_PC24	IO	PU	Enable	8mA	No		GPC[24]	PWM4			WKUP	VDDIO
K1	PWM0_PC25	IO	PD	Enable	8mA	No		GPC[25]	PWM0			WKUP	VDDIO
K2	I2C1_SCK_PWM1_PC26	IO	PU	Enable	8mA	No		GPC[26]	I2C1_SCK	PWM1		WKUP	VDDIO
J1	I2C1_SDA_PWM2_PC27	IO	PU	Enable	8mA	No		GPC[27]	I2C1_SDA	PWM2		WKUP	VDDIO

2.2.4 GPIO Group D

Table 2-4 GPIO Group D Pinmux(6)

Ball No.	Ball Name	In/ Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
P3	SSI0_CLK_I2C2_SCK_PD00	IO	PU	Enable	8mA	No	5V	GPD[0]	SSI0_CLK	I2C2_SCK		WKUP	VDDIO_5T
R1	SSI0_CE0_I2C2_SDA_PD01	IO	PU	Enable	8mA	No	5V	GPD[1]	SSI0_CE0	I2C2_SDA		WKUP	VDDIO_5T
P2	SSI0_DT_UART1_RXD_PD02	IO	PU	Enable	8mA	No	5V	GPD[2]	SSI0_DT	UART1_RXD		WKUP	VDDIO_5T
P1	SSI0_DR_UART1_TXD_PD03	IO	PU	Enable	8mA	No	5V	GPD[3]	SSI0_DR	UART1_TXD		WKUP	VDDIO_5T
N2	UART2_TXD_UART1_CTS_PD04	IO	PU	Enable	8mA	No	5V	GPD[4]	UART2_TXD	UART1_CTS		WKUP	VDDIO_5T
N1	UART2_RXD_UART1_RTS_PD05	IO	PU	Enable	8mA	No	5V	GPD[5]	UART2_RXD	UART1_RTS		WKUP	VDDIO_5T

2.3 X1000/E FUNCTION PIN DESCRIPTION

Table 2-5 X1000/E function pin description

Ball No.	Pin Names	IO	Power	Pin Description
Debug				
K3	pad_TRST_	I	VDDIO	JTAG reset
G1	TDO_UART2_TXD	O	VDDIO	JTAG serial data output
G2	TDI_UART2_RXD	I	VDDIO	JTAG serial data input
L3	TCK	I	VDDIO	JTAG clock
M3	TMS	I	VDDIO	JTAG mode select
Memory				
E6	LPDDR_VDD	P	-	Power for SIP LPDDR 1.8V
F6	LPDDR_VDD	P	-	Power for SIP LPDDR 1.8V
G6	LPDDR_VDD	P	-	Power for SIP LPDDR 1.8V
J7	LPDDR_VSS	P	-	Ground for SIP LPDDR
K7	LPDDR_VSS	P	-	Ground for SIP LPDDR
L7	LPDDR_VSS	P	-	Ground for SIP LPDDR
F5	LPDDR_VDDQ	P	-	Power for SIP LPDDR 1.8V
G5	LPDDR_VDDQ	P	-	Power for SIP LPDDR 1.8V
H5	LPDDR_VDDQ	P	-	Power for SIP LPDDR 1.8V
H6	LPDDR_VDDQ	P	-	Power for SIP LPDDR 1.8V
H7	LPDDR_VDDQ	P	-	Power for SIP LPDDR 1.8V
J5	LPDDR_VSSQ	P	-	Ground for SIP LPDDR
J6	LPDDR_VSSQ	P	-	Ground for SIP LPDDR
K5	LPDDR_VSSQ	P	-	Ground for SIP LPDDR

K6	LPDDR_VSSQ	P	-	Ground for SIP LPDDR
L6	LPDDR_VSSQ	P	-	Ground for SIP LPDDR
B9	ZQ			DDR PHY ZQ calibration resistor
A8	VREF0			DDR PHY VREF
Power and Ground				
E7	VDDMEM	P	-	IO digital power for DRAM 1.8V
E8	VDDMEM	P	-	IO digital power for DRAM 1.8V
F7	VDDMEM	P	-	IO digital power for DRAM 1.8V
F8	VDDMEM	P	-	IO digital power for DRAM 1.8V
G7	VDDMEM	P	-	IO digital power for DRAM 1.8V
G8	VDDMEM	P	-	IO digital power for DRAM 1.8V
E9	VSSMEM	P	-	IO digital ground for DRAM, 0V
E10	VSSMEM	P	-	IO digital ground for DRAM, 0V
F9	VSSMEM	P	-	IO digital ground for DRAM, 0V
F10	VSSMEM	P	-	IO digital ground for DRAM, 0V
G9	VSSMEM	P	-	IO digital ground for DRAM, 0V
G10	VSSMEM	P	-	IO digital ground for DRAM, 0V
K11	VDDIO	P	-	IO digital power for none DRAM 1.8~3.3V
K12	VDDIO	P	-	IO digital power for none DRAM 1.8~3.3V
L12	VDDIO	P	-	IO digital power for none DRAM 1.8~3.3V
N6	VDDIO_5T	P	-	IO digital power for none DRAM (5V tolerant)
J10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
K8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
K9	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
K10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
L8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V

L9	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
L10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
L11	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
M8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
M9	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
M10	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F11	VDD	P	-	CORE digital power, 1.2V
G11	VDD	P	-	CORE digital power, 1.2V
G12	VDD	P	-	CORE digital power, 1.2V
H10	VDD	P	-	CORE digital power, 1.2V
H11	VDD	P	-	CORE digital power, 1.2V
H12	VDD	P	-	CORE digital power, 1.2V
J11	VDD	P	-	CORE digital power, 1.2V
J12	VDD	P	-	CORE digital power, 1.2V
Audio Codec				
P16	CODEC_AVDD	S	-	Analog positive power supply
P14	CODEC_AVSS	S	-	Analog negative power supply 2 Ohms max
P15	CODEC_VREFP	S	-	Analog negative power supply for ADC part
T15	VCAP	AO	AVD	Decoupling cap for internal biasing voltage for core part
R16	AIP	AI	AVD	Left channel single-ended or positive analog input
R15	AIN	AI	AVD	Left channel negative analog input 1.Must be left floating in single-ended configuration
R14	MICBIAS	AO	AVD	Electric microphone biasing voltage
L16	VDDIO_CODEC	S	-	PWM digital line out IO positive power supply
M14	VSSIO_CODEC	S	-	PWM digital line out IO negative power supply
N15	CODEC_PWMLP	DO	VDDIO_CODEC	PWM digital line out positive left channel

N16	CODEC_PWMLN	DO	VDDIO_CODEC	PWM digital line out negative left channel
M15	COEDC_PWMRP	DO	VDDIO_CODEC	PWM digital line out positive right channel
M16	CODEC_PWMRN	DO	VDDIO_CODEC	PWM digital line out negative right channel
USB OTG				
R12	USB_DP0(OTG_DP)	AIO	AVDUSB33	USB OTG data plus
T12	USB_DM0(OTG_DM)	AIO	AVDUSB33	USB OTG data minus
P13	USB_VBUS(OTG_VBUS)	AIO	5V	USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin
P11	USB_ID(OTG_ID)	AI	AVDUSB25	USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDUSB25.
R13	OTG_TXR_RKL	AIO	AVDUSB25	Transmitter resister tune. It connects to an external resistor of 43.2Ω with 1% tolerance to analog ground, that adjusts the USB 2.0 high-speed source impedance
T14	AVDOTG	P	-	USB analog power.3.3V
R11	AVSOTG	P	-	USB analog ground.
T13	AVDOTG25	P	-	USB OTG analog power, 2.5V
EFUSE				
H2	AVDEFUSE	P	AVEFUSE	EFUSE programming power, 0V/2.5V
CPM				
T10	EXCLK_XI(EXCLK_I)	AI	VDDIO	OSC input.
R10	EXCLK_XO(EXCLK_O)	AO	VDDIO	OSC output.
T9	PLL_DVDD	P	-	PLL digital power, 1.2V
P9	PLL_DVSS	P	-	PLL digital ground
R9	PLL_AVDD	P	-	PLL analog power, 1.2V
P10	PLL_AVSS	P	-	PLL analog ground
RTC				
R8	RTCLK	AI	VDDRTC	OSC input or 32768Hz clock input
T8	XRTCLK	AO	-	OSC output

R7	PWRON	O	VDDRTC	Power on/off control of main power
P6	PPRST_	I	VDDRTC	RTC power on reset and RESET-KEY reset input
P7	TEST_TE	I	VDDRTC	Manufacture test enable, program readable
T7	LDOOUT	P	-	capacitor pin for RTC LDO need a 1nF decoupling capacitor to ground
N7	VSSRTC	P	-	RTC ground
T6	VDDRTC	P	-	VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down(normally you can use 1.8V instead to reduce power consumption)

2.4 X1000/E FUNCTION DESCRIPTION

Table 2-6 X1000/E Function Description

Signal Name	In/Out	Description
SLCD(Smart LCD)		
SLCD_D0	Output	Smart LCD data output bit 0
SLCD_D1	Output	Smart LCD data output bit 1
SLCD_D2	Output	Smart LCD data output bit 2
SLCD_D3	Output	Smart LCD data output bit 3
SLCD_D4	Output	Smart LCD data output bit 4
SLCD_D5	Output	Smart LCD data output bit 5
SLCD_D6	Output	Smart LCD data output bit 6
SLCD_D7	Output	Smart LCD data output bit 7
SLCD_D8	Output	Smart LCD data output bit 8
SLCD_D9	Output	Smart LCD data output bit 9
SLCD_D10	Output	Smart LCD data output bit 10
SLCD_D11	Output	Smart LCD data output bit 11

SLCD_D12	Output	Smart LCD data output bit 12
SLCD_D13	Output	Smart LCD data output bit 13
SLCD_D14	Output	Smart LCD data output bit 14
SLCD_D15	Output	Smart LCD data output bit 15
SLCD_RD	Output	Smart LCD read signal
SLCD_WR	Output	Smart LCD write signal
SLCD_CE	Output	Smart LCD chip select signal
SLCD_TE	Input	Smart LCD tearing effect signal
SLCD_DC	Output	Smart LCD data/command select signal
CIM(Camera Interface)		
CIM_PCLK	Input	CIM pixel clock input
CIM_HSYN	Input	CIM line horizonal sync input
CIM_VSYN	Input	CIM vertical sync input
CIM_MCLK	Output	CIM master clock output
CIM_D7	Input	CIM data input bit 7
CIM_D6	Input	CIM data input bit 6
CIM_D5	Input	CIM data input bit 5
CIM_D4	Input	CIM data input bit 4
CIM_D3	Input	CIM data input bit 3
CIM_D2	Input	CIM data input bit 2
CIM_D1	Input	CIM data input bit 1
CIM_D0	Input	CIM data input bit 0
I2S		
I2S_MCLK	Output	I2S master clock out
I2S_BCLK	Bidirection	I2S bit clock
I2S_LRCLK	Bidirection	I2S LR clock

I2S_DI	Input	I2S data input
I2S_DO	Output	I2S data output
PCM		
PCM_CLK	Bidirection	PCM clock
PCM_DO	Output	PCM data out
PCM_DI	Input	PCM data in
PCM_SYN	Bidirection	PCM sync
DMIC		
DMIC0_IN	Input	Digital MIC data input(Front/Back channel)
DMIC1_IN	Input	Digital MIC data input(Left/Right channel)
DMIC_CLK	Output	Digital MIC clock output
SFC		
SFC_CLK	Output	Serial Flash clock output
SFC_CE_	Output	Serial Flash chip enable
SFC_DR	Bidirection	Serial Flash data input
SFC_DT	Bidirection	Serial Flash data output
SFC_WP	Bidirection	Serial Flash write protect signal
SRC_HOLD	Bidirection	Serial Flash hold signal
PWM		
PWMn	Bidirection	PWM output or pulse input channel n
RTC		
RTC32K	Output	32768Hz clock output
I2C		
I2Cn_SCK	Bidirection	I2C n serial clock
I2Cn_SDA	Bidirection	I2C n serial data
SCC		

SCC_CLK	Bidirection	Smart Card clock
SCC_DATA	Bidirection	Smart Card data
SSI		
SSIn_CLK	Output	SSI n clock output
SSIn_CE0_	Output	SSI n chip enable 0
SSIn_CE1_	Output	SSI n chip enable 1
SSIn_GPC	Output	SSI n general-purpose control signal
SSIn_DT	Output	SSI n data output
SSIn_DR	Input	SSI n data input
UART		
UARTn_RXD	Input	UART n receiving data
UARTn_TXD	Output	UART n transmitting data
UARTn_CTS_	Input	UART Clear to send control
UARTn_RTS_	Output	UART Request to send control
MSC		
MSCn_D7	Bidirection	MSC(MMC/SD) n data bit 7
MSCn_D6	Bidirection	MSC(MMC/SD) n data bit 6
MSCn_D5	Bidirection	MSC(MMC/SD) n data bit 5
MSCn_D4	Bidirection	MSC(MMC/SD) n data bit 4
MSCn_D3	Bidirection	MSC(MMC/SD) n data bit 3
MSCn_D2	Bidirection	MSC(MMC/SD) n data bit 2
MSCn_D1	Bidirection	MSC(MMC/SD) n data bit 1
MSCn_D0	Bidirection	MSC(MMC/SD) n data bit 0
MSCn_CLK	Output	MSC(MMC/SD) n clock output
MSCn_CMD	Bidirection	MSC(MMC/SD) n command
USB 2.0 OTG		

DRV_VBUS	Output	USB OTG VBUS driver control signal
MAC		
MAC_PHY_CLK	Output	Ethernet PHY clock (50MHz)
MAC_CRS_DV	Input	Ethernet carrier sense
MAC_RXD1	Input	Ethernet receive data bit 1 for RMII
MAC_RXD0	Input	Ethernet receive data bit 0 for RMII
MAC_TXEN	Output	Ethernet transmit enable
MAC_TXD1	Output	Ethernet transmit data bit 1 for RMII
MAC_TXD0	Output	Ethernet transmit data bit 0 for RMII
MAC_MDC	Output	Ethernet management clock
MAC_MDIO	Bidirection	Ethernet management data
MAC_REF_CLK	Input	Ethernet reference clock (50MHz)

NOTES:

1 The meaning of phases in IO cell characteristics are:

a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.

b Output, Single-end: output and single-ended DDR IO are used.

c Output, Differential: output and differential signal DDR IO are used.

d Bi-dir, Differential: bi-direction and differential signal DDR IO are used.

e 4mA, 8mA, 16mA out: The IO cell's output driving strength is about 4mA,8mA,16mA.
4/8mA means the IO cell's output driving strength is selected and can be set as 4mA or 8mA.
2/4mA means the IO cell's output driving strength is selected and can be set as 2mA or 4mA.

f Pull-up: The IO cell contains a pull-up resistor.

g Pull-down: The IO cell contains a pull-down resistor.

h Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.

i Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.

j rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull

disabled

k Schmitt: The IO cell is Schmitt trig input.

l ~SL: The IO cell do not limited slew rate.

2 All GPIO shared pins are reset to GPIO input

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	85	°C
VDDMEM power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIO_5T power supplies voltage	-0.5	3.6	V
VDDIO_Codec power supplies voltage	-0.5	3.6	V
VDD core power supplies voltage	-0.2	1.32	V
PLLVDD12 power supplies voltage	-0.2	1.32	V
PLLAVDD power supplies voltage	-0.2	1.32	V
AVDEFUSE power supplies voltage	-0.5	2.75	V
VDDRTC power supplies voltage	-0.5	3.63	V
AVDUSB25 power supplies voltage	-0.5	2.75	V
AVDUSB33 power supplies voltage	-0.5	3.63	V
AVDCDC power supplies voltage	-0.5	3.63	V
Input voltage to VDDMEM supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDIO_5T supplied non-supply pins with 5V tolerance	-0.5	5.5	V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance	-0.5	3.6	V
Input voltage to VDDIO_Codec supplied non-supply pins	-0.5	3.6	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	3.6	V
Input voltage to AVDCDC supplied non-supply pins	-0.5	3.63	V
Input voltage to AVDUSB25 supplied non-supply pins	-0.5	2.75	V
Input voltage to AVDUSB33 supplied non-supply pins	-0.5	3.63	V
Output voltage from VDDMEM supplied non-supply pins	-0.5	1.98	V
Output voltage from VDDIO supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDIO_Codec supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDIO_5T supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDUSB25 supplied non-supply pins	-0.5	2.75	V
Output voltage from AVDUSB33 supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDCDC supplied non-supply pins	-0.5	3.63	V

Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDMEM voltage for LPDDR	1.65	1.8	1.95	V
	VDDMEM voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
	VDDMEM voltage for DDR3	1.425	1.5	1.575	V
	VDDMEM voltage for DDR3L	1.28	1.35	1.45	V
VIO(1.8V)	VDDIO voltage, use as 1.8V	1.62	1.8	1.98	V
VIO5(1.8V)	VDDIO_5T voltage, use as 1.8V	1.62	1.8	1.98	V
VIOC(1.8V)	VDDIO_Codec voltage, use as 1.8V	1.62	1.8	1.98	V
VIO(2.5V)	VDDIO voltage, use as 2.5V	2.25	2.5	2.75	V
VIO5(2.5V)	VDDIO_5T voltage, use as 2.5V	2.25	2.5	2.75	V
VIOC(2.5V)	VDDIO_Codec voltage, use as 2.5V	2.25	2.5	2.75	V
VIO(3.3V)	VDDIO voltage, use as 3.3V	2.97	3.3	3.63	V
VIO5(3.3V)	VDDIO_5T voltage, use as 3.3V	2.97	3.3	3.63	V
VIOC(3.3V)	VDDIO_Codec voltage, use as 3.3V	2.97	3.3	3.63	V
VCORE	VDD core voltage	1.08	1.2	1.32	V
VPLL12	PLLVDD, PLLAVDD voltage	1.08	1.2	1.32	V
VEFUSE	AVDEFUSE voltage	2.25	2.5	2.75	V
VRTC33	VDDRTC voltage	1.8	1.8	3.63	V
VUSB25	AVDOTG25 voltage	2.25	2.5	2.75	V
VUSB33	AVDOTG voltage	3.0	3.3	3.6	V
VCDC	CODEC_AVDD voltage	2.97	3.3	3.63	V

Table 3-3 Recommended operating conditions for VDDMEM supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
VI18	Input voltage for LPDDR applications	0	1.8	1.9	V
VO18	Output voltage for LPDDR applications	0	1.8	1.9	V

Table 3-4 Recommended operating conditions for VDDIO/VDDIO_5T/VDDIO_Codec/VDDRTC supplied pins

Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Unit**
VIH18	Input high voltage for 1.8V I/O application	1.17	1.8	3.6	V
VIL18	Input low voltage for 1.8V I/O application	–0.3	0	0.63	V

VIH25	Input high voltage for 2.5V I/O application	1.7	2.5	3.6	V
VIL25	Input low voltage for 2.5V I/O application	–0.3	0	0.7	V
VIH33	Input high voltage for 3.3V I/O application	2	3.3	3.6	V
VIL33	Input low voltage for 3.3V I/O application	–0.3	0	0.8	V

Table 3-5 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
TA	Ambient temperature	–40		85	℃

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-6 DC characteristics for V_{REFMEM}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.5	0.51	VMEM

Table 3-7 DC characteristics for VDDmem supplied pins in LPDDR application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	Input logic threshold High	0.7* VMEM		VMEM+0.3	V
$V_{IL(DC)}$	Input logic threshold Low	VMEM-0.3		0.3* VMEM	V
VIH(AC)	AC Input logic High	0.8* VMEM		VMEM+0.3	V
VIL(AC)	AC Input logic Low	VMEM-0.3		0.2* VMEM	V
VOH	DC output logic High (IOH=-0.1mA)	0.9*VMEM			V
VOL	DC output logic Low (IOL=0.1mA)			0.1 *VMEM	V
ILL	Input leakage current		0.01	6.45	uA
IMEM	VMEM quiescent current		0.02	15.03	uA

Table 3-8 DC characteristics for VDDIO/VDDIO_5T/VDDIO_Codec/VDDRTC supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.79	0.86	0.94	V
V_{T+}	Schmitt trig low to high threshold point	0.95	1.06	1.16	V

V_{T-}	Schmitt trig high to low threshold point		0.58	0.69	0.79	V
V_{TPU}	Threshold point with pull-up resistor enabled		0.79	0.86	0.94	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.79	0.86	0.94	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.95	1.06	1.16	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.58	0.68	0.78	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.96	1.07	1.17	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.59	0.69	0.79	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		66	114	211	kΩ
R_{PD}	Pull-down Resistor		58	103	204	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	5.3	9.8	15.8	mA
		16mA	10.8	19.7	31.8	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	3.3	8.3	16.6	mA
		16mA	6.6	16.5	33.2	mA

Table 3-9 DC characteristics for VDDIO/VDDIO_5T/VDDIO_Codec/VDDRTC supplied pins for 2.5V application

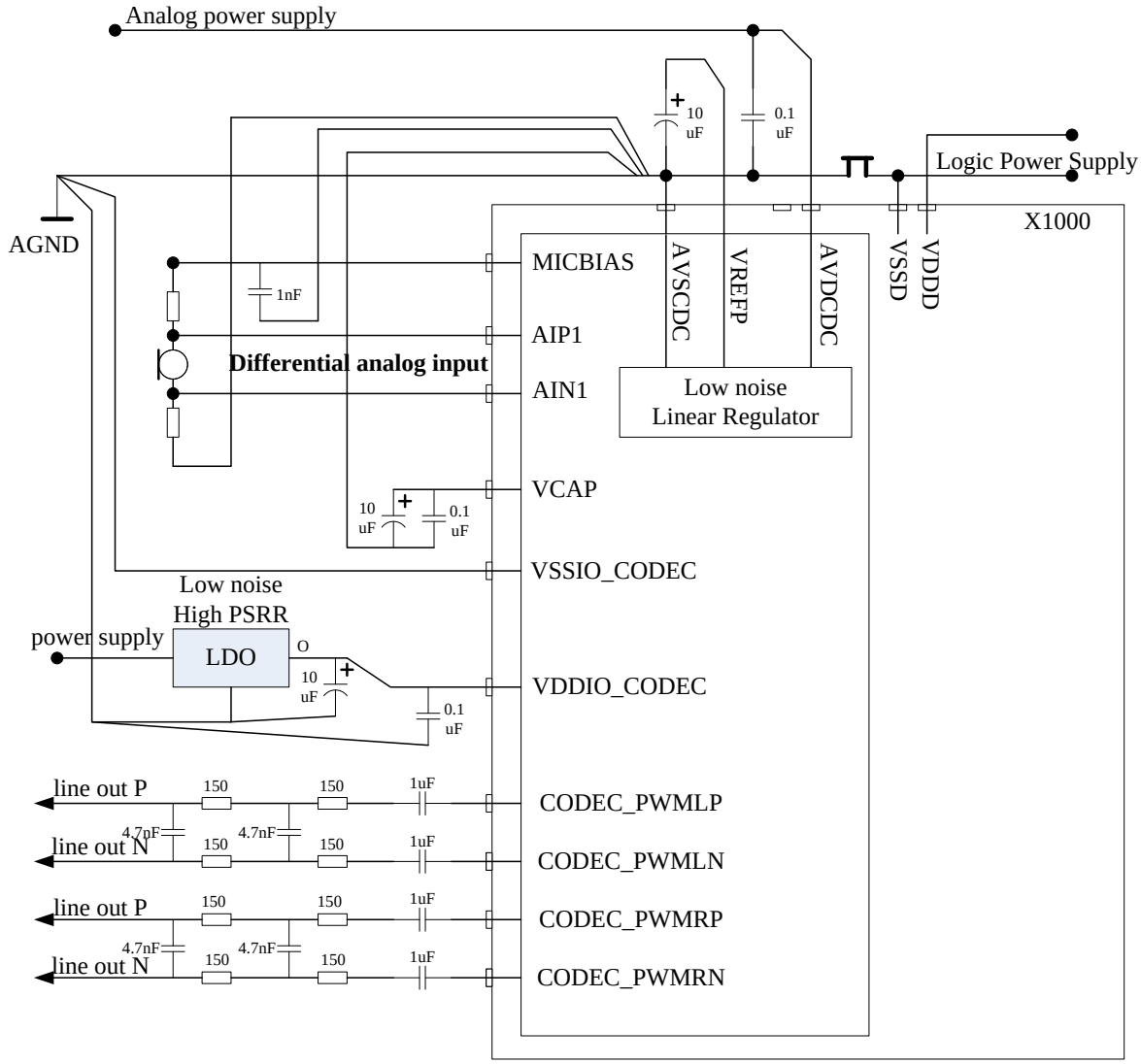
Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.06	1.17	1.27	V
V_{T+}	Schmitt trig low to high threshold point	1.27	1.40	1.50	V
V_{T-}	Schmitt trig high to low threshold point	0.86	0.98	1.09	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.05	1.16	1.25	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.06	1.17	1.27	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.27	1.39	1.48	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.85	0.97	1.08	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.27	1.41	1.50	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.88	0.99	1.10	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA
R_{PU}	Pull-up Resistor	43	69	120	kΩ

R_{PD}	Pull-down Resistor		41	66	124	kΩ
V_{OL}	Output low voltage				0.7	V
V_{OH}	Output high voltage		1.7			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	11.6	19.4	28.4	mA
		16mA	23.3	39.1	57.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	9.3	19.4	34.6	mA
		16mA	18.6	38.7	69.2	mA

Table 3-10 DC characteristics for VDDIO/VDDIO_5T/VDDIO_Codec/VDDRTC supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.39	1.50	1.65	V
V_{T+}	Schmitt trig low to high threshold point		1.62	1.75	1.90	V
V_{T-}	Schmitt trig high to low threshold point		1.18	1.29	1.44	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.36	1.48	1.64	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.40	1.52	1.66	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.62	1.75	1.89	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.16	1.28	1.43	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.64	1.77	1.91	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.19	1.31	1.45	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		34	51	81	kΩ
R_{PD}	Pull-down Resistor		35	51	88	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	10.0	15.2	20.2	mA
		16mA	20.2	30.6	40.6	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	13.9	28.0	48.2	mA
		16mA	27.8	56.0	96.3	mA

3.4 Audio codec



Note: 1. The single-ended/differential input port AIP1/AIN1 can be configure to microphone input or line input by software.

2. VCAP/AVDCDC each of them requires connecting decoupling capacitors (0.1uF) between the pads VCAP/AVDCDC and AVSCDC. This ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch).

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X1000/E processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1shows this sequence and Table 3-11 gives the timing parameters. Following are the name of the power.

- VDDRTC: VDDRTC
- AVDAUD: AVDCDC

- VDD: all 1.2V power supplies, include VDDCORE, PLLVDD12, PLLAVDD
- VDDIO: all other digital IO, include DDR power supplies: VDDMEM, VDDIO, VDDIO_5T, VDDIO_Codec
- AVD: all other analog power supplies: AVDUSB25, AVDUSB33
- AVDEFUSE

Table 3-11 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDDIO}	VDDIO rise time[1]	0	5	ms
t_{D_VDDIO}	Delay between VDD arriving 50% (or 90%) to VDDIO arriving 50% (or 90%)	0	–	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD arriving 50% (or 90%)	0	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between AVDAUD arriving 90% to VDD arriving 90%	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVD}	Delay between VDDIO arriving 90% to AVD arriving 90%	0	1	ms
$t_{D\_PPRST\_}$	Delay between AVD stable and PPRST_ de-asserted	TBD[3]	–	ms[2]
$t_{D\_AVDEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

1 The power rise time is defined as 10% to 90%.

2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

3 It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.

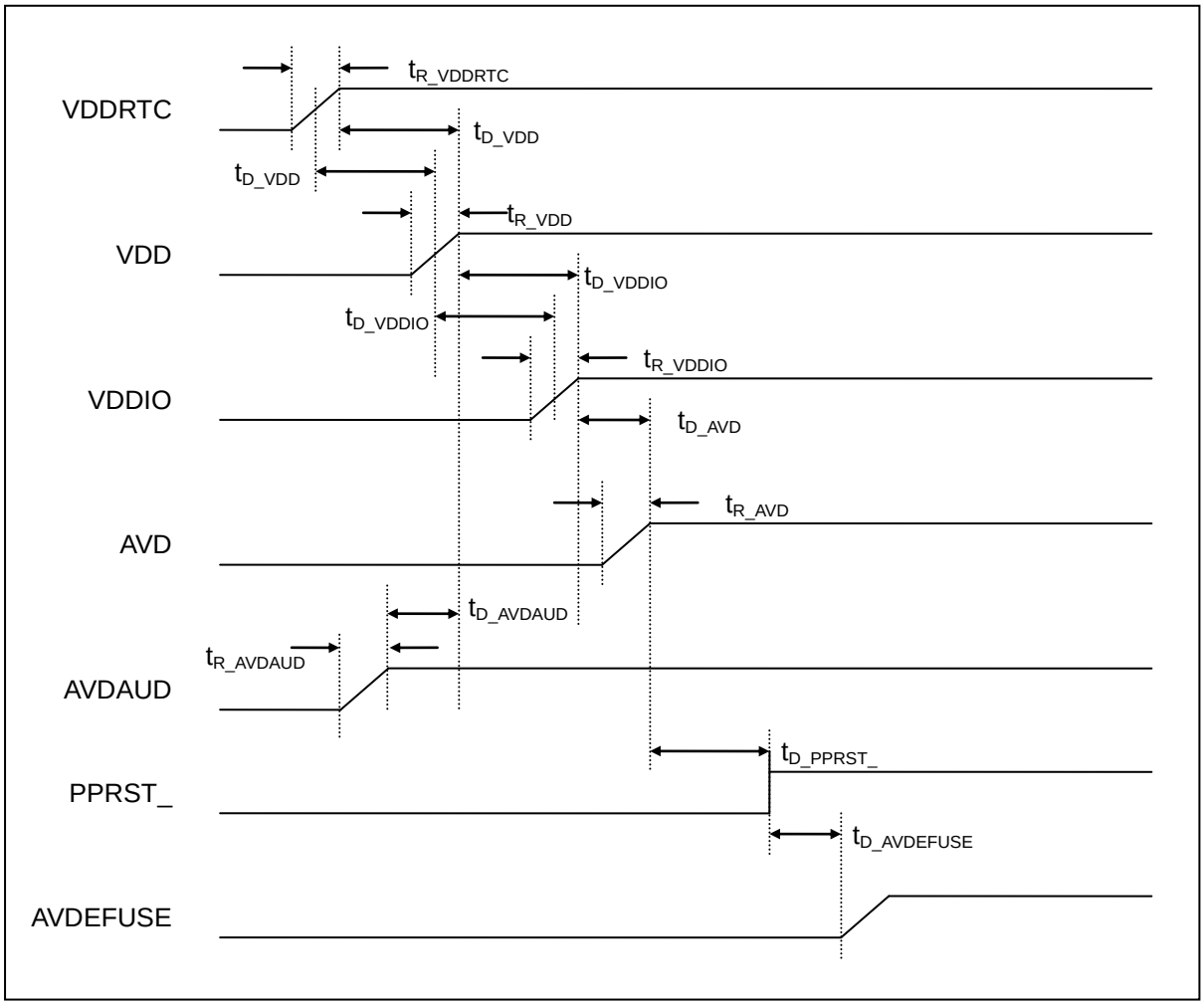


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5 Pin Descriptions” for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY, the audio CODEC DAC/ADC put in suspend mode.

3.5.3 BOOT

The boot sequence of the X1000/E is controlled by boot_sel [2:0] pin values. The following table lists them:

Table 3-12 Boot Configuration of X1000/E

boot_sel[2]	boot_sel[1]	boot_sel[0]	Boot configuration
1	X	X	EXTCLK is 26MHz
0	X	X	EXTCLK is 24MHz
X	1	1	Boot from SFC0
X	0	1	Boot from MSC0
X	1	0	Boot from USB 2.0 device

X: means "Don't Care"

The boot procedure is showed in the following flow chart:

After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[2:0] to determine the boot method.

2 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 12KB code from MMC/SD card to tcsm and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/128 is used initially. When reading data, the clock EXTCLK/4 is used.

3 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in tcsm. Then branch to this area in tcsm.

4 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE,SFC_DR,SFC_DT, SFC_WP, SFC_HOLD are initialized, the boot program loads the 12KB code from MMC/SD card to tcsm and jump to it.

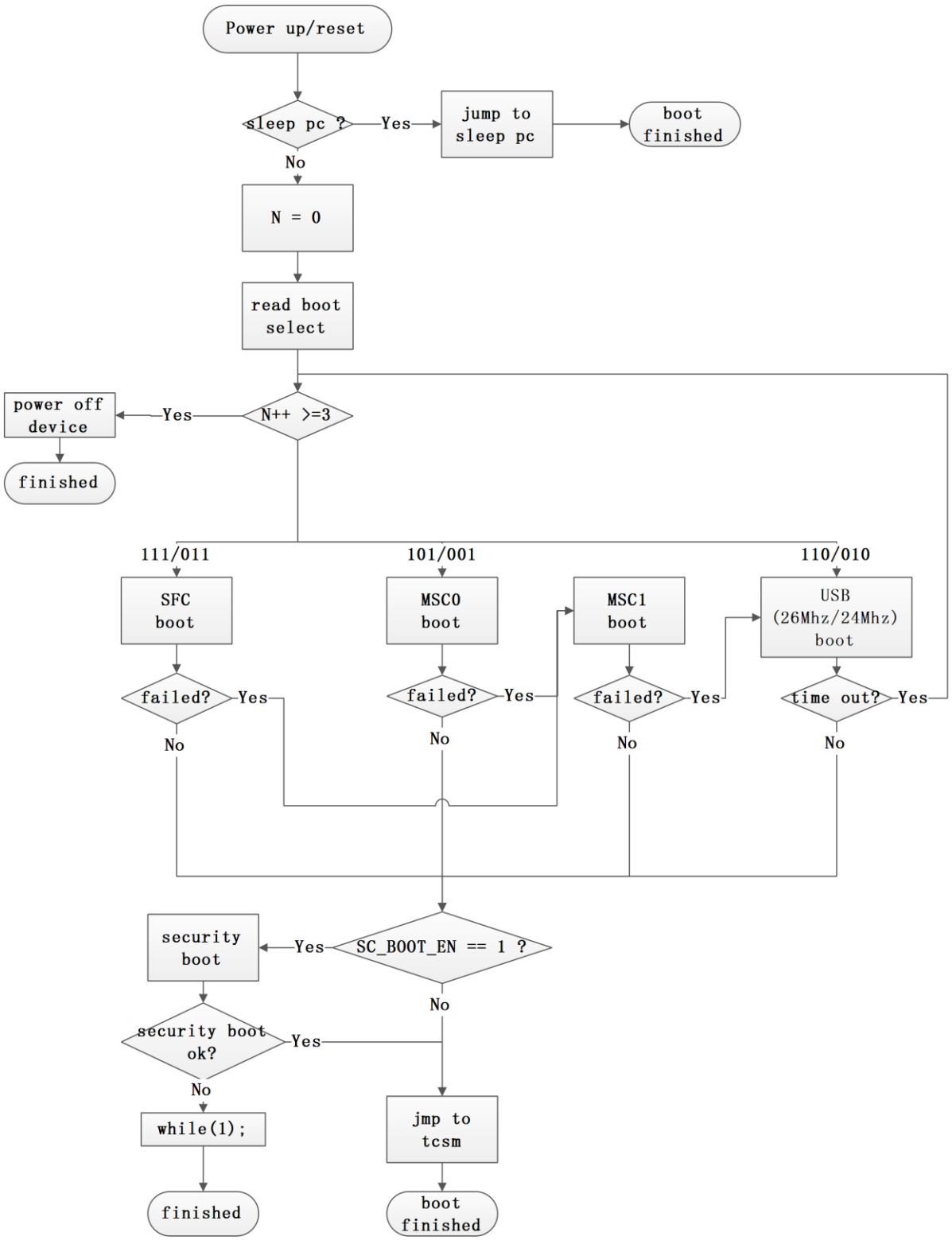


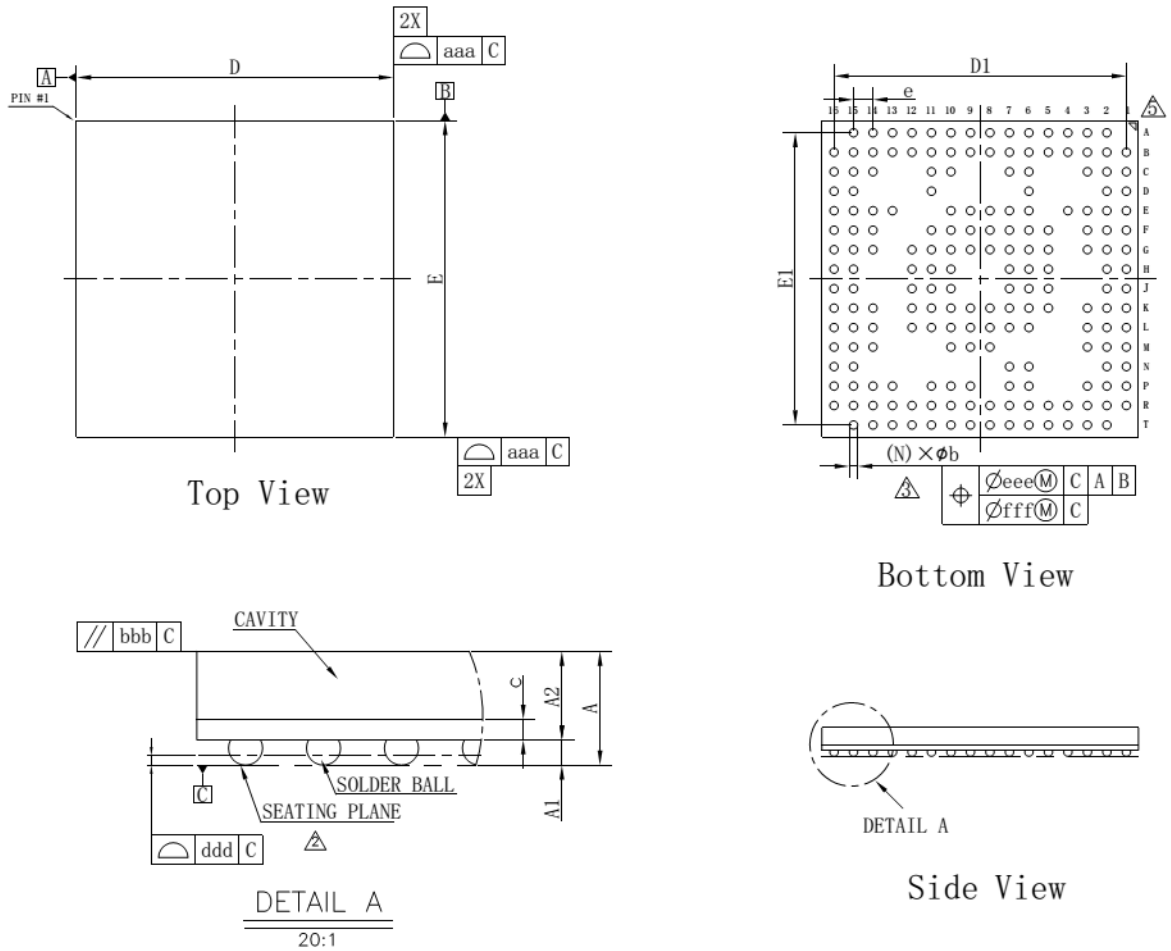
Figure 3-2 Boot flow diagram of X1000/E

4 Packaging Information

4.1 Overview

X1000/E processor is offered in 190-pin BGA package, which is 13mm x 13mm x 1.2mm outline, 16 x 16 matrix ball grid array and 0.8mm ball pitch, show in Figure 4-1.

4.2 X1000/E Device Dimensions



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.270	—	—	0.050
A1	0.210	0.260	0.310	0.008	0.010	0.012
A2	0.860	0.910	0.960	0.034	0.036	0.038
c	0.170	0.210	0.250	0.007	0.008	0.010
D	12.900	13.000	13.100	0.508	0.512	0.516
E	12.900	13.000	13.100	0.508	0.512	0.516
D1	—	12.000	—	—	0.472	—
E1	—	12.000	—	—	0.472	—
e	—	0.800	—	—	0.031	—
b	0.300	0.350	0.400	0.012	0.014	0.016
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.100			0.004		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.350			0.014		
N	190			190		
MD/ME	16/16			16/16		

Figure 4-1 X1000/E package outline drawing

Notes:

1. BALL PAD OPENING: 0.315mm；
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS；
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,PARALLEL TO PRIMARY DATUM C；
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd；
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY；
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING；
7. ALL UNITS ARE IN MILLIMETER；

4.3 Solder Ball Materials

Both the top (joint) and bottom solder ball materials of X1000/E are SAC105.

4.4 Moisture Sensitivity Level

X1000/E package moisture sensitivity is level 3.

5 PCB Mounting Guidelines

5.1 RoHS compliance

TBD.

5.2 Reflow profile

X1000/E package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.