# 1Gb LPDDR2 Specification

## Specifications

- **Density**: 1G bits
- **Organization**
  - 8 banks x 8M words x 16 bits
- **Power supply**
  - $V_{DD1}$=1.7 to 1.95V
  - $V_{DD2}$,$V_{DDQ}$=1.14 to 1.3V
- **Clock frequency**
  - 533/466/400/333/266/200/166Mhz (max.)
- **2KB page size**
  - Row address: AX0 to AX12
  - Column address: AY0 to AY9 (x16 bits)
- **8 internal banks** for concurrent operation
- **Interface**: HSUL_12
- **Burst lengths (BL)**: 4, 8, 16
- **Burst type (BT)**
  - Sequential (4, 8, 16)
  - Interleave (4, 8)
- **Read latency (RL)**: 3, 4, 5, 6**,** 7, 8
- **Write latency (WL)**: 1, 2, 3, 4
- **Precharge**: auto precharge option for each burst access
- **Programmable driver strength**
- **Refresh**: auto-refresh, self-refresh
- **Average refresh period**:
  - 7.8uS @ ≤ 85°C
  - 3.9uS @ > 85°C and ≤ 95°C
  - 1.95uS @ > 95°C and ≤ 105°C
- **Operating temperature range**
  - TC = -25°C to +85°C
  - TC = -40°C to +105°C (extended range)

## Features

- DLL is not implemented
- Low power consumption
- JEDEC LPDDR2-S4B compliance
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Deep power-down mode
- Double-data-rate architecture; two data transfers per one clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Differential clock inputs (CK and /CK)
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data

# Differences from JEDEC:

Mode Register 9, bit [5] is a readable Failed Die Bit

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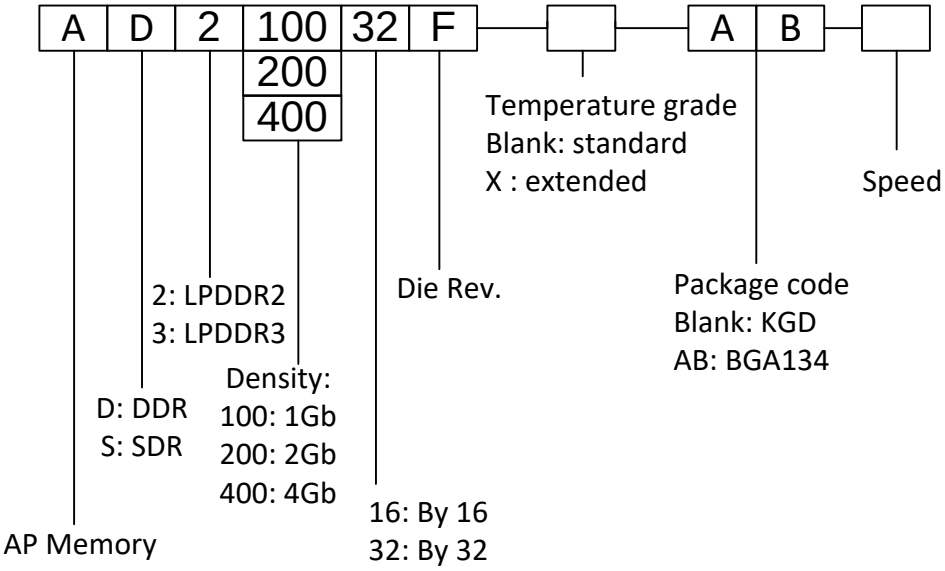
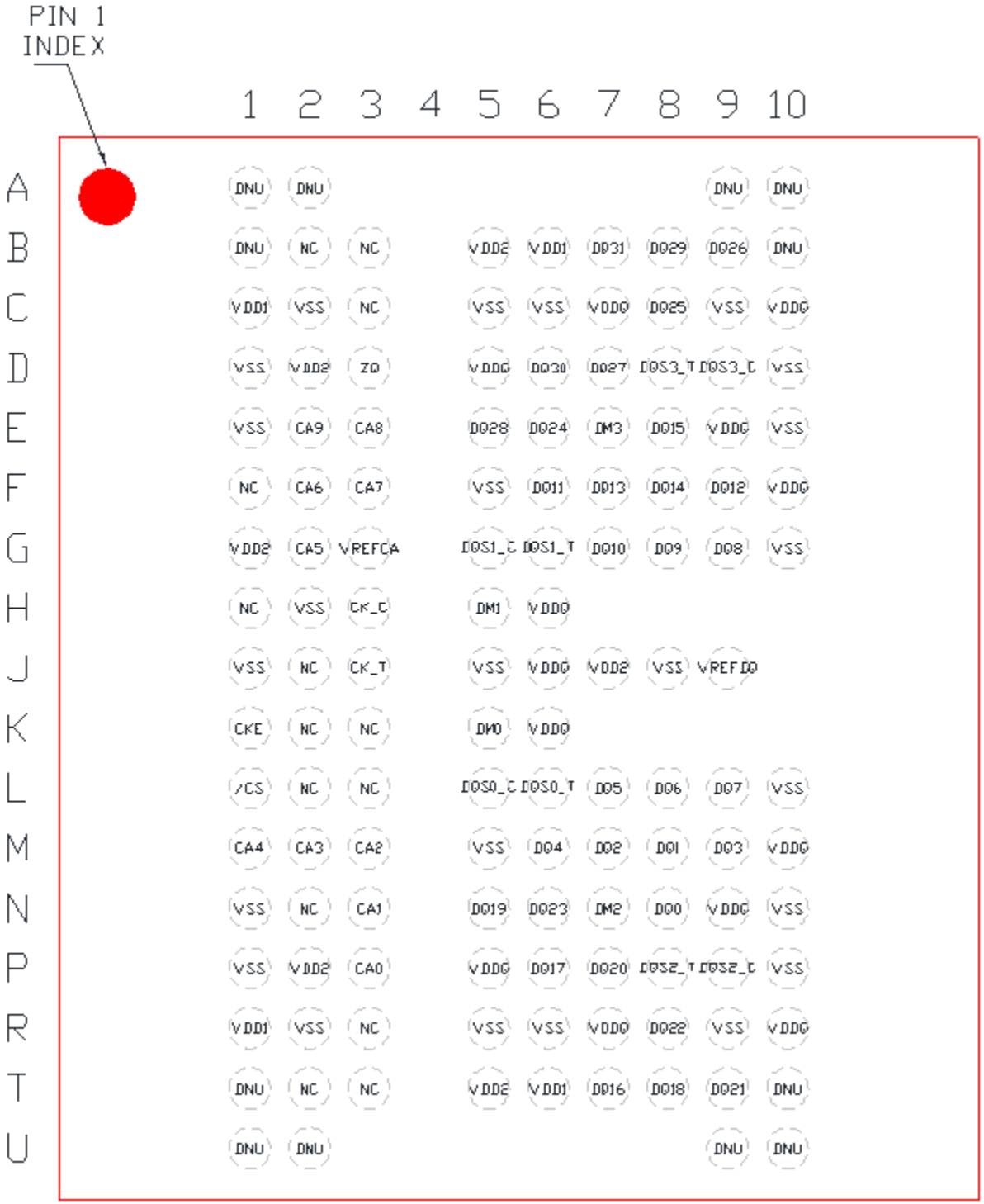
# 1 Ordering Information:

| *Part Number* | *Configuration* | *Temperature Range* | *Max Frequency* | *Note* |
|---|---|---|---|---|
| AD210032F | X32 | -25°C to +85°C | 533 MHz | Bare die |
| AD210016F | X16 | -25°C to +85°C | 533 MHz | Bare die |
| AD210032F-X | X32 | -40°C to +105°C | 533 MHz | Bare die |
| AD210016F-X | X16 | -40°C to +105°C | 533 MHz | Bare die |
| AD210032F-AB | X32 | -25°C to +85°C | 466 MHz | Package |
| AD210016F-AB | X16 | -25°C to +85°C | 466 MHz | Package |
| AD210032F-X-AB | X32 | -40°C to +105°C | 466 MHz | Package |
| AD210016F-X-AB | X16 | -40°C to +105°C | 466 MHz | Package |



## 2 Package Ball Assignment

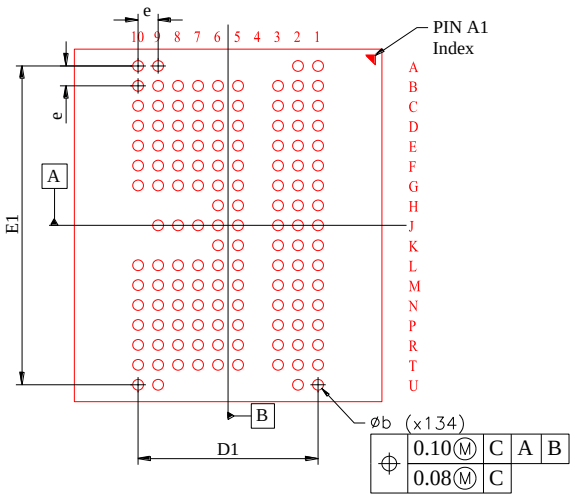
***x32/x16: "134-Ball FBGA –10x11.5x1.0 mm, ball pitch 0.65 mm, ball size 0.4 mm. (package code AB)"***



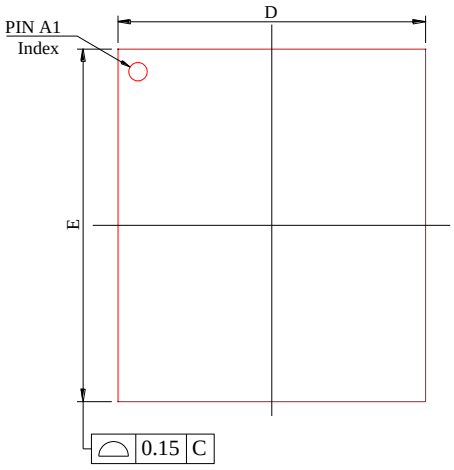

Top View

Package Outline Drawing

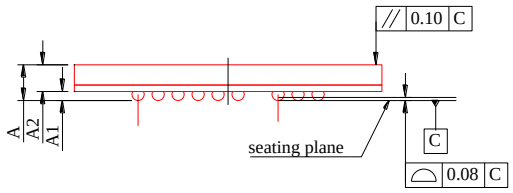
***x32/x16: "134-Ball FBGA –10x11.5x1.0 mm, ball pitch 0.65 mm, ball size 0.4 mm. (package code AB)"***




Bottom View




Top View




Side View

| Symbol | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.00 |
| A1 | 0.27 | 0.32 | 0.37 |
| A2 | 0.545 | 0.58 | 0.63 |
| D | 9.90 | 10.00 | 10.10 |
| D1 | 5.85 BSC | | |
| E | 11.40 | 11.50 | 11.60 |
| E1 | 10.40 BSC | | |
| b | 0.35 | 0.40 | 0.45 |
| e | 0.65 BSC | | |

# 3 Electrical Specifications:

All voltages are referenced to each GND level (VSS, VSSCA, and VSSQ).
Execute power-up and Initialization sequence before proper device operation can be achieved.

## *3.1 Absolute Maximum Ratings*

| *Parameter* | *Symbol* | *Rating* | *Unit* | *Notes* |
|---|---|---|---|---|
| Voltage on any pin relative to $V_{SSCA}$, $V_{SSQ}$ | VT | -0.4 to +1.6 | V | |
| Power supply voltage (core power1) relative to $V_{SS}$ | $V_{DD1}$ | -0.4 to +2.3 | V | |
| Power supply voltage (core power2) relative to $V_{SS}$ | $V_{DD2}$ | -0.4 to +1.6 | V | |
| Power supply voltage for output relative to $V_{SSQ}$ | $V_{DDQ}$ | -0.4 to +1.6 | V | |
| Storage temperature | $T_{STG}$ | -55 to +125 | °C | 1 |

Notes:
Storage temperature the case surface temperature on the center/top side of the DRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

## *3.2 Operating Temperature Condition*

| *Temperature Range* | *Symbol* | *Rating* | *Unit* | *Notes* |
|---|---|---|---|---|
| Normal | TC | -25 to +85 | °C | 1 |
| Extended | | -40 to +105 | °C | 2 |

Notes:
Operating temperature is the case surface temperature on the center/top side of the DRAM.
Refer to MR4 programming table for Temperature Sensor de-rating & refresh rate numbers.

### 3.3 Recommended DC Operating Conditions

| Parameter | | Symbol | min. | typical | max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply voltage | Core Power1 | $V_{DD1}$ | 1.7 | 1.8 | 1.95 | V | 1 |
| | | $V_{SS}$ | 0 | 0 | 0 | V | |
| | Core Power2 | $V_{DD2}$ | 1.14 | 1.2 | 1.3 | V | 1 |
| | | $V_{SS}$ | 0 | 0 | 0 | V | |
| | I/O Buffer Power | $V_{DDQ}$ | 1.14 | 1.2 | 1.3 | V | 1 |
| | | $V_{SSQ}$ | 0 | 0 | 0 | V | |

Notes:
$V_{DDQ}$ tracks with $V_{DD2}$. AC parameters are measured with $V_{DD2}$ and $V_{DDQ}$ tied together.

### 3.4 AC and DC Input Measurement Levels

[Refer to section 8 in JEDEC Standard No. 209-2E]

### 3.5 DC Characteristics 1

| Parameter | Test Condition | Symbol | Power Supply | Max | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | DDR 1066 | DDR 933 | DDR 800 | DDR 667 | DDR 533 | DDR 400 | DDR 333 | |
| Operating one bank active-precharge current | $t_{CK} = t_{CK(min)}$; $t_{RC} = t_{RC(min)}$; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE | $I_{DD01}$ | $V_{DD1}$ | 14 | | | | | | | mA |
| | | $I_{DD02}$ | $V_{DD2}$ | 70 | | | | | | | mA |
| | | $I_{DD0IN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Idle power-down standby current | $t_{CK} = t_{CK(min)}$; CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE | $I_{DD2P1}$ | $V_{DD1}$ | 0.8 | | | | | | | mA |
| | | $I_{DD2P2}$ | $V_{DD2}$ | 1.4 | | | | | | | mA |
| | | $I_{DD2PIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Idle power-down standby current with clock stop | CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bust inputs are STABLE; | $I_{DD2PS1}$ | $V_{DD1}$ | 0.8 | | | | | | | mA |
| | | $I_{DD2PS2}$ | $V_{DD2}$ | 1.4 | | | | | | | mA |
| | | $I_{DD2PSIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Idle non power-down standby current | $t_{CK} = t_{CK(min)}$; CKE is HIGH; CS_n is HIGH, all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE | $I_{DD2N1}$ | $V_{DD1}$ | 0.8 | | | | | | | mA |
| | | $I_{DD2N2}$ | $V_{DD2}$ | 25 | | | | | | | mA |
| | | $I_{DD2NIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Idle non power-down standby current with clock stop | CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE | $I_{DD2NS1}$ | $V_{DD1}$ | 0.8 | | | | | | | mA |
| | | $I_{DD2NS2}$ | $V_{DD2}$ | 17 | | | | | | | mA |
| | | $I_{DD2NSIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Active power-down standby current | $t_{CK} = t_{CK(min)}$; CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE | $I_{DD3P1}$ | $V_{DD1}$ | 1.5 | | | | | | | mA |
| | | $I_{DD3P2}$ | $V_{DD2}$ | 8 | | | | | | | mA |
| | | $I_{DD3PIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Active power-down standby current with clock stop | CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are STABLE; Data bus inputs are STABLE | $I_{DD3PS1}$ | $V_{DD1}$ | 1.5 | | | | | | | mA |
| | | $I_{DD3PS2}$ | $V_{DD2}$ | 8 | | | | | | | mA |
| | | $I_{DD3PSIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Active non power-down standby current | $t_{CK} = t_{CK(min)}$; CKE is HIGH; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE | $I_{DD3N1}$ | $V_{DD1}$ | 1.5 | | | | | | | mA |
| | | $I_{DD3N2}$ | $V_{DD2}$ | 30 | | | | | | | mA |
| | | $I_{DD3NIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Active non power-down standby current with clock stop | CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE | $I_{DD3NS1}$ | $V_{DD1}$ | 1.5 | | | | | | | mA |
| | | $I_{DD3NS2}$ | $V_{DD2}$ | 20 | | | | | | | mA |
| | | $I_{DD3NSIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |

| Parameter | Test Condition | Symbol | Power Supply | Max DDR 1066 | Max DDR 933 | Max DDR 800 | Max DDR 667 | Max DDR 533 | Max DDR 400 | Max DDR 333 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Operating burst read current | $t_{CK} = t_{CK(min)}$; CS_n is HIGH between valid commands; one bank active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer | $I_{DD4R1}$ | $V_{DD1}$ | 24 | 21 | 18 | 15.5 | 12.5 | 9.5 | 8 | mA |
| | | $I_{DD4R2}$ | $V_{DD2}$ | 180 | 175 | 165 | 150 | 130 | 100 | 90 | mA |
| Operating burst write current | $t_{CK} = t_{CK(min)}$; CS_n is HIGH between valid commands; one bank active; BL = 4; WL = WL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer | $I_{DD4W1}$ | $V_{DD1}$ | 24 | 21 | 18 | 15.5 | 12.5 | 9.5 | 8 | mA |
| | | $I_{DD4W2}$ | $V_{DD2}$ | 210 | 195 | 175 | 150 | 125 | 105 | 90 | mA |
| | | $I_{DD4WIN}$ | $V_{DDQ}$ | 35 | | | | | | | mA |
| All Bank Auto Refresh Burst Current | $t_{CK} = t_{CK(min)}$; CS_n is HIGH between valid commands; $t_{RC} = t_{RFCab(min)}$; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE | $I_{DD51}$ | $V_{DD1}$ | 32 | | | | | | | mA |
| | | $I_{DD52}$ | $V_{DD2}$ | 160 | | | | | | | mA |
| | | $I_{DD5IN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| All Bank Auto Refresh Average Current | $t_{CK} = t_{CK(min)}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are SWITCHING; Data bus inputsa are STABLE | $I_{DD5ab1}$ | $V_{DD1}$ | 2 | | | | | | | mA |
| | | $I_{DD5ab2}$ | $V_{DD2}$ | 45 | | | | | | | mA |
| | | $I_{DD5abIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Per Bank Auto Refresh Average Current | $t_{CK} = t_{CK(min)}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI/8}$; CA bus inputs are SWITCHING; Data bus inputs are STABLE | $I_{DD5pb1}$ | $V_{DD1}$ | 3 | | | | | | | mA |
| | | $I_{DD5pb2}$ | $V_{DD2}$ | 27 | | | | | | | mA |
| | | $I_{DD5pbIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Self Refresh Current (Standard Temerature Range: -30˚C to 85˚C) | CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-refresh rate | $I_{DD61}$ | $V_{DD1}$ | 1 | | | | | | | mA |
| | | $I_{DD62}$ | $V_{DD2}$ | 1.6 | | | | | | | mA |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 0.3 | | | | | | | mA |
| Deep Power Down Current (Standard Temerature Range: -30˚C to 85˚C) | CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE | $I_{DD81}$ | $V_{DD1}$ | 0.2 | | | | | | | mA |
| | | $I_{DD82}$ | $V_{DD2}$ | 0.6 | | | | | | | mA |
| | | $I_{DD8IN}$ | $V_{DDQ}$ | 0.3 | | | | | | | mA |
| Self Refresh Current (Extended Temerature Range: 85˚C to 105˚C) | CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE Maximum 4x Self-refresh rate | $I_{DD6ET1}$ | $V_{DD1}$ | 2 | | | | | | | mA |
| | | $I_{DD6ET2}$ | $V_{DD2}$ | 4 | | | | | | | mA |
| | | $I_{DD6ETIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |
| Deep Power Down Current (Extended Temerature Range: 85˚C to 105˚C) | CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE | $I_{DD8ET1}$ | $V_{DD1}$ | 0.4 | | | | | | | mA |
| | | $I_{DD8ET2}$ | $V_{DD2}$ | 1 | | | | | | | mA |
| | | $I_{DD8ETIN}$ | $V_{DDQ}$ | 1 | | | | | | | mA |

### 3.6 Advanced Data Retention Current (Self-refresh current)

| Parameter | | Symbol | supply | Typical | Unit | Test Condition |
|---|---|---|---|---|---|---|
| +25°C CKE ≤ 0.2V | Full Array | $I_{DD61}$ | $V_{DD1}$ | 88 | µA | All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE |
| | | $I_{DD62}$ | $V_{DD2}$ | 180 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 6 | µA | |
| | 1/2 Array | $I_{DD61}$ | $V_{DD1}$ | 76 | µA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 133 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 6 | µA | |
| | 1/4 Array | $I_{DD61}$ | $V_{DD1}$ | 65 | µA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 95 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 6 | µA | |
| | 1/8 Array | $I_{DD61}$ | $V_{DD1}$ | 59 | µA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 74 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 6 | µA | |
| +45°C CKE ≤ 0.2V | Full Array | $I_{DD61}$ | $V_{DD1}$ | 126 | µA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 282 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 12 | µA | |
| | 1/2 Array | $I_{DD61}$ | $V_{DD1}$ | 99 | µA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 182 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 12 | µA | |
| | 1/4 Array | $I_{DD61}$ | $V_{DD1}$ | 85 | µA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 132 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 12 | µA | |
| | 1/8 Array | $I_{DD61}$ | $V_{DD1}$ | 79 | µA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 106 | µA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 12 | µA | |

| Parameter | | Symbol | supply | max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| +45°C ≤ TC ≤ +85°C CKE ≤ 0.2V | Full Array | $I_{DD61}$ | $V_{DD1}$ | 1 | mA | All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE |
| | | $I_{DD62}$ | $V_{DD2}$ | 1.6 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 0.3 | mA | |
| | 1/2 Array | $I_{DD61}$ | $V_{DD1}$ | 0.8 | mA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 1.2 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 0.3 | mA | |
| | 1/4 Array | $I_{DD61}$ | $V_{DD1}$ | 0.7 | mA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 1 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 0.3 | mA | |
| | 1/8 Array | $I_{DD61}$ | $V_{DD1}$ | 0.65 | mA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 0.9 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 0.3 | mA | |
| +85°C ≤ TC ≤ +105°C CKE ≤ 0.2V | Full Array | $I_{DD61}$ | $V_{DD1}$ | 2 | mA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 4 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 1 | mA | |
| | 1/2 Array | $I_{DD61}$ | $V_{DD1}$ | 1.6 | mA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 2.7 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 1 | mA | |
| | 1/4 Array | $I_{DD61}$ | $V_{DD1}$ | 1.4 | mA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 1.7 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 1 | mA | |
| | 1/8 Array | $I_{DD61}$ | $V_{DD1}$ | 1.3 | mA | |
| | | $I_{DD62}$ | $V_{DD2}$ | 1.4 | mA | |
| | | $I_{DD6IN}$ | $V_{DDQ}$ | 1 | mA | |

Notes:
This device supports bank-masking.
$I_{DD6}$ 85°C/105°C are the maximum and $I_{DD6}$ 25°C/45°C are typical of the distribution of the arithmetic mean.

### 3.7 DC Characteristics 2

| Parameter | Symbol | min. | max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | -2.0 | 2.0 | µA | $0 \le V_{IN} \le V_{DDQ}$ | |
| Output leakage current | $I_{LO}$ | -1.5 | 1.5 | µA | $0 \le V_{OUT} \le V_{DDQ}$<br>DQ = disable | |
| Output high voltage | $V_{OH}$ | $0.9 \times V_{DDQ}$ | -- | V | $I_{OH}$ = -0.1mA | |
| Output low voltage | $V_{OL}$ | -- | $0.1 \times V_{DDQ}$ | V | $I_{OL}$ = 0.1mA | |

### 3.8 DC Characteristics 3

| Parameter | Symbol | min. | max | Unit | Notes |
|---|---|---|---|---|---|
| AC differential input voltage | $V_{ID (AC)}$ | -0.2 | $V_{DDQ}$ + 0.2 | V | |
| AC differential cross point voltage | $V_{IX (AC)}$ | 0.5 x $V_{DDQ}$ - 0.15 | 0.5 x $V_{DDQ}$ + 0.15 | V | |
| AC differential cross point voltage | $V_{OX (AC)}$ | 0.5 x $V_{DDQ}$ - 0.2 | 0.5 x $V_{DDQ}$ + 0.2 | V | |

### 3.9

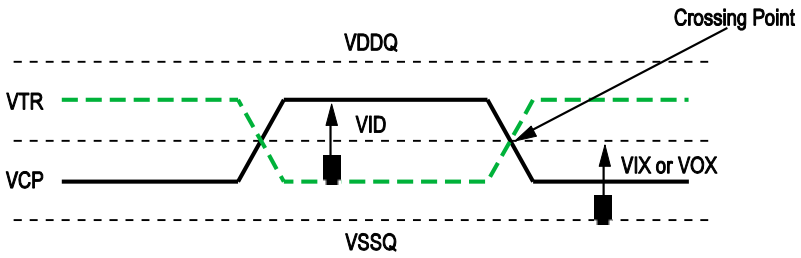



**Figure 1. Differential Signal Levels**

### *Pin Capacitance*

(TC = +25°C, $V_{DD1}$ = 1.7V to 1.95V, $V_{DD2}/V_{DDQ}$ = 1.14V to 1.3V, $V_{SS}/V_{SSCA}/V_{SSQ}$ = 0V)

| Parameter | Symbol | | LPDDR2 1066-466 | LPDDR2 400-200 | Unit | Notes |
|---|---|---|---|---|---|---|
| CLK input pin capacitance CK, /CK | $C_{CK}$ | min. | 1.0 | | pF | 1,2 |
| | | max | 2.0 | | | |
| CLK input pin capacitance Δ CK, /CK | $C_{DCK}$ | min. | 0 | | pF | 1,2,3 |
| | | max | 0.20 | 0.25 | | |
| Input pin capacitance CA, /CS, CKE | $C_I$ | min. | 1.0 | | pF | 1,2,4 |
| | | max | 2.0 | | | |
| Input pin capacitance Δ CA, /CS, CKE | $C_{DI}$ | min. | -0.4 | -0.5 | pF | 1,2,5 |
| | | max | 0.4 | 0.5 | | |
| Input/output pin capacitance DQS, /DQS, DQ, DM | $C_{IO}$ | min. | 1.25 | | pF | 1,2,6,7 |
| | | max | 2.5 | | | |
| Input/output pin capacitance Δ DQS, /DQS | $C_{DDQS}$ | min. | 0 | | pF | 1,2,7,8 |
| | | max | 0.25 | 0.30 | | |
| Input/output pin capacitance Δ DQ, DM | $C_{DIO}$ | min. | -0.5 | -0.6 | pF | 1,2,7,9 |
| | | max | 0.5 | 0.6 | | |
| Calibration pin capacitance | $C_{ZQ}$ | min. | 0 | | pF | 1,2 |
| | | max | 2.5 | | | |

Notes:

This parameter applies to die device only (does not include package capacitance)

This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with $V_{DD1}$, $V_{DD2}$, $V_{DDQ}$, $V_{SS}$, $V_{SSCA}$, $V_{SSQ}$ applied and all other pins floating.

Absolute value of $C_{CK\_t}$-$C_{CK\_c}$.

$C_I$ applies to /CS, CKE, CA0-CA9.

$C_{DI}=C_I-0.5x(C_{CK\_t}+C_{CK\_c})$

DM loading matches DQ and DQS

MR3 I/O configuration DS OP3-OP0=4'b0001 (34.3Ω typical)

Absolute value of $C_{DQS\_t}$ and $C_{DQS\_c}$.

$C_{DIO}=C_{IO}-0.5x(C_{DQS\_t}+C_{DQS\_c})$ in byte-lane.

## 3.10 *Refresh Requirement Parameters (1Gb)*

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Number of Banks | | 8 | |
| Refresh Window $T_{CASE} \leq 85°C$ | $t_{REFW}$ | 32 | ms |
| Refresh Window $85°C < T_{CASE} \leq 95°C$ | $t_{REFW}$ | 16 | ms |
| Refresh Window $95°C < T_{CASE} \leq 105°C$ | $t_{REFW}$ | 8 | ms |
| Required number of REFRESH commands (min) | R | 4,096 | |
| Average time between REFRESH commands TCASE ≤ 85°C | $t_{REFIab}$ | 7.8 | µs |
| Average time between REFRESH commands 85°C < TCASE ≤ 95°C | $t_{REFIab}$ | 3.9 | µs |
| Average time between REFRESH commands 95°C < TCASE ≤ 105°C | $t_{REFIab}$ | 1.95 | µs |
| All Bank Refresh Cycle time | $t_{RFCab}$ | 130 | ns |
| Per Bank Refresh Cycle time | $t_{RFCpb}$ | 60 | ns |
| Burst Refresh Window = 4 x 8 x $t_{RFCab}$ | $t_{REFBW}$ | 4.16 | µs |

### 3.11 AC Characteristics

| Parameter | Symbol | min/max | min $t_{CK}$ | LPDDR2 | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | Mbps |
| Max. Frequency | | ~ | | 533 | 466 | 400 | 333 | 266 | 200 | 166 | MHz |
| Clock Timing | | | | | | | | | | | |
| Average Clock Period | $t_{CK}$(avg) | min | | 1.875 | 2.15 | 2.5 | 3 | 3.75 | 5 | 6 | ns |
| | | max | | 100 | | | | | | | |
| Average high pulse width | $t_{CH}$(avg) | min | | 0.45 | | | | | | | $t_{CK}$(avg) |
| | | max | | 0.55 | | | | | | | |
| Average low pulse width | $t_{CL}$(avg) | min | | 0.45 | | | | | | | $t_{CK}$(avg) |
| | | max | | 0.55 | | | | | | | |
| Absolute Clock Period | $t_{CK}$(abs) | min | | $t_{CK}$(avg)(min) + $t_{JIT}$(per)(min) | | | | | | | ps |
| Absolute clock HIGH pulse width (with allowed jitter) | $t_{CH}$(abs) | min | | 0.43 | | | | | | | $t_{CK}$(avg) |
| | | max | | 0.57 | | | | | | | |
| Absolute clock LOW pulse width (with allowed jitter) | $t_{CH}$(abs) | min | | 0.43 | | | | | | | $t_{CK}$(avg) |
| | | max | | 0.57 | | | | | | | |
| Clock Period Jitter (with allowed jitter) | $t_{JIT}$(per) | min | | -90 | -95 | -100 | -110 | -120 | -140 | -150 | ps |
| | | max | | 90 | 95 | 100 | 110 | 120 | 140 | 150 | |
| Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter) | $t_{JIT}$(cc) | max | | 180 | 190 | 200 | 220 | 240 | 280 | 300 | ps |
| Duty cycle Jitter (with allowed jitter) | $t_{JIT}$(duty) allowed | min | | min(($t_{CH}$(abs),min - $t_{CH}$(avg),min) ($t_{CL}$(abs), min - $t_{CL}$(avg), min)) x $t_{CK}$(avg) | | | | | | | ps |
| | | max | | max(($t_{CH}$(abs),max - $t_{CH}$(avg),max) ($t_{CL}$(abs), max - $t_{CL}$(avg), max)) x $t_{CK}$(avg) | | | | | | | |
| Cumulative error across 2 cycles | $t_{ERR}$(2per) allowed | min | | -132 | -140 | -147 | -162 | -177 | -206 | -221 | ps |
| | | max | | 132 | 140 | 147 | 162 | 177 | 206 | 221 | |
| Cumulative error across 3 cycles | $t_{ERR}$(3per) allowed | min | | -157 | -166 | -175 | -192 | -210 | -245 | -262 | ps |
| | | max | | 157 | 166 | 175 | 192 | 210 | 245 | 262 | |
| Cumulative error across 4 cycles | $t_{ERR}$(4per) allowed | min | | -175 | -185 | -194 | -214 | -233 | -272 | -291 | ps |
| | | max | | 175 | 185 | 194 | 214 | 233 | 272 | 291 | |
| Cumulative error across 5 cycles | $t_{ERR}$(5per) allowed | min | | -188 | -199 | -209 | -230 | -251 | -293 | -314 | ps |
| | | max | | 188 | 199 | 209 | 230 | 251 | 293 | 314 | |
| Cumulative error across 6 cycles | $t_{ERR}$(6per) allowed | min | | -200 | -210 | -222 | -244 | -266 | -311 | -333 | ps |
| | | max | | 200 | 210 | 222 | 244 | 266 | 311 | 333 | |
| Cumulative error across 7 cycles | $t_{ERR}$(7per) allowed | min | | -209 | -221 | -232 | -256 | -279 | -325 | -348 | ps |
| | | max | | 209 | 221 | 232 | 256 | 279 | 325 | 348 | |

| Parameter | Symbol | min/max | min $t_{CK}$ | LPDDR2 | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | Mbps |
| Cumulative error across 8 cycles | $t_{ERR}$(8per) allowed | min | | -217 | -229 | -241 | -256 | -290 | -338 | -362 | ps |
| | | max | | 217 | 229 | 241 | 256 | 290 | 338 | 362 | |
| Cumulative error across 9 cycles | $t_{ERR}$(9per) allowed | min | | -224 | -237 | -249 | -274 | -299 | -349 | -374 | ps |
| | | max | | 224 | 237 | 249 | 274 | 299 | 349 | 374 | |
| Cumulative error across 10 cycles | $t_{ERR}$(10per) allowed | min | | -231 | -244 | -257 | -282 | -308 | -359 | -385 | ps |
| | | max | | 231 | 244 | 257 | 282 | 308 | 359 | 385 | |
| Cumulative error across 11 cycles | $t_{ERR}$(11per) allowed | min | | -237 | -250 | -263 | -289 | -316 | -368 | -395 | ps |
| | | max | | 237 | 250 | 263 | 289 | 316 | 368 | 395 | |
| Cumulative error across 12 cycles | $t_{ERR}$(12per) allowed | min | | -242 | -256 | -269 | -296 | -323 | -377 | -403 | ps |
| | | max | | 242 | 256 | 269 | 296 | 323 | 377 | 403 | |
| Cumulative error across n = 13, 14 … 49, 50 cycles | $t_{ERR}$(nper) allowed | min | | $t_{ERR}$(nper), allowed, min = (1 + 0.68ln(n)) x $t_{JIT}$(per), allowed, min | | | | | | | ps |
| | | max | | $t_{ERR}$(nper), allowed, max = (1 + 0.68ln(n)) x $t_{JIT}$(per), allowed, max | | | | | | | |
| ZQ Calibration Parameters | | | | | | | | | | | |
| Initialization Calibration Time | $t_{ZQINIT}$ | min | | 1 | | | | | | | µs |
| Long Calibration Time | $t_{ZQCL}$ | min | 6 | 360 | | | | | | | ns |
| Short Calibration Time | $t_{ZQCS}$ | min | 6 | 90 | | | | | | | ns |
| Calibration Reset Time | $t_{ZQRESET}$ | min | 3 | 50 | | | | | | | ns |
| Read Parameters | | | | | | | | | | | |
| DQS output access time from CK_t/CK_c | $t_{DQSCK}$ | min | | 2500 | | | | | | | ps |
| | | max | | 5500 | | | | | | | |
| DQSCK Delta Short | $t_{DQSCKDS}$ | max | | 330 | 380 | 450 | 540 | 670 | 900 | 1080 | ps |
| DQSCK Delta Medium | $t_{DQSCKDM}$ | max | | 680 | 780 | 900 | 1050 | 1350 | 1800 | 1900 | ps |
| DQSCK Delta Long | $t_{DQSCKDL}$ | max | | 920 | 1050 | 1200 | 1400 | 1800 | 2400 | - | ps |
| DQS-DQ skew | $t_{DQSQ}$ | max | | 200 | 220 | 240 | 280 | 340 | 400 | 500 | ps |
| Data hold skew factor | $t_{QHS}$ | max | | 230 | 260 | 280 | 340 | 400 | 480 | 600 | ps |
| DQS Output High Pulse Width | $t_{QSH}$ | min | | $t_{CH}$(abs) - 0.05 | | | | | | | $t_{CK}$(avg) |
| DQS Output Low Pulse Width | $t_{QSL}$ | min | | $t_{CL}$(abs) - 0.05 | | | | | | | $t_{CK}$(avg) |
| Data Half Period | $t_{QHP}$ | min | | min($t_{QSH}$, $t_{QSL}$) | | | | | | | $t_{CK}$(avg) |
| DQ/DQS output hold time from DQS | $t_{QH}$ | min | | $t_{QHP}$-$t_{QHS}$ | | | | | | | ps |
| Read preamble | $t_{RPRE}$ | min | | 0.9 | | | | | | | $t_{CK}$(avg) |
| Read Postamble | $t_{RPST}$ | min | | $t_{CL}$(abs) - 0.05 | | | | | | | $t_{CK}$(avg) |
| DQS low-Z from clock | $t_{LZ(DQS)}$ | min | | $t_{DQSCK(min)}$ - 300 | | | | | | | ps |
| DQ low-Z from clock | $t_{LZ(DQ)}$ | min | | $t_{DQSCK(min)}$ - (1.4*$t_{QHS(max)}$) | | | | | | | ps |
| DQS high-Z from clock | $t_{HZ(DQS)}$ | max | | $t_{DQSCK(max)}$ - 100 | | | | | | | ps |

| Parameter | Symbol | min/max | min $t_{CK}$ | LPDDR2 | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | Mbps |
| **Write Parameters** | | | | | | | | | | | |
| DQ and DM input hold time (Vref based) | $t_{DH}$ | min | | 210 | 235 | 270 | 350 | 430 | 480 | 600 | ps |
| DQ and DM input setup time (Vref based) | $t_{DS}$ | min | | 210 | 235 | 270 | 350 | 430 | 480 | 600 | ps |
| DQ and DM input pulse width | $t_{DIPW}$ | min | | 0.35 | | | | | | | $t_{CK}$(avg) |
| Write command to 1st DQS latching transition | $t_{DQSS}$ | min | | 0.75 | | | | | | | $t_{CK}$(avg) |
| | | max | | 1.25 | | | | | | | $t_{CK}$(avg) |
| DQS input high-level width | $t_{DQSH}$ | min | | 0.4 | | | | | | | $t_{CK}$(avg) |
| DQS input low-level width | $t_{DQSL}$ | min | | 0.4 | | | | | | | $t_{CK}$(avg) |
| DQS falling edge to CK setup time | $t_{DSS}$ | min | | 0.2 | | | | | | | $t_{CK}$(avg) |
| DQS falling edge hold time from CK | $t_{DSH}$ | min | | 0.2 | | | | | | | $t_{CK}$(avg) |
| Write postamble | $t_{WPST}$ | min | | 0.4 | | | | | | | $t_{CK}$(avg) |
| Write preamble | $t_{WPRE}$ | min | | 0.35 | | | | | | | $t_{CK}$(avg) |
| **CKE Input Parameters** | | | | | | | | | | | |
| CKE min. pulse width (high and low pulse width) | $t_{CKE}$ | min | 3 | 3 | | | | | | | $t_{CK}$(avg) |
| CKE input setup time | $t_{ISCKE}$ | min | | 0.25 | | | | | | | $t_{CK}$(avg) |
| CKE input hold time | $t_{IHCKE}$ | min | | 0.25 | | | | | | | $t_{CK}$(avg) |
| **Command Address Input Parameters** | | | | | | | | | | | |
| Address & control input setup time (Vref based) | $t_{IS}$ | min | | 220 | 250 | 290 | 370 | 460 | 600 | 740 | ps |
| Address & control input hold time (Vref based) | $t_{IH}$ | min | | 220 | 250 | 290 | 370 | 460 | 600 | 740 | ps |
| Address & control input pulse width | $t_{IPW}$ | min | | 0.40 | | | | | | | $t_{CK}$(avg) |
| **Boot Parameters (10 MHz - 55 MHz)** | | | | | | | | | | | |
| Clock Cycle Time | $t_{CKb}$ | max | - | 100 | | | | | | | ns |
| | | min | | 18 | | | | | | | |
| CKE input setup time | $t_{ISCKEb}$ | min | - | 2.5 | | | | | | | ns |
| CKE input hold time | $t_{IHCKEb}$ | min | - | 2.5 | | | | | | | ns |
| Address & control input setup time | $t_{ISb}$ | min | - | 1150 | | | | | | | ps |
| Address & control input hold time | $t_{IHb}$ | min | - | 1150 | | | | | | | ps |
| DQS Output data access time from CK_t/CK_c | $t_{DQSCKb}$ | min | - | 2.0 | | | | | | | ns |
| | | max | | 10.0 | | | | | | | |
| Data strobe edge to output data edge $t_{DQSQb}$-1.2 | $t_{DQSQb}$ | max | - | 1.2 | | | | | | | ns |
| Data hold skew factor | $t_{QHSb}$ | max | - | 1.2 | | | | | | | ns |
| **Mode Register Parameters** | | | | | | | | | | | |
| Mode Register Write command period | $t_{MRW}$ | min | 5 | 5 | | | | | | | $t_{CK}$(avg) |
| Mode Register Read command period | $t_{MRR}$ | min | 2 | 2 | | | | | | | $t_{CK}$(avg) |

| Parameter | Symbol | min/max | min $t_{CK}$ | LPDDR2 | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1066 | 933 | 800 | 667 | 533 | 400 | 333 | Mbps |
| LPDDR2 SDRAM Core Parameters | | | | | | | | | | | |
| Read Latency | RL | min | 3 | 8 | 7 | 6 | 5 | 4 | 3 | 3 | $t_{CK}$(avg) |
| Write Latency | WL | min | 1 | 4 | 4 | 3 | 2 | 2 | 1 | 1 | $t_{CK}$(avg) |
| Active to Active command period | $t_{RC}$ | min | - | $t_{RAS}$ + $t_{RPab}$ (with all-bank Precharge)<br>$t_{RAS}$ + $t_{RPab}$ (with per-bank Precharge) | | | | | | | ns |
| CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh) | $t_{CKESR}$ | min | 3 | 15 | | | | | | | ns |
| Self refresh exit to next valid command delay | $t_{XSR}$ | min | 2 | $t_{RFCab}$+10 | | | | | | | ns |
| Exit power down to next valid command delay | $t_{XP}$ | min | 2 | 7.5 | | | | | | | ns |
| LPDDR2-S4 CAS to CAS delay | $t_{CCD}$ | min | 2 | 2 | | | | | | | $t_{CK}$(avg) |
| Internal Read to Precharge command delay | $t_{RTP}$ | min | 2 | 7.5 | | | | | | | ns |
| RAS to CAS Delay | $t_{RCD}$ | min | 3 | 18 (typical) | | | | | | | ns |
| Row Precharge Time (single bank) | $t_{RPpb}$ | min | 3 | 18 (typical) | | | | | | | ns |
| Row Precharge Time (all banks) | $t_{RPab}$ | min | 3 | 21 (greater than typical, less than slow) | | | | | | | ns |
| Row Active Time | $t_{RAS}$ | min | 3 | 42 | | | | | | | ns |
| | | max | - | 70 | | | | | | | µs |
| Write Recovery Time | $t_{WR}$ | min | 3 | 15 | | | | | | | ns |
| Internal Write to Read command delay | $t_{WTR}$ | min | 2 | 7.5 | | | | | 10 | | ns |
| Active bank A to Active bank B | $t_{RRD}$ | min | 2 | 10 | | | | | | | ns |
| Four Bank Activate window | $t_{FAW}$ | min | 8 | 50 | | | | | | 60 | ns |
| Minimum Deep Power Down time | $t_{DPD}$ | min | | 500 | | | | | | | µs |

# 4 Block Diagram

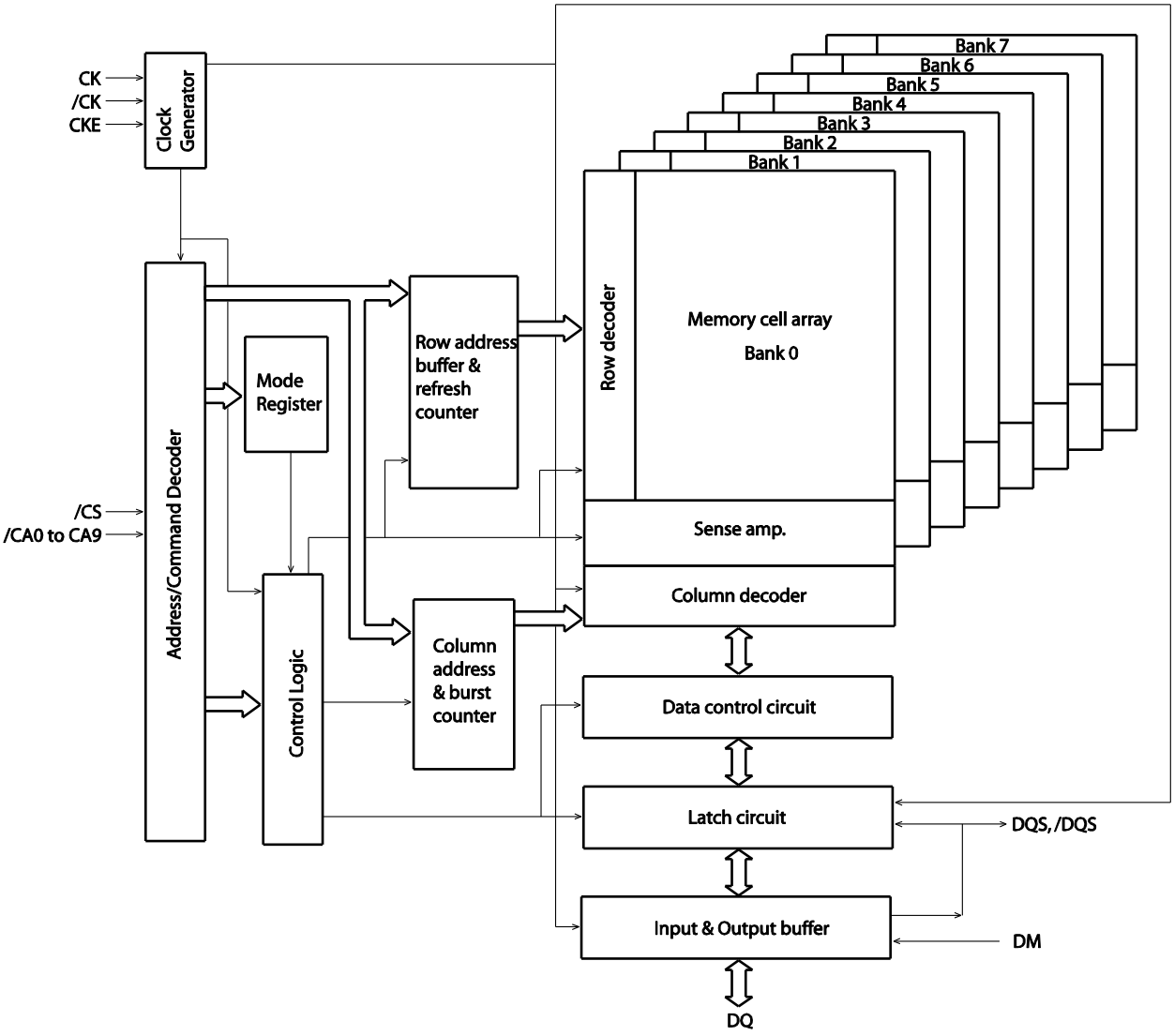



**Figure 2. Block Diagram**

# 5 Pin Function

## *5.1 CK, /CK (input pins)*

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the /CK falling edge. When in a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When in a write operation, DMs and DQs are referred to the cross point of the DQS and the $V_{DDQ}/2$ level. DQSs for write operation are referred to the cross point of the CK and the /CK. The other input signals are referred at CK rising edge.

## *5.2 /CS (input pin)*

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

## *5.3 CA0 to CA9 (input pins)*

These pins define the row & column addresses and operating commands (read, write, etc.) depend on their voltage levels. See "Addressing Table" and “Command operation”.

## *5.4 [Addressing Table]*

| Part Number | Organization | Row address | Column address |
|---|---|---|---|
| AD210016F-x | x 16 bits | R0 to R12 | C0[*1] to C9 |
| AD210032F-x | x 32 bits | R0 to R12 | C0[*1] to C8 |

| Command | DDR CA Pins | | | | | | | | | | CK edge |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 | |
| Active | -- | -- | R8 | R9 | R10 | R11 | R12 | BA0 | BA1 | BA2 | ↑ |
| | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | -- | -- | ↓ |
| Write/Read | -- | -- | -- | -- | -- | C1 | C2 | BA0 | BA1 | BA2 | ↑ |
| | AP | C3 | C4 | C5 | C6 | C7 | C8 | C9 | -- | -- | ↓ |

Remarks: Rx = row address. Cx = column address
Notes:
C0 is not present on the command & address, therefore C0 is implied to be zero.

BA0,1 &2 are bank select signals. The memory array is divided into 8 banks. BA0,1 & 2 define to which bank an active/read/write/precharge command is being applied.

AP defines the precharge mode when a read command or a write command is issued. If AP = high during a read or write command, auto precharge function is enabled.

### 5.5 [Bank Numbering and BA Input Table]

| | BA0 | BA1 | BA2 |
|---|---|---|---|
| Bank0 | L | L | L |
| Bank1 | H | L | L |
| Bank2 | L | H | L |
| Bank3 | H | H | L |
| Bank4 | L | L | H |
| Bank5 | H | L | H |
| Bank6 | L | H | H |
| Bank7 | H | H | H |

Remarks: H = VIH, L = VIL.

### 5.6 CKE (input pin)

CKE controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE level must be kept for 2 clocks at least if CKE changes at the crossing point of the CK rising edge and the /CK falling edge with proper setup time tIS, by the next CK rising edge CKE level must be kept with proper hold time tIH.

### 5.7 DQ0 to DQ15 (x16), DQ0 to DQ31 (x32) - (input/output pins)

Data are input to and output from these pins.

### 5.8 DQSx, /DQSx (input/ output pins, where x = 0 to 3)

DQS and /DQS provide the read data strobes (as output) and the write data strobes (as input). Each DQS (/DQS) pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

### 5.9 DM0 to DM3 (input pins)

DM is the reference signals of the data input mask function. DM is sampled at the crossing point of DQS and $V_{DDQ}/2$. When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up.

### 5.10 [DM truth table]

| Name (Functional) | DM | DQ | Note |
|---|---|---|---|
| Write enable | L | Valid | 1 |
| Write inhibit | H | X | 1 |

Notes:
Used to mask write data. Provided coincident with the corresponding data.

Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

### 5.11 [DQS and DM Correspondence Table]

| Part Number | Organization | DQS | Data Mask | DQ |
|---|---|---|---|---|
| AD210016F-x | x 16 bits | DQS0, /DQS0 | DM0 | DQ0 to DQ7 |
| | | DQS1, /DQS1 | DM1 | DQ8 to DQ15 |
| AD210032F-x | x 32 bits | DQS0, /DQS0 | DM0 | DQ0 to DQ7 |
| | | DQS1, /DQS1 | DM1 | DQ8 to DQ15 |
| | | DQS2, /DQS2 | DM2 | DQ16 to DQ23 |
| | | DQS3, /DQS3 | DM3 | DQ24 to DQ31 |

### 5.12 $V_{DD1}$, $V_{SS}$, $V_{SS2}$, $V_{SSCA}$, $V_{DDQ}$, $V_{SSQ}$ (power supply)

$V_{DD1/2}$ and $V_{SS}$ are power supply pins for internal circuits. $V_{DDQ}$ and $V_{SSQ}$ are power supply pins for the output buffers. $V_{SSCA}$ is a power supply pin for command address input buffers.

# 6 Command Operation

## 6.1 Command Truth Table

The LPDDR2 RAM recognizes the following commands specified by the /CS, CA0, CA1, CA2, CA3 and CKE at the rising edge of the clock.

- CAxr refers to the command/address bit x on the rising edge of clock. (↑)
- CAxf refers to the command/address bit x on the falling edge of clock. (↓)

| Function | Symbol | CKE | | /CS | DDR CA Pins | | | | | | | | | | CK edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Previous cycle | Current cycle | | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | CA6 | CA7 | CA8 | CA9 | |
| Mode register write | MRW | H | H | L | L | L | L | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | ↑ |
| | | | | × | MA6 | MA7 | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | OP6 | OP7 | ↓ |
| Mode register read | MRR | H | H | L | L | L | L | H | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | ↑ |
| | | | | × | MA6 | MA7 | × | | | | | | | | ↓ |
| Refresh per bank | REFpb | H | H | L | L | L | H | L | × | | | | | | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| Refresh all banks | REFab | H | H | L | L | L | H | H | × | | | | | | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| Self-refresh entry | SELF | H | L | L | L | L | H | × | | | | | | | ↑ |
| | | × | | × | × | | | | | | | | | | ↓ |
| Bank activate | ACT | H | H | L | L | H | R8 | R9 | R10 | R11 | R12 | BA0 | BA1 | BA2 | ↑ |
| | | | | × | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | × | | ↓ |
| Write | WRIT | H | H | L | H | L | L | RFU | RFU | C1 | C2 | BA0 | BA1 | BA2 | ↑ |
| | | | | × | AP[*1] | C3 | C4 | C5 | C6 | C7 | C8 | C9 | × | | ↓ |
| Read | READ | H | H | L | H | L | H | RFU | RFU | C1 | C2 | BA0 | BA1 | BA2 | ↑ |
| | | | | × | AP[*1] | C3 | C4 | C5 | C6 | C7 | C8 | C9 | × | | ↓ |
| Precharge | PRE | H | H | L | H | H | L | H | AB | × | | BA0 | BA1 | BA2 | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| Burst terminate | BST | H | H | L | H | H | L | L | × | | | | | | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| Deep power-down mode entry | DPDEN | H | L | L | H | H | L | × | | | | | | | ↑ |
| | | × | | × | × | | | | | | | | | | ↓ |
| No operation | NOP | H | H | L | H | H | H | × | | | | | | | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| Maintain PD/SREF/DPD | NOP | L | L | L | H | H | H | × | | | | | | | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| No operation | NOP | H | H | H | × | | | | | | | | | | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| Device deselect | DESL | H | H | H | × | | | | | | | | | | ↑ |
| | | | | × | × | | | | | | | | | | ↓ |
| Power-down mode entry | PDEN | H | L | H | × | | | | | | | | | | ↑ |
| | | × | | × | × | | | | | | | | | | ↓ |
| Exit power-down/deep power-down mode, self refresh | PDEX, SELFX, DPDX | L | H | H | × | | | | | | | | | | ↑ |
| | | × | | × | × | | | | | | | | | | ↓ |

Remarks: H = $V_{IH}$, L = $V_{IL}$, × = $V_{IH}$ or $V_{IL}$, Rx = row address, Cx = column address,
AB = all banks or selected bank precharge.

Notes:

AP high during a read or write command indicates that an auto precharge will occur to the bank associated with the read or write command.

Bank selects (BA0, 1 & 2) determine which bank is to be operated upon.

Self-refresh exit and deep power-down exit are asynchronous.

/CS and CKE are sampled at the rising edge of clock.

VREF must be maintained during self-refresh and deep power-down operation.

### *6.2 Register Commands [MRR/MRW]*

The register commands include both a mode register read (MRR) and a mode register write (MRW) command. The protocol provides support for a total of up to 256 8-bit registers, which will be either read-only, write-only, or both readable and writeable by the memory controller.

### *6.3 Refresh Commands [REF]*

The refresh commands include an All Banks refresh command, and a self-refresh command. Entry into self-refresh mode will occur upon the transition of CKE from high to low.

### *6.4 Active Command [ACT]*

Only CA0r and CA1r are needed to encode this command. The remaining bits in the CA map specify the row and bank address.

### *6.5 Read/Write Commands [READ/WRIT]*

The read and write commands indicate whether a read or write is desired. CA0r, CA1r, and CA2r are needed to encode either command. The remaining bits in the CA map are used to indicate the column address. A bit to indicate whether an auto precharge is desired is provided and is registered on CA0f of both read and write commands. Two bits in the read and write command encoding have been specified as Reserved for Future Use (RFU).

### *6.6 Precharge Commands [PRE]*

The Precharge command requires that the bank be specified at command time only when the auto precharge bit indicates that an All Bank pre-charge is not desired (I.E. AB (CA4r) = 0). If the All Bank precharge bit is set (I.E. AB (CA4r) = 1), bank information is not required.

### *6.7 Burst Terminate Command [BST]*

The BST command will allow for both read and write commands (without auto precharge) to be interrupted on prefetch boundaries prior to the end of a burst. The desired burst length will be set in one of the mode registers.

### *6.8 Power-down and Deep Power Down [PDEN/DPDEN]*

Both power-down and deep power-down modes are supported by the protocol. In normal power-down mode all input and output buffers as well as CK and /CK will be disabled. If all banks are precharged prior to entering power-down mode, the device will be said to be in Precharge power-down mode. If at least one bank is open while entering power-down mode, the SDRAM device will be said to be in Active power-down mode.

In Deep power-down mode all input/output buffers, CK, /CK, and power to the array will be disabled. The contents of the SDRAM will be lost upon entry into deep power-down mode.

The command for entry into normal power-down mode requires that /CS is high, while the command for entry into Deep power-down mode requires that /CS be low. In both cases CKE will remain active and will be the mechanism by which the SDRAM is able to exit either power-down modes.

### 6.9 Exit Command [PDEX, DPDX, SELFX]

Exit from self-refresh, power down, or deep power-down modes requires a low to high transition of CKE.

### 6.10 No Operation Command [NOP]

NOP can either be issued using a command when /CS is low or by simply deselecting /CS.

### 6.11 CKE Truth Table

| | CKE | | Command (n) *3 | | |
|---|---|---|---|---|---|
| Current state *2 | Previous cycle (n-1) *1 | Current cycle (n) *1 | /CS, CA0r to CA3r | Operation (n) *3 | Notes |
| Active/Idle power-down | L | L | × | Maintain power-down | 8 |
| | L | H | DESL or NOP | Power-down exit | 4 |
| Deep power-down entry | L | L | × | Maintain power-down | 8 |
| | L | H | DESL or NOP | Deep power-down exit | |
| Self-refresh | L | L | × | Maintain self-refresh | 8 |
| | L | H | DESL or NOP | Self-refresh exit | 4, 7 |
| Bank Active | H | L | DESL or NOP | Active power down entry | 4 |
| All banks idle | H | L | DESL or NOP | Precharge power down entry | 4 |
| | H | L | SELF | Self-refresh entry | 5 |
| Other | H | H | Refer to the Command Truth Table | | 6 |

Remark: H = $V_{IH}$, L = $V_{IL}$, × = Don't care

Notes:

CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.

Current state is the state of the LPDDR2 RAM immediately prior to clock edge n.

Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n).

All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

Self-refresh mode can only be entered from the all banks idle state.

Must be a legal command as defined in the command truth table.

Valid commands for deep power-down exit and power-down exit and self-refresh exit are NOP and DESL only.

Deep power-down, power-down and self-refresh cannot be entered while read/write operations, mode register read/write or precharge operations are in progress.

$V_{REF}$ must be maintained during self-refresh operation.

Clock frequency may be changed or stopped during the active power-down or idle power-down state.

# 7 Simplified State Diagram

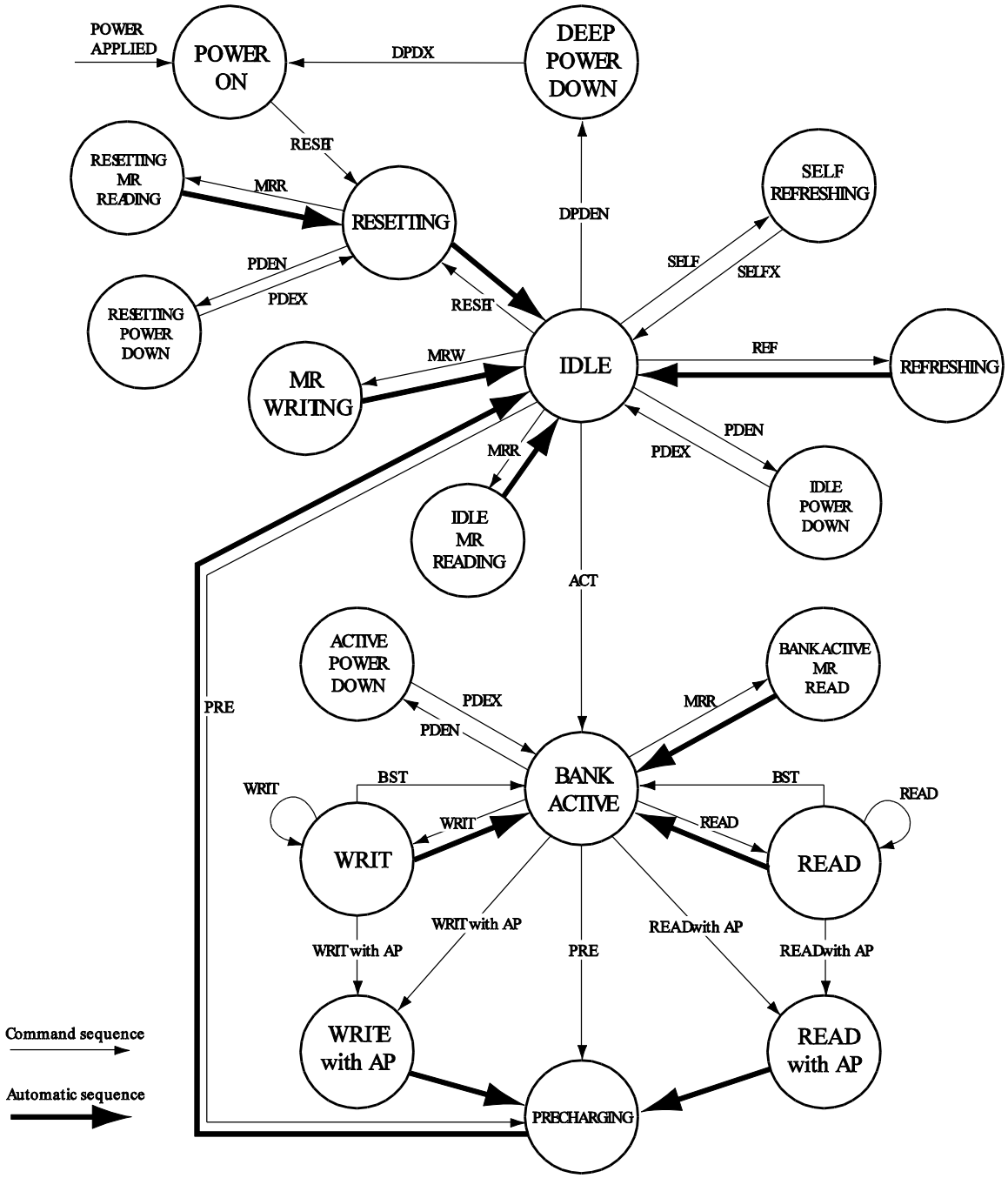



**Figure 3 Simplified State Diagram**

# 8 Operation of the LPDDR2 RAM

Read and write accesses to the LPDDR2 RAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of four, eight, and sixteen in a programmed sequence. Accesses begin with the registration of an active command, which is then followed by a read or write command. The address bits registered coincident with the active command is used to select the bank and row to be accessed (BA0, 1 & 2 selects the bank; R0 to R12 selects the row). The address bits registered coincident with the read or write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued.

Prior to normal operations, the LPDDR2 RAM must be initialized. The following sections provide detailed information covering device initialization; register definition, command descriptions and device operation.

## *8.1 LPDDR2 RAM Power-On and Initialization Sequence*

### *8.1.1 Power Ramp and Device Initialization*

**Power Ramp**

While applying power (after Ta), CKE shall be held at a logic low level (≤0.2 × $V_{DD2}$), all other inputs shall be between $V_{IL}$ (min.) and $V_{IH}$ (max.). The LPDDR2 RAM device will only guarantee that outputs are in a high impedance state while CKE is held low. On or before the completion of the power ramp (Tb) CKE must be held low. Voltage levels at I/Os and outputs must be between $V_{SSQ}$ and $V_{DDQ}$ during voltage ramp time to avoid latch-up.

The following conditions apply:

- Ta is the point where any power supply first reaches 300mV.
- After Ta is reached, $V_{DD1}$ must be greater than $V_{DD2}$ – 200mV.
- After Ta is reached, $V_{DD1}$ and $V_{DD2}$ must be greater than $V_{DDQ}$ – 200mV.
- After Ta is reached, $V_{REF}$ must always be less than all other supply voltages.
- The voltage difference between any of $V_{SS}$, $V_{SSQ}$, and $V_{SSCA}$ pins may not exceed 100mV.
- Tb is the point when all supply and reference voltages are within their respective min/max operating conditions.
- Power ramp duration $t_{INIT0}$ (Tb – Ta) must be no greater than 20ms.

Note: $V_{DD2}$ is not present in some systems. Rules related to $V_{DD2}$ in those cases do not apply.

**CKE and Clock**

Beginning at Tb, CKE must remain low for at least $t_{INIT1}$ = 100ns, after which it may be asserted high. Clock must be stable at least $t_{INIT2}$ = $5t_{CK}$ prior to the first low to high transition of CKE (Tc). CKE, /CS and CA inputs must observe setup and hold time ($t_{IS}$, $t_{IH}$) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

**Reset Command**

After $t_{INIT3}$ is satisfied, a MRW (Reset) command shall be issued (Td). Wait for at least $t_{INIT4}$ = 1µs while keeping CKE asserted and issuing NOP or DESL commands.

**Mode Register Reads and Device Auto-Initialization (DAI) polling**

After $t_{INIT4}$ is satisfied (Te), only MRR commands (including power-down entry/exit) are allowed. It is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0, Device ID, etc.). The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete. As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured. After the DAI-bit (MR0.DAI) is set to "ready" by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR0 DAI. The LPDDR2 RAM will set the DAI-bit no later than $t_{INIT5}$ (10µs) after the Reset command.

**Normal Operation**

After $t_{INIT5}$ (Tf), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. The LPDDR2 RAM device will now be in IDLE state and ready for any valid command. After Tf, the clock frequency may be changed according to the clock frequency change procedure described in section Input Clock Stop and Frequency Change during Power-Down of this specification.

### 8.1.2 *Timing Parameters for Initialization*

| Symbol | Value | | Unit | Test Condition |
|---|---|---|---|---|
| | min. | max. | | |
| $t_{INIT0}$ | -- | 20 | ms | Maximum Power Ramp Time |
| $t_{INIT1}$ | 100 | -- | ns | Minimum CKE low time after completion of power ramp |
| $t_{INIT2}$ | 5 | -- | tCK | Minimum stable clock before first CKE high |
| $t_{INIT3}$ | 200 | -- | µs | Minimum Idle time after first CKE assertion |
| $t_{INIT4}$ | 1 | -- | µs | Minimum Idle time after Reset command, this time will be about 2 × $t_{RFCab}$ (max density) + $t_{RP}$ |
| $t_{INIT5}$ | -- | 10 | µs | Maximum duration of Device Auto-Initialization |
| $t_{CKBOOT}$ | 18 | 100 | ns | Clock cycle time during boot |

[See Figure 134 in JEDEC Standard No. 209-2E]

**Initialization After RESET (without power ramp)**
If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

**Power-off Sequence**
The following procedure is required to power off the device.
While powering off, CKE must be held LOW (≤0.2 × $V_{DD2}$);.all other inputs must be between $V_{ILmin}$ and $V_{IHmax}$.
The device outputs remain at High-Z while CKE is held LOW.
DQ, DM, DQS_t, and DQS_c voltage levels must be between $V_{SSQ}$ and $V_{DDQ}$ during the power-off sequence to avoid latch-up.
CK_t, CK_c, CS_n, and CA input levels must be between $V_{SS}$ and $V_{DD2}$ during the power-off sequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see the following Table).

| Between… | Applicable Conditions |
|---|---|
| Tx and Tz | $V_{DD1}$ must be greater than $V_{DD2}$ -- 200mV |
| Tx and Tz | $V_{DD1}$ must be greater than $V_{DDCA}$ -- 200mV |
| Tx and Tz | $V_{DD1}$ must be greater than $V_{DDQ}$ -- 200mV |
| Tx and Tz | $V_{REF}$ must always be less than all other supply voltages |

The voltage difference between any of $V_{SS}$ and $V_{SSQ}$ pins must not exceed 100mV.

**Uncontrolled Power-Off Sequence**
When an uncontrolled power-off occurs, the following conditions must be met:
At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

**Power-up, Initialization, and Power-off (cont'd)**
After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. $V_{DD1}$ and $V_{DD2}$ must decrease with a slope lower than 0.5 V/µs between Tx and Tz.
An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

| Symbol | Value | | Unit | Comment |
|---|---|---|---|---|
| | min. | max. | | |
| $t_{POFF}$ | -- | 2 | s | Maximum Power-Off ramp time |

## 8.2 Programming the Mode Register

### 8.2.1 Mode Register Assignment

| MR No. | MA [7:0] | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 00h | Device Info. | R | (RFU) | | | | | | DI | DAI | See MR0 |
| 1 | 01h | Device Feature 1 | W | nWR (for AP) | | | WC | BT | BL | | | See MR1 |
| 2 | 02h | Device Feature 2 | W | (RFU) | | | | RL & WL | | | | See MR2 |
| 3 | 03h | I/O Config-1 | W | (RFU) | | | | DS | | | | See MR3 |
| 4 | 04h | SDRAM Refresh Rate | R | TUF | (RFU) | | | | Refresh Rate | | | See MR4 |
| 5 | 05h | Basic Config-1 | R | Company ID | | | | | | | | See MR5 |
| 6 | 06h | Basic Config-2 | R | Revision ID1 | | | | | | | | See MR6 |
| 7 | 07h | Basic Config-3 | R | Revision ID2 | | | | | | | | See MR7 |
| 8 | 08h | Basic Config -4 | R | I/O Width | | Density | | | | Type | | See MR8 |
| 9 | 09h | Test Mode | W*[1] | Vendor-Specific Test Mode | | | | | | | | See MR9 |
| 10 | 0Ah | IO Calibration | W | Calibration Code | | | | | | | | See MR10 |
| 11:15 | 0Bh TO 0Fh | Reserved | | (RFU) | | | | | | | | |
| 16 | 10h | PASR_Bank | W | Bank Mask | | | | | | | | See MR16 |
| 17 | 11h | PASR_Seg | W | Segment Mask | | | | | | | | See MR17 |
| 17:23 | 11h TO 17h | Reserved | | (RFU) | | | | | | | | |

MR No.24 to 31 are Non-Volatile Memory (NVM) specific mode registers, which LPDDR2 does not have.

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 32 | 20h | Calibration Pattern A | R | Calibration Pattern A | | | | | | | | See MR32 |
| 40 | 28h | Calibration Pattern B | R | Calibration Pattern B | | | | | | | | See MR40 |
| 63 | 3FH | Reset | W | × | | | | | | | | See MR63 |

MR No. 33 to 39, 41 to 62 and MR 64 to 255 are reserved.

Note: MR9[5] is Fail Bit, and Read-Only.

Remarks: R = read-only
W = write-only
DAI = Device Auto-Initialization
DI = Device Information
nWR = Write Recovery for auto precharge
WC = Wrap Control
BT = Burst Type
BL = Burst Length
RL & WL = Read latency & Write latency
DS = Drive Strength
TUF = Temperature Update Flag

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR0 | (RFU) | | | | | | DI | DAI |

| | | | |
|---|---|---|---|
| Device Auto-Initialization | Read-only | 0 | DAI complete |
| | | 1 | DAI still in progress |
| Device Information | Read-only | 0 | SDRAM |
| | | 1 | Reserved |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR1 | nWR (for AP) | | | WC | BT | BT | | |

| | | | |
|---|---|---|---|
| Burst Length | Write-only | 010 | BL4 (default) |
| | | 011 | BL8 |
| | | 100 | BL16 |
| | | Other | Reserved |
| Burst Type | Write-only | 0 | Sequential (default) |
| | | 1 | Interleaved |
| Wrap Control | Write-only | 0 | Wrap (default) |
| | | 1 | No Wrap |
| Write Recovery for Autoprecharge* | Write-only | 001 | nWR=3 (default) |
| | | 010 | nWR=4 |
| | | 011 | nWR=5 |
| | | 100 | nWR=6 |
| | | 101 | nWR=7 |
| | | 110 | nWR=8 |
| | | Other | Reserved |

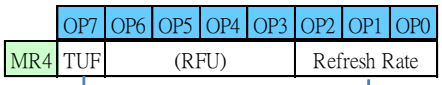
Note: Programmed value in nWR register is the number of clock cycles which determined when to start internal precharge operation for a write burst with AP enabled. It is determined by RU (tWR/tCK).

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR2 | (RFU) | | | | RL & WL | | | |

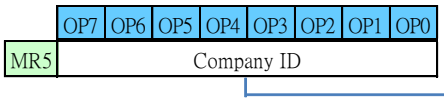
| | | | |
|---|---|---|---|
| Read latency and Write latency | Write-only | 0001 | RL3/WL1 (default) |
| | | 0010 | RL4/WL2 |
| | | 0011 | RL5/WL2 |
| | | 0100 | RL6/WL3 |
| | | 0101 | RL7/WL4 |
| | | 0110 | RL8/WL4 |
| | | Other | Reserved |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR3 | (RFU) | | | | DS | | | |

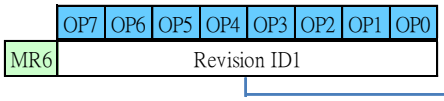
| | | | |
|---|---|---|---|
| Drive Strength | Write-only | 0000 | Reserved |
| | | 0001 | 34.3Ω typical |
| | | 0010 | 40Ω typical (default) |
| | | 0011 | 48Ω typical |
| | | 0100 | 60Ω typical |
| | | 0101 | reserved for 68.6Ω typical |
| | | 0110 | 80Ω typical |
| | | 0111 | 120Ω typical |
| | | Other | Reserved |



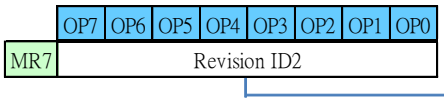

| | | | |
|---|---|---|---|
| Refresh Rate | Read-only | 000 | Reserved |
| | | 001 | Reserved |
| | | 010 | 2 × tREFI |
| | | 011 | 1 × tREFI |
| | | 100 | Reserved |
| | | 101 | 0.25 × tREFI, set to 85C, do not derate |
| | | 110 | 0.25 × tREFI, set to 95C, de-rate |
| | | 111 | temp>105C, set to 105C, stall |
| Temperature Update Flag | Read-only | 0 | OP<2:0> value has not changed since last read of MR4. |
| | | 1 | OP<2:0> value has changed since last read of MR4. |



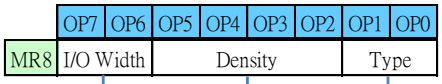

| | | | |
|---|---|---|---|
| Company ID | Read-only | 11111101 | AP Memory |




| | | | |
|---|---|---|---|
| Revision ID1 | Read-only | 00000000 | Version A |




| | | | |
|---|---|---|---|
| Revision ID2 | Read-only | 00000000 | Version A |




| | | | |
|---|---|---|---|
| Type | Read-only | **00** | **S4 SDRAM** |
| | | 01 | Reserved |
| | | 10 | Reserved |
| | | 11 | Reserved |
| Density | Read-only | 0010 | 256Mb |
| | | 0011 | 512Mb |
| | | **0100** | **1Gb** |
| | | 0101 | 2Gb |
| | | 0110 | 4Gb |
| | | 0111 | 8Gb |
| | | 1000 | 16Gb |
| | | 1001 | 32Gb |
| | | Other | Reserved |
| I/O Width | Read-only | 00 | x32 |
| | | 01 | x16 |
| | | 10 | x8 |
| | | 11 | Not used |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR9 | Vendor-Specific Test Mode | | | | | | | |

| | | | |
|---|---|---|---|
| Failed Die Bit[5] | Read-only | 0 | Pass (default) |
| | | 1 | Fail |
| Tested Die Bit [4] | Read-only | 0 | Reserved |
| | | 1 | Reserved |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR10 | Calibration Code | | | | | | | |

| | | | |
|---|---|---|---|
| Calibration Code | Write-only | hFF | Calibration command after initialization |
| | | hAB | Long calibration |
| | | h56 | Short calibration |
| | | hC3 | ZQ Reset |
| | | others | Reserved |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR16 | Bank Mask | | | | | | | |

| | | | |
|---|---|---|---|
| Bank [7:0] Mask | Write-only | 0 | Refresh enable to the bank (=unmasked, default) |
| | | 1 | Refresh blocked (=masked) |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR17 | Segment Mask | | | | | | | |

| | | | |
|---|---|---|---|
| Seg [7:0] Mask | Write-only | 0 | Refresh enable to the segment (=unmasked, default) |
| | | 1 | Refresh blocked (=masked) |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR32 | Calibration Pattern "A" | | | | | | | |

| | Bit Time 0 | Bit Time 1 | Bit Time 2 | Bit Time 3 |
|---|---|---|---|---|
| DQ outputs pattern A | 1 | 0 | 1 | 0 |

| | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| MR40 | Calibration Pattern "B" | | | | | | | |

| | Bit Time 0 | Bit Time 1 | Bit Time 2 | Bit Time 3 |
|---|---|---|---|---|
| DQ outputs pattern B | 0 | 0 | 1 | 1 |

### *8.3 Bank Activate Command [ACT]*

The bank activate command is issued by holding /CS low, CA0 low, and CA1 high at the rising edge of the clock. The bank addresses BA0, 1 & 2 are used to select the desired bank. The row address R0 through R12 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any read or write operation can be executed. Immediately after the Bank Active command, the LPDDR2 RAM can accept a read or write command on the following clock cycle at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another bank activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive bank activate commands to the same bank is determined by the /RAS cycle time of the device (tRC). The minimum time interval between successive bank activate commands to the different bank is determined by (tRRD).

[See Figure 19 in JEDEC Standard No. 209-2E]

### 8.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting /CS low, CA0 high, and CA1 low at the rising edge of the clock. CA2r must also be defined at this time to determine whether the access cycle is a read operation (CA2r high) or a write operation (CA2r low).

The LPDDR2 RAM provides a fast column access operation. A single read or write command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 8M bits x 16 I/O x 8 banks chip has a page length of 16384 bits (defined by C1 to C11). The page length of 16384 is divided into 4096, 2048, or 1024 for 16 bits burst respectively. A 4 bits or 8 bits or 16 bits burst operation will occur entirely within one of the 4096, 2048, or 1024 groups beginning with the column address supplied to the device during the read or write command (C1 to C11). The second, third and fourth access will also occur within this group segment. However, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bits burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, reads may be interrupted by reads and writes may be interrupted by writes provided that this occurs on a 4 bits boundary. The minimum CAS to CAS delay is defined by tCCD.

### 8.5 Burst Mode Operation

| | | | | | | | Burst cycle number and burst address sequence | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C3 (CA1f) | C2 (CA6r) | C1 (CA5r) | C0 (0) | BL | BT | WC | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| × | × | 0 | 0 | 4 | any | Wrap | 0 | 1 | 2 | 3 | | | | | | | | | | | | |
| × | × | 1 | 0 | | | | 2 | 3 | 0 | 1 | | | | | | | | | | | | |
| × | × | × | 0 | | any | NW*5 | y | y+1 | y+2 | y+3 | | | | | | | | | | | | |
| × | 0 | 0 | 0 | 8 | Seq | Wrap | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | |
| × | 0 | 1 | 0 | | | | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | | | | | | | | |
| × | 1 | 0 | 0 | | | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | | | | | | | | |
| × | 1 | 1 | 0 | | | | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | | | | | | | | |
| × | 0 | 0 | 0 | | Int | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | |
| × | 0 | 1 | 0 | | | | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 | | | | | | | | |
| × | 1 | 0 | 0 | | | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | | | | | | | | |
| × | 1 | 1 | 0 | | | | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 | | | | | | | | |
| 0 | 0 | 0 | 0 | 16 | Seq | Wrap | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0 | 0 | 1 | 0 | | | | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 |
| 0 | 1 | 0 | 0 | | | | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 |
| 0 | 1 | 1 | 0 | | | | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 |
| 1 | 0 | 0 | 0 | | | | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | 0 | 1 | 0 | | | | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 1 | 1 | 0 | 0 | | | | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B |
| 1 | 1 | 1 | 0 | | | | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D |

Remarks: NW: no wrap. Int: interleaved. Seq: sequential. Any: sequential or interleaved.
C3 = CA1f. C2 = CA6r. C1 = Ca5r. C0=0.
Notes:
C0 input is not present on CA bus. It is implied zero.
For BL = 4, the burst address represents C1 to C0.
For BL = 8, the burst address represents C2 to C0.
For BL = 16, the burst address represents C3 to C0.
Non-wrap, BL4, data-orders shown below are prohibited:
Not across full page boundary. (x16: 3FE, 3FF, 000, 001)
(x32: 1FE, 1FF, 000, 001)
Not across sub page boundary. (x16: 1FE, 1FF, 200, 201)

### *8.6 Burst Read Command [READ]*

The Burst Read command is initiated by having /CS low, CA0 high, CA1 high and CA2 low at the rising edge of the clock. The address inputs, CA5r to CA4r and CA1f to CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the read command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL + tDQSCK + tDQSQ after the rising edge of the clock where the read command is issued. The data strobe output (DQS) is driven low tRPRE before valid data (DQ) is driven onto the data bus.

The first bit of the burst is synchronized with the first rising edge of the data strobe (DQS). Each subsequent dataout appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is defined by mode register.

Pin timings are measured relative to the cross point of DQS and its complement, /DQS.

[See Figures 24, 25 in JEDEC Standard No. 209-2E]

[See Figure 33 in JEDEC Standard No. 209-2E]

The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU (tDQSCKmax/tCK) + BL/2 + 1 – WL. Note that if a read burst is interrupted with a Burst Terminate (BST) command, the effective BL of the interrupted read burst should be used to calculate the minimum read to write latency.

[See Figure 35 in JEDEC Standard No. 209-2E]

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 16 clocks for BL = 16 operation. This operation is allowed regardless of whether the same or different banks as long as the banks are activated.

Burst read can only be interrupted by another read with 4 bits burst boundary.

[See Figure 37 in JEDEC Standard No. 209-2E]

Notes:
Read burst interrupt function is only allowed on burst of 8 and 16.
Read burst interrupt may only occur on even clocks after the previous read commands provided that tCCD is met.
Reads can only be interrupted by other reads or the BST command.
Read burst interruption is allowed to any bank inside SDRAM.
Read burst with auto precharge is not allowed to be interrupted.
The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

### *8.7 Burst Write Command [WRIT]*

The Burst Write command is initiated by having /CS low, CA0 high, CA1 high and CA2 high at the rising edge of the clock. The address inputs determine the starting column address. The first valid datum is available Write Latency (WL) cycles + tDQSS from the rising edge of the clock from which the Write command is driven. A data strobe signal (DQS) should be driven low (preamble) nominally half clock prior to the data input. The first data bit of the burst cycle must be applied to the DQ pins tDS prior to the first rising edge of the DQS following the preamble. The subsequent burst bit data are sampled on successive edges of the DQS until the burst length is completed, which is 4, 8 or 16 bit burst.

tWR must be satisfied before a precharge command to the same bank may be issued after a burst write operation. Pin timings are measured relative to the crossing point of DQS and its complement, /DQS.

[See Figure 42 in JEDEC Standard No. 209-2E]

[See Figure 45 in JEDEC Standard No. 209-2E]

The minimum number of clocks from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU (tWTR/tCK)]. If a write burst is interrupted with a Burst Terminate (BST) command, the effective BL of the interrupted write burst should be used to calculate the minimum write to read latency.

[See Figure 47 in JEDEC Standard No. 209-2E]

The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL = 16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Burst write can only be interrupted by another write with 4 bits burst boundary, provided that tCCD is met.

[See Figure 49 in JEDEC Standard No. 209-2E]

Notes:
Write burst interrupt function is only allowed on burst of 8 and 16.
Write burst interrupt may only occur on even clocks after the previous write commands, provided that tCCD is met.
Writes can only be interrupted by other writes or the BST command.
Write burst interruption is allowed to any bank inside SDRAM.
Write burst with auto precharge is not allowed to be interrupted.

### *8.8 Write Data Mask*

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on LPDDR2 RAM.
DM can mask input data. By setting DM to low, data can be written. When DM is set to high, the corresponding data is not written, and the previous data is held.

The latency between DM input and enabling/disabling mask function is 0.

[See Figure 57 in JEDEC Standard No. 209-2E]

### *8.9 Precharge Command [PRE]*

The precharge command is used to precharge or close a bank that has been activated. The precharge command is initiated by having /CS low, CA0 high, CA1 high, CA2 low, and CA3 high at the rising edge of the clock. The precharge command can be used to precharge each bank independently or all banks simultaneously. Three address bits CA4r, CA7r and CA8r are used to define which bank to precharge when the command is issued.

| *CA4r* | *CA7r* | *CA8r* | *CA9r* | *Precharged bank(s)* |
|---|---|---|---|---|
| L | L | L | L | Bank 0 only |
| L | H | L | L | Bank 1 only |
| L | L | H | L | Bank 2 only |
| L | H | H | L | Bank 3 only |
| L | L | L | H | Bank 4 only |
| L | H | L | H | Bank 5 only |
| L | L | H | H | Bank 6 only |
| L | H | H | H | Bank 7 only |
| H | × | × | × | All banks |

Remark: H = $V_{IH}$, L = $V_{IL}$, × = $V_{IH}$ or $V_{IL}$

### 8.10 Burst Read Operation Followed by Precharge

For the earliest possible precharge, the precharge command may be issued on the rising edge of clock BL/2 clocks after a read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (tRP). A precharge command cannot be issued until tRAS is satisfied.

The minimum read to precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefretch of a read to precharge command. This time is called tRTP (Read to Precharge).

[See Figure 64 in JEDEC Standard No. 209-2E]

### 8.11 Burst Write Operation Followed by Precharge

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the precharge command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No precharge command should be issued prior to the tWR delay. Minimum Write to Precharge command spacing to the same bank is WL + BL/2 + RU (tWR/tCK) clock cycles. If the data burst is interrupted with a BST command, the effective BL shall be used to calculate the minimum Write to Precharge spacing.

[See Figure 67 in JEDEC Standard No. 209-2E]

### 8.12 Auto Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto precharge function. When a read or a write command is given to the LPDDR2 RAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If AP is low when the read or write command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If AP is high when the read or write command is issued, then the auto precharge function is engaged. During auto precharge on the rising edge which is Read Latency (RL) clock cycles before the end of the read burst.

Auto precharge can also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read latency) thus improving system performance for random data access.

### 8.13 Burst Read with Auto Precharge

If AP (CA0f) is high when a read command is issued, the read with auto precharge function is engaged. The LPDDR2 RAM starts an auto precharge operation on the rising edge of the clock BL/2 or RU (tRTP/tCK) cycles later than the read with AP command.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

The /RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

[See Figure 68 in JEDEC Standard No. 209-2E]

### 8.14 Burst Write with Auto Precharge

If AP (CA0f) is high when a write command is issued, the write with auto precharge function is engaged. The LPDDR2 RAM starts with an auto precharge operation on the rising edge of which is tWR cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

The data-in to bank activate delay time (tWR + tRP) has been satisfied.
The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

[See Figure 70 in JEDEC Standard No. 209-2E]

The LPDDR2 RAM supports the concurrent auto precharge feature, a read with auto precharge enabled, or a write with auto precharge enabled, may be followed by any column command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply. (E.G. Conflict between READ data and WRITE data must be avoided.)

The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below.

| *From command* | *To command (different bank, non-interrupting command)* | *Minimum delay (concurrent AP supported)* | *Units* |
|---|---|---|---|
| Read w/ AP | Read or Read w/ AP | BL/2 | tCK |
| | Write or Write w/ AP | (BL/2) + 2 | tCK |
| | Precharge or Activate | 1 | tCK |
| Write w/ AP | Read or Read w/ AP | WL + (BL/2) + tWTR | tCK |
| | Write or Write w/ AP | BL/2 | tCK |
| | Precharge or Activate | 1 | tCK |

The minimum delay from the read, write and precharge command to the precharge command to the same bank is summarized below.

| *From Command* | *To Command* | *Minimum delay between "From Command" to "To Command"* | *Units* | *Notes* |
|---|---|---|---|---|
| Read | Precharge (to same bank as Read) | (BL/2) + Max (2, RU (tRTP/tCK)) -2 | tCK | 1 |
| | Precharge all | (BL/2) + Max (2, RU (tRTP/tCK)) -2 | tCK | 1 |
| Read w/ AP | Precharge (to same bank as Read w/ AP) | (BL/2) + Max (2, RU (tRTP/tCK)) -2 | tCK | 1 |
| | Precharge all | (BL/2) + Max (2, RU (tRTP/tCK)) -2 | tCK | 1 |
| Write | Precharge (to same bank as Write) | WL + (BL/2) + tWTR | tCK | 1 |
| | Precharge all | WL + (BL/2) + tWTR | tCK | 1 |
| Write w/ AP | Precharge (to same bank as Write w/ AP) | WL + (BL/2) + tWTR | tCK | 1 |
| | Precharge all | WL + (BL/2) + tWTR | tCK | 1 |
| Precharge | Precharge (to same bank as precharge) | 1 | tCK | 1 |
| | Precharge all | 1 | tCK | 1 |
| Precharge All | Precharge | 1 | tCK | 1 |
| | Precharge all | 1 | tCK | 1 |

Notes:
For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.

### *8.15 The Burst Terminate [BST]*

The Burst Terminate (BST) command is initiated by having /CS low, CA0 high, CA1 high, CA2 low, and CA3 low at the rising edge of clock. The 4-bit prefetch architecture allows the BST command to be asserted on an even number of clock cycles after a write or read command. The BST command only affects the most recent read or write command. The latency of the BST command following a read command is equal to the Read Latency (RL). The latency of the BST command following

a Write command is equal to the Write Latency (WL). Therefore, the effective burst length of a Read or Write command interrupted by a BST command is an integer multiple of 4 and is defined as follows:

Effective BL = 2 × {Number of clocks from the read or write command to the BST command}

[See Figure 54 in JEDEC Standard No. 209-2E]

Burst Terminate interrupts the burst RL cycles after the BST command for reads. BST can only be issued an even number of clocks after the read command.

[See Figure 53 in JEDEC Standard No. 209-2E]

Burst Terminate interrupts the burst WL cycles after the BST command for writes. BST can only be issued an even number of clocks after the write command.

### *8.16 Refresh Command [REF]*

The Refresh command is initiated by having /CS low, CA0 low, CA1 low, and CA2 high at the rising edge of clock. All Bank Refresh is initiated by having CA3 high at the rising edge of clock.

For All Bank Refresh, all banks of the LPDDR2 RAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Refresh command (REF) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started. When the All Bank refresh cycle has completed, all banks of the LPDDR2 RAM will be in the precharged (idle) state. A delay between the Refresh Command (REF) and the next Activate command or subsequent Refresh command must be greater than or equal to the Refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given LPDDR2 RAM SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 × tREFI.

[See Figures 76, 77 in JEDEC Standard No. 209-2E]

### *8.17 Self-Refresh [SELF]*

The self-refresh command can be used to retain data in the LPDDR2 RAM, even if the rest of the system is powered down. When in the self-refresh mode, the LPDDR2 RAM retains data without external clocking. The LPDDR2 RAM device has a built-in timer to accommodate self-refresh operation. The self-refresh command is defined by having CKE low, /CS low, CA0 low, CA1 low, and CA2 high at the rising edge of the clock. CKE must be high during the previous clock cycle. Once the command is registered, CKE must be held low to keep the device in self-refresh model. Once the LPDDR2 RAM has entered self refresh mode, all of the external signals except CKE, are “don’t care”. For proper self-refresh operation, all power supply pins ($V_{DD1}$, $V_{DD2}$, $V_{DDQ}$ and $V_{REF}$) must be at valid levels. The SDRAM initiates a minimum of one refresh command internally within tCKE period once it enters self-refresh mode. The clock is internally disabled during self-refresh operation to save power. The minimum time that the LPDDR2 RAM must remain in self-refresh mode is tCKE. The user may change the external clock frequency or halt the external clock one clock after self-refresh entry is registered; however, the clock must be restarted and stable before the device can exit self-refresh operation.

The use of self-refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self-refresh mode. Upon exit from self-refresh, the LPDDR2 RAM requires a minimum of one extra auto refresh command before it is put back into self-refresh mode.

[See Figure 78 in JEDEC Standard No. 209-2E]

Note: Device must be in the “All banks idle” state prior to entering self refresh mode.

### *8.18 Mode Register Read Command*

The mode register read command is used to read configuration and status data from mode registers. The mode register read (MRR) command is initiated by having /CS low, CA0 low, CA1 low, CA2 low, and CA3 high at the rising edge of the clock. The mode register is selected by {CA1f to CA0f, CA9r to CA4r}. The mode register contents are available on the first data beat of DQ0 to DQ7, RL + tDQSCK + tDQSQ after the rising edge of the clock where the mode register read command is issued. Subsequent data beats contain valid, but undefined content. The MRR command has a burst length of four. The MRR command may not be interrupted by the BST command, MRR command or any other read command. The MRR command period (tMRR) is 2 clocks.

[See Figure 79 in JEDEC Standard No. 209-2E]

Notes:
Mode register read has a burst length of four.
Mode register read may not be interrupted by subsequent read, MRR, or BST command.
Mode register data is valid only on DQ0 to DQ7 on the first beat. Subsequent beats contain valid, but undefined data.
The mode register read command period (tMRR) is 2 clocks. No command (other than NOP or DESL) is allowed during this period.

### *8.19 Mode Register Write Command*

The mode register write command is used to write configuration data to mode registers. The mode register write (MRW) command is initiated by having /CS low, CA0 low, CA1 low, CA2 low, and CA3 low at the rising edge of the clock. The mode register is selected by {CA1f to CA0f, CA9r to CA4r}. The data to be written to the mode register is contained in CA9f to CA3f. The MRW command period is defined by tMRW.

The MRW may only be issued when all banks are in the idle pre-charge state or to issue a reset command.

The MRW command is also used to initiate the reset command. The reset command is allowed in both the Idle and row active states as well as the power on Initialization sequence and brings the device to the tRESET ($t_{INIT4}$) state in the power on Initialization sequence.

[[See Figure 84 in JEDEC Standard No. 209-2E]

Note: The mode register write command period (tMRW) is 5 clocks. No command (other than NOP or DESL) is allowed during this period.

### *8.20 Power-Down [PDEN]*

Power-down is synchronously entered when CKE is registered low and /CS high at the rising edge of clock. CKE is not allowed to go low while mode register read or write operations are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto precharge, or auto-refresh is in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in the following pages with details for entry into power-down.

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, /CK and CKE. In power-down mode, CKE low must be maintained at the inputs should be in a valid state but all other input signals are “Don’t Care”. CKE low must be maintained until tCKE has been satisfied. Maximum power-down duration is limited by the refresh requirements of the device, which allows a maximum of 9 tREFI if maximum posting of REF is utilized immediately before entering power-down.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or deselect command). CKE high must be maintained until tCKE has been satisfied.

[See Figure 91 in JEDEC Standard No. 209-2E]

The pattern shown below can repeat over a long period of time. With this pattern, LPDDR2 RAM guarantees all AC and DC timing, voltage specifications with temperature and voltage drift.

[See Figure 93 in JEDEC Standard No. 209-2E]

[See Figure 95 in JEDEC Standard No. 209-2E]

[See Figure 96 in JEDEC Standard No. 209-2E]

[See Figure 97 in JEDEC Standard No. 209-2E]

[See Figure 99 in JEDEC Standard No. 209-2E]

[See Figure 100 in JEDEC Standard No. 209-2E]

[See Figure 101 in JEDEC Standard No. 209-2E]

[See Figure 102 in JEDEC Standard No. 209-2E]

[[See Figure 103 in JEDEC Standard No. 209-2E]

[See Figure 104 in JEDEC Standard No. 209-2E]

### *8.21 Deep Power-Down [DPDEN]*

Deep power-down is synchronously entered when CKE is registered low with /CS low, CA0 high, CA1 high, and CA2 low at the rising edge of clock. In deep power-down mode, all input buffers except CKE, all output buffers, and the power to the array will be disabled. The contents of the SDRAM will be lost upon entry into deep power-down mode.

The deep power-down state is asynchronously exited when CKE is registered high with a stable clock input. The SDRAM must be fully re-initialized as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

[See Figure 105 in JEDEC Standard No. 209-2E]

### *8.22 Input Clock Stop and Frequency Change during Power-Down*

LPDDR2 RAM input clock frequency can be changed under following conditions:
LPDDR2 RAM is in power down mode.
CKE must be at logic low level.
A minimum of 2 clocks must be waited after CKE goes low before clock frequency may change

In order to reduce power, the input clock may be stopped during power down. When exiting power down, the clock must be stable prior to CKE going high.

SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, CKE must be held at stable low levels. Once input clock frequency is changed, stable new clocks must be provided to SDRAM before precharge power down may be exited. Depending on new clock frequency an additional MRW command may need to be issued to appropriately set the WR, RL and so on.

[See Figure 91 in JEDEC Standard No. 209-2E]

### *8.23 Clock Stop*

Stopping the clocks during idle periods is an effective way of reducing power consumption. In addition to clock stop during power-down states, LPDDR2 RAM also supports clock stop under the following conditions:

The last command (activate, read, write, precharge, mode register write, mode register read, refresh) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency.
The related timing conditions (tRCD, tWR, tRP, tMRR, tMRW, etc.) have been met.
CKE is held high.

When the above conditions have been met, the device is either in "idle state" or "row active" state and clock stop mode may be entered with CK held low and /CK held high.

Clock stop mode is exited by restarting the clock. At least one NOP command must be issued before the next command may be applied. Additional clock pulses might be required depending on the system characteristics.

[See Figure 91 in JEDEC Standard No. 209-2E]

### *8.24 No Operation Command [NOP]*

The no operation command (NOP) should be used in cases when the LPDDR2 RAM is in an idle or a wait state. The purpose of the no operation command is to prevent the LPDDR2 RAM from registering any unwanted commands between operations. NOP command is holding /CS low, CA0 high, CA1 high, and CA2 high at the rising edge of the clock. NOP command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

### *8.25 Deselect Command [DESL]*

The deselect command (DESL) performs the same function as a no operation command. DESL command occurs when /CS is brought high at the rising edge of the clock.

| Change History | | | |
|---|---|---|---|
| Rev. # | Who | When | What |
| 0.0 | Conan | 2017-07-14 | Initial Version |
| 0.1 | Conan | 2017-07-20 | updated IDD #s |
| 0.2 | HCLIN | 2017-08-22 | Updated temperature grade, added ordering information & package detail |
| 0.3 | Jecy | 2017-12-18 | Added operating junction temperature for KGD products |
| 0.4 | Jecy | 2018-04-09 | Updated ball assignment of 134b package |
| 0.5 | Jecy | 2018-04-24 | Updated tREFI specification |
| 0.6 | Lance | 2018-07-07 | modify temperature grade code of PN from XT to X |
| 0.7 | Lance | 2018-07-23 | modify idd spec |
| 0.8 | David | 2019-06-13 | add the current under 45 degree in section 2.6 |
| 1.1 | Jacky | 2020-02-19 | 1.modify from X16 v0.8<br>file : AD12 1Gb F-X LPDDR2 (v0.8 prelim).doc<br>2.Add information about X32.<br>3.Add Package Ball Assignment and Package Outline Drawing.<br>4.Add Bare die and X32 Part Number. |
| 1.1a | Jacky | 2020-04-27 | 1.Modify MR4's access of Mode Register Assignment from W to R.<br>2.Modify bit[4] tested Die of MR9 to Reserved. |
| 1.1b | Jacky | 2020-05-13 | 1.Added Power-off Sequence description. |