TISP7070H3SL THRU TISP7095H3SL, TISP7125H3SL THRU TISP7210H3SL
TISP7250H3SL THRU TISP7400H3SL
TRIPLE BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

MARCH 1999 - REVISED MARCH 2000

TELECOMMUNICATION SYSTEM 2x100 A 10/1000 OVERVOLTAGE PROTECTORS

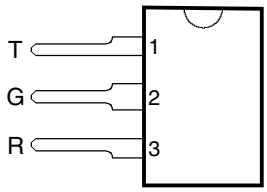
- **Ion-Implanted Breakdown Region**
  - Precise DC and Dynamic Voltages

DEVICE	V_{DRM} V	$V_{(BO)}$ V
‘7070	58	70
‘7080	65	80
‘7095	75	95
‘7125	100	125
‘7135	110	135
‘7145	120	145
‘7180	145	180
‘7210	160	210
‘7250	200	250
‘7290	230	290
‘7350	275	350
‘7400	300	400

- **Rated for International Surge Wave Shapes**
  - Single and Simultaneous Impulses

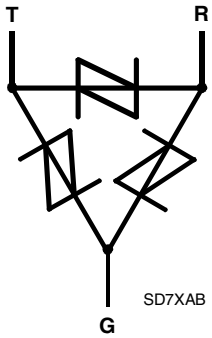
WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	GR-1089-CORE	500
8/20 µs	IEC 61000-4-5	350
10/160 µs	FCC Part 68	250
10/700 µs	FCC Part 68 ITU-T K20/21	200
10/560 µs	FCC Part 68	130
10/1000 µs	GR-1089-CORE	100

SL PACKAGE
(TOP VIEW)



MDXXAGA

device symbol



Terminals T, R and G correspond to the alternative line designators of A, B and C

- **3-Pin Through-Hole Packaging**
  - Compatible with TO-220AB pin-out
  - Low Height. . . . . .8.3 mm

description

The TISP7xxxH3SL limits overvoltages between the telephone line Ring and Tip conductors and Ground. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line.

Each terminal pair, T-G, R-G and T-R, has a symmetrical voltage-triggered bidirectional thyristor protection characteristic. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

This TISP7xxxH3SL range consists of twelve voltage variants to meet various maximum system voltage levels (58 V to 300 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These high current protection devices are in a 3-pin single-in-line (SL) plastic package and are supplied in tube pack. For alternative impulse rating, voltage and holding current values in SL packaged protectors, consult the factory. For lower rated impulse currents in the SL package, the 45 A 10/1000 TISP7xxxF3SL series is available.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation

absolute maximum ratings, T_A = 25°C (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, (see Note 1)	'7070	V_{DRM}	± 58	V
	'7080		± 65	
	'7095		± 75	
	'7125		±100	
	'7135		±110	
	'7145		±120	
	'7180		±145	
	'7210		±160	
	'7250		±200	
	'7290		±230	
	'7350		±275	
	'7400		±300	
Non-repetitive peak on-state pulse current (see Notes 2, and 3)		I_{TSP}		A
2/10 (Telcordia GR-1089-CORE, 2/10 voltage wave shape)			500	
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage, 8/20 current combination wave generator)			350	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)			250	
4/250 (ITU-T K.20/21, 10/700 voltage wave shape, dual)			225	
0.2/310 (CNET I 31-24, 0.5/700 voltage wave shape)			200	
5/310 (ITU-T K.20/21, 10/700 voltage wave shape, single)			200	
5/320 µs (FCC Part 68, 9/720 µs voltage wave shape)			200	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)			130	
10/1000 (Telcordia GR-1089-CORE, 10/1000 voltage wave shape)			100	
Non-repetitive peak on-state current (see Notes 2, 3 and 4)		I_{TSM}		A
20 ms (50 Hz) full sine wave			55	
16.7 ms (60 Hz) full sine wave			60	
1000 s 50 Hz/60 Hz a.c.			0.9	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. Derate value at -0.13%/°C for temperatures below 25 °C.
2. Initially the TISP7xxxH3 must be in thermal equilibrium.
3. These non-repetitive rated currents are peak values of either polarity. The rated current values may be applied to any terminal pair. Additionally, both R and T terminals may have their rated current values applied simultaneously (in this case the G terminal return current will be the sum of the currents applied to the R and T terminals). The surge may be repeated after the TISP7xxxH3 returns to its initial conditions.
4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C

electrical characteristics for any terminal pair, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25°C			±5	µA
			T_A = 85°C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'7070			±70	V
			'7080			±80	
			'7095			±95	
			'7125			±125	
			'7135			±135	
			'7145			±145	
			'7180			±180	
			'7210			±210	
			'7250			±250	
			'7290			±290	
			'7350			±350	
			'7400			±400	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V, di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'7070			±78	V
			'7080			±88	
			'7095			±103	
			'7125			±134	
			'7135			±144	
			'7145			±154	
			'7180			±189	
			'7210			±220	
			'7250			±261	
			'7290			±302	
			'7350			±362	
			'7400			±414	
$I_{(BO)}$	Breakover current	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω		±0.1		±0.8	A
V_T	On-state voltage	I_T = ±5 A, t_W = 100 µs				±5	V
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15		±0.6	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85°C			±10	µA
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = 0,	'7070 thru '7095			170	pF
			'7125 thru '7210			90	
			'7250 thru '7400			84	
		f = 1 MHz, V_d = 1 V rms, V_D = -1 V	'7070 thru '7095			150	
			'7125 thru '7210			79	
			'7250 thru '7400			67	
		f = 1 MHz, V_d = 1 V rms, V_D = -2 V	'7070 thru '7095			140	
			'7125 thru '7210			74	
			'7250 thru '7400			62	
		f = 1 MHz, V_d = 1 V rms, V_D = -50 V	'7070 thru '7095			73	
			'7125 thru '7210			35	
			'7250 thru '7400			28	
		f = 1 MHz, V_d = 1 V rms, V_D = -100 V (see Note 5)	'7125 thru '7210			33	
			'7250 thru '7400			26	

NOTE 5: To avoid possible voltage clipping, the '7125 is tested with V_D = -98 V.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 6)			50	°C/W

NOTE 6: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

PARAMETER MEASUREMENT INFORMATION

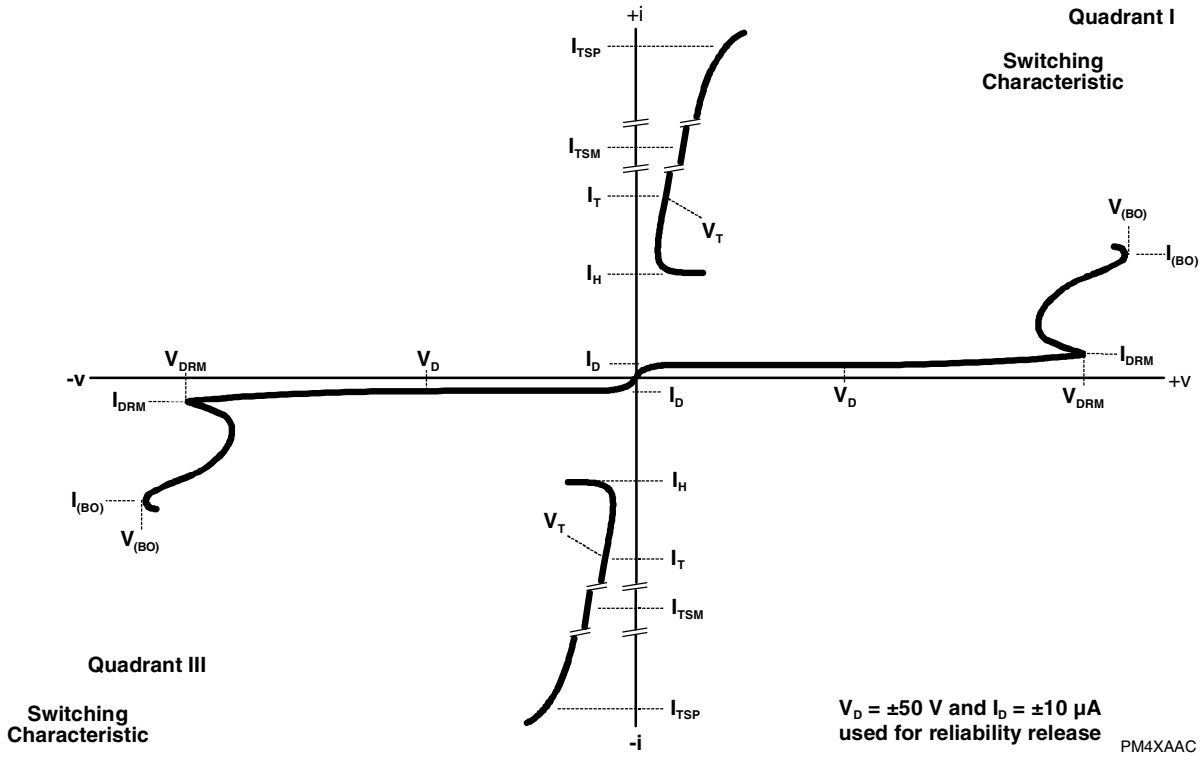


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR TERMINAL PAIRS

TYPICAL CHARACTERISTICS

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

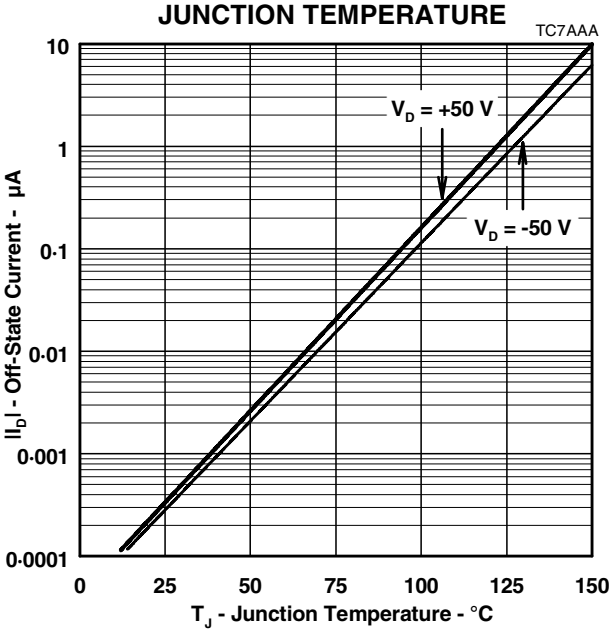


Figure 2.

NORMALISED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

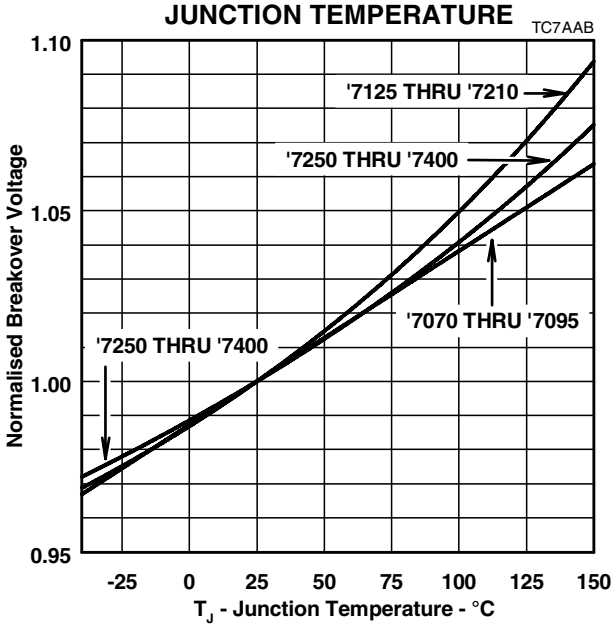


Figure 3.

NORMALISED BREAKOVER CURRENT vs JUNCTION TEMPERATURE

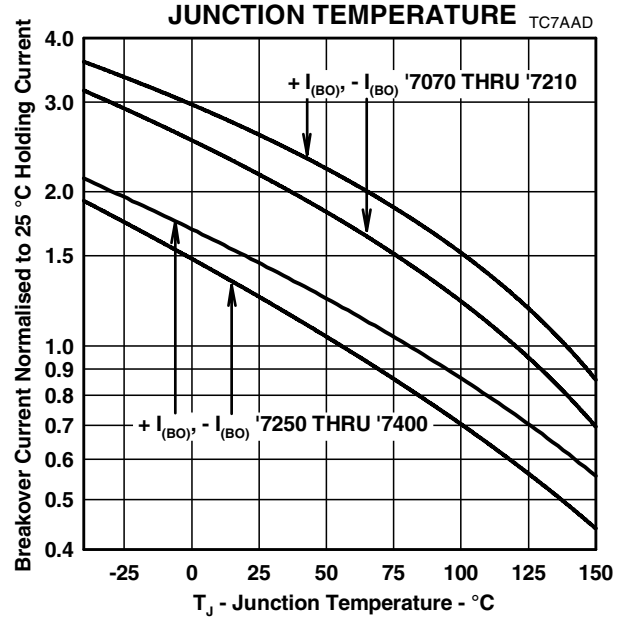


Figure 4.

NORMALISED HOLDING CURRENT vs JUNCTION TEMPERATURE

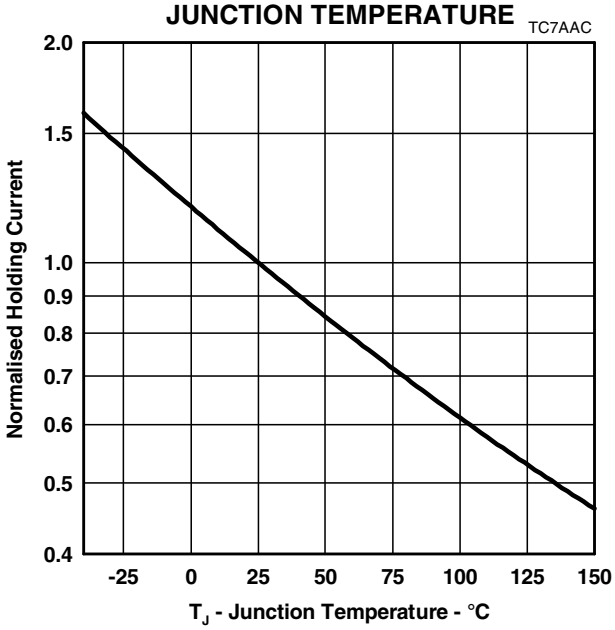


Figure 5.

TYPICAL CHARACTERISTICS

NORMALISED CAPACITANCE vs OFF-STATE VOLTAGE

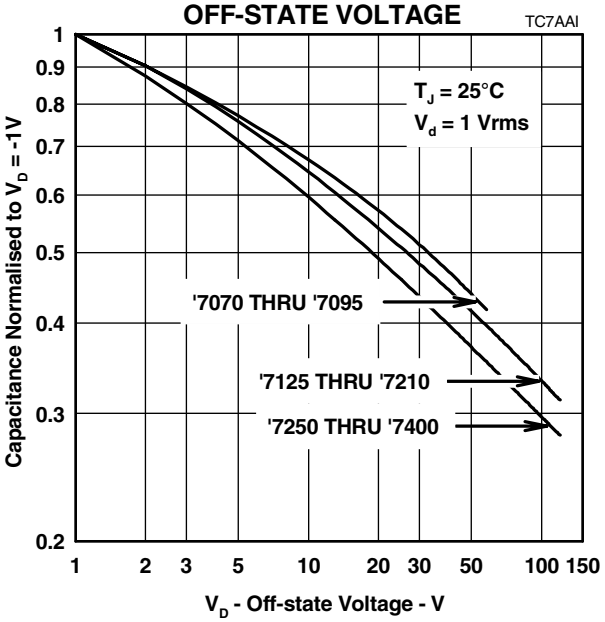


Figure 6.

DIFFERENTIAL OFF-STATE CAPACITANCE vs RATED REPETITIVE PEAK OFF-STATE VOLTAGE

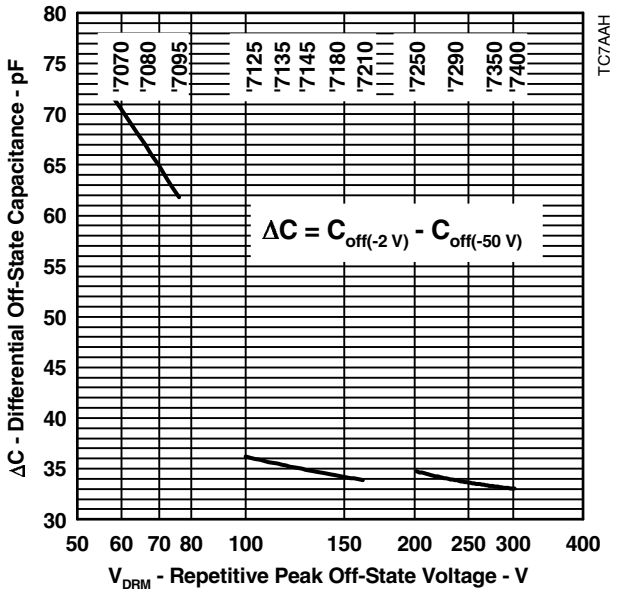


Figure 7.

RATING AND THERMAL INFORMATION

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

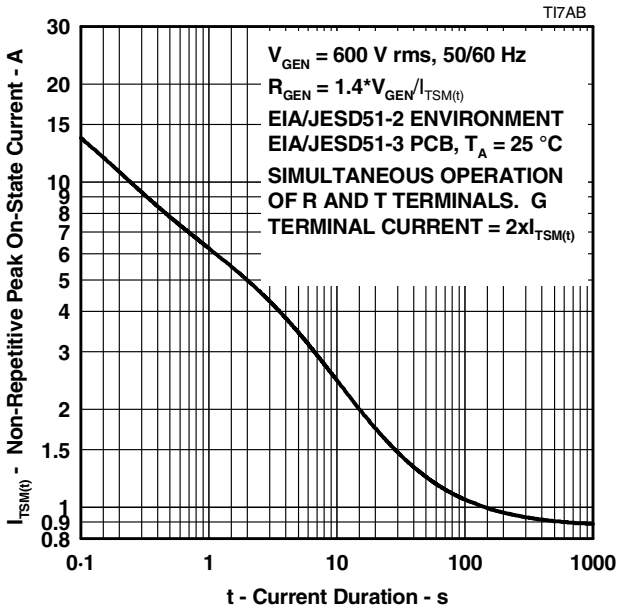


Figure 8.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

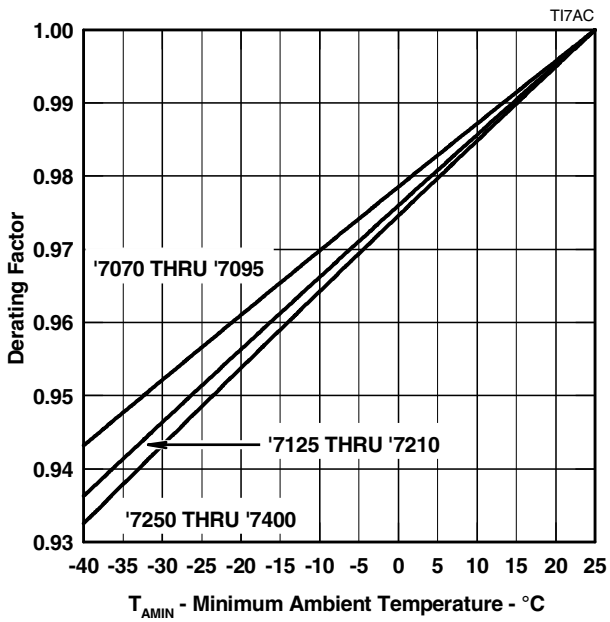


Figure 9.

IMPULSE RATING vs AMBIENT TEMPERATURE

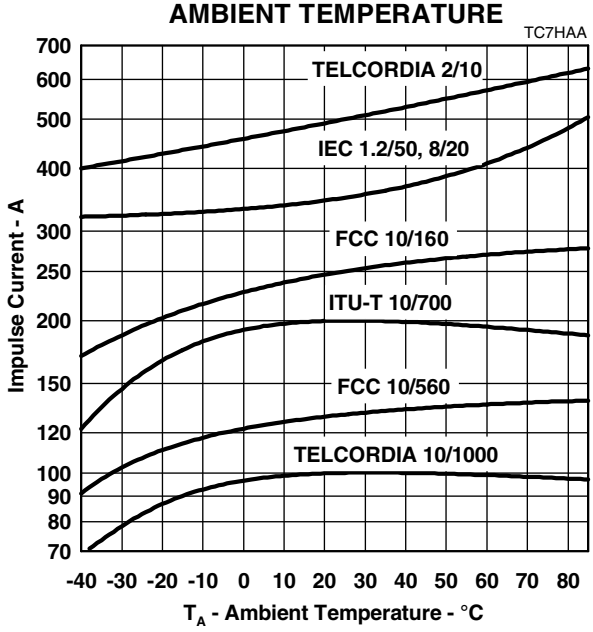


Figure 10.

PRODUCT INFORMATION

APPLICATIONS INFORMATION

deployment

These devices are three terminal overvoltage protectors. They limit the voltage between three points in the circuit. Typically, this would be the two line conductors and protective ground (Figure 11).

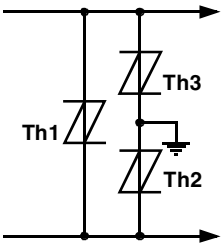


Figure 11. MULTI-POINT PROTECTION

In Figure 11, protectors Th2 and Th3 limit the maximum voltage between each conductor and ground to the $\pm V_{(BO)}$ of the individual protector. Protector Th1 limits the maximum voltage between the two conductors to its $\pm V_{(BO)}$ value.

Manufacturers are being increasingly required to design in protection coordination. This means that each protector is operated at its design level and currents are diverted through the appropriate protector e.g. the primary level current through the primary protector and lower levels of current may be diverted through the secondary or inherent equipment protection. Without coordination, primary level currents could pass through the equipment only designed to pass secondary level currents. To ensure coordination happens with fixed voltage protectors, some resistance is normally used between the primary and secondary protection. The values given in this data sheet apply to a 400 V (d.c. sparkover) gas discharge tube primary protector and the appropriate test voltage when the equipment is tested with a primary protector.

impulse testing

To verify the withstand capability and safety of the equipment, standards require that the equipment is tested with various impulse wave forms. The table below shows some common values.

STANDARD	PEAK VOLTAGE SETTING V	VOLTAGE WAVE FORM µs	PEAK CURRENT VALUE A	CURRENT WAVE FORM µs	TISP7xxxH3 25 °C RATING A	SERIES RESISTANCE Ω	COORDINATION RESISTANCE Ω (MIN).
GR-1089-CORE	2500	2/10	500	2/10	500	0	NA
	1000	10/1000	100	10/1000	100		
FCC Part 68 (March 1998)	1500	10/160	200	10/160	250	0	NA
	800	10/560	100	10/560	130		
	1000	9/720 †	25	5/320 †	200		
	1500	(SINGLE)	37.5	5/320 †	200		
	1500	(DUAL)	2 x 27	4/250	2 x 225		
I 31-24	1500	0.5/700	37.5	0.2/310	200	0	NA
ITU-T K20/K21	1000	10/700	25	5/310	200	0	NA
	1500	(SINGLE)	37.5	5/310	200		NA
	4000	(SINGLE)	100	5/310	200		4.5
	4000	(DUAL)	2 x 72	4/250	2 x 225		6.0

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K21 10/700 impulse generator

NA = Not Applicable, primary protection removed or not specified.

If the impulse generator current exceeds the protectors current rating then a series resistance can be used to reduce the current to the protectors rated value and so prevent possible failure. The required value of series resistance for a given waveform is given by the following calculations. First, the minimum total circuit impedance is found by dividing the impulse generators peak voltage by the protectors rated current. The impulse generators fictive impedance (generators peak voltage divided by peak short circuit current) is then subtracted from the minimum total circuit impedance to give the required value of series resistance. In some cases the equipment will require verification over a temperature range. By using the rated waveform values from Figure 10, the appropriate series resistor value can be calculated for ambient temperatures in the range of -40 °C to 85 °C.

a.c. power testing

The protector can withstand the G return currents applied for times not exceeding those shown in Figure 8. Currents that exceed these times must be terminated or reduced to avoid protector failure. Fuses, PTC (Positive Temperature Coefficient) resistors and fusible resistors are overcurrent protection devices which can be used to reduce the current flow. Protective fuses may range from a few hundred milliamperes to one ampere. In some cases it may be necessary to add some extra series resistance to prevent the fuse opening during impulse testing. The current versus time characteristic of the overcurrent protector must be below the line shown in Figure 8. In some cases there may be a further time limit imposed by the test standard (e.g. UL 1459 wiring simulator failure).

capacitance

The protector characteristic off-state capacitance values are given for d.c. bias voltage, V_D, values of 0, -1 V, -2 V and -50 V. Where possible values are also given for -100 V. Values for other voltages may be calculated by multiplying the V_D = 0 capacitance value by the factor given in Figure 6. Up to 10 MHz the capacitance is essentially independent of frequency. Above 10 MHz the effective capacitance is strongly dependent on connection inductance. For example, a printed wiring (PW) trace of 10 cm could create a circuit resonance with the device capacitance in the region of 50 MHz. In many applications, the typical conductor bias voltages will be about -2 V and -50 V. Figure 7 shows the differential (line unbalance) capacitance caused by biasing one protector at -2 V and the other at -50 V.

normal system voltage levels

The protector should not clip or limit the voltages that occur in normal system operation. For unusual conditions, such as ringing without the line connected, some degree of clipping is permissible. Under this condition, about 10 V of clipping is normally possible without activating the ring trip circuit.

Figure 9 allows the calculation of the protector V_{DRM} value at temperatures below 25 °C. The calculated value should not be less than the maximum normal system voltages. The TISP3290H3, with a V_{DRM} of 220 V, can be used for the protection of ring generators producing 105 V rms of ring on a battery voltage of -58 V. The peak ring voltage will be 58 + 1.414*105 = 206.5 V. However, this is the open circuit voltage and the connection of the line and its equipment will reduce the peak voltage.

For the extreme case of an unconnected line, the temperature at which clipping begins can be calculated using the data from Figure 9. To possibly clip, the V_{DRM} value has to be 206.5 V. This is a reduction of the 220 V 25 °C V_{DRM} value by a factor of 206.5/220 = 0.94. Figure 9 shows that a 0.94 reduction will occur at an ambient temperature of -32 °C. In this example, the TISP3290H3 will allow normal equipment operation, even on an open-circuit line, provided that the minimum expected ambient temperature does not fall below -32 °C.

JESD51 thermal measurement method

To standardise thermal measurements, the EIA (Electronic Industries Alliance) has created the JESD51 standard. Part 2 of the standard (JESD51-2, 1995) describes the test environment. This is a 0.0283 m^3 (1 ft^3) cube which contains the test PCB (Printed Circuit Board) horizontally mounted at the centre. Part 3 of the

standard (JESD51-3, 1996) defines two test PCBs for surface mount components; one for packages smaller than 27 mm on a side and the other for packages up to 48 mm. The thermal measurements used the smaller 76.2 mm x 114.3 mm (3.0 " x 4.5 ") PCB. The JESD51-3 PCBs are designed to have low effective thermal conductivity (high thermal resistance) and represent a worse case condition. The PCBs used in the majority of applications will achieve lower values of thermal resistance and so can dissipate higher power levels than indicated by the JESD51 values.

typical circuits

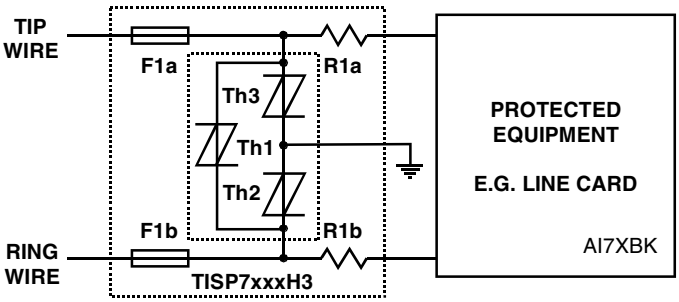


Figure 12. PROTECTION MODULE

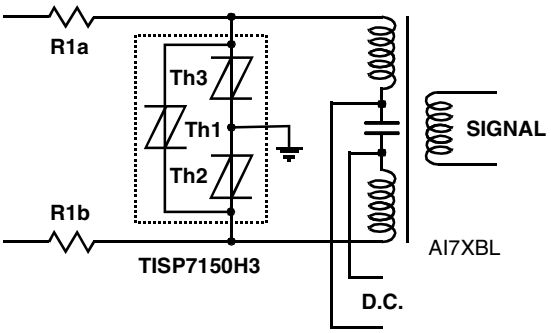


Figure 13. ISDN PROTECTION

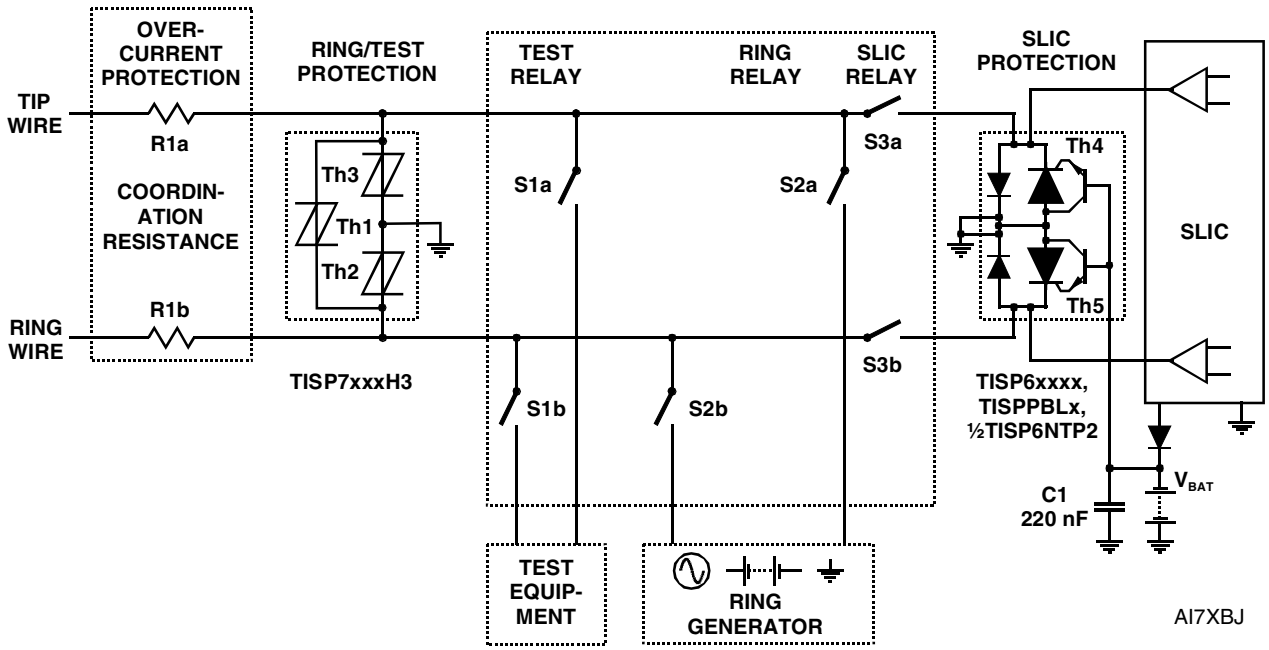


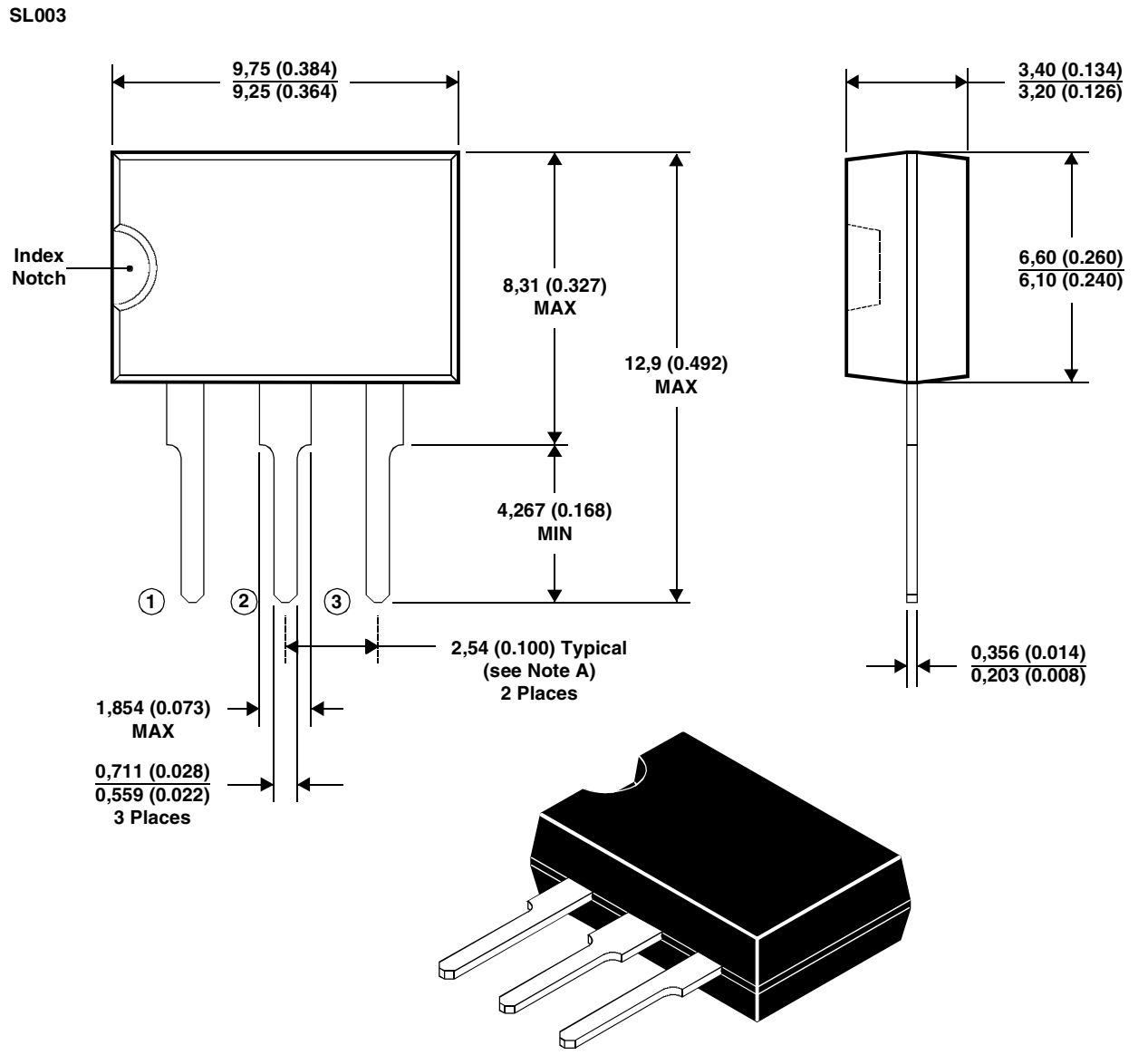
Figure 14. LINE CARD RING/TEST PROTECTION

MECHANICAL DATA

SL003

3-pin plastic single-in-line package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



ALL LINEAR DIMENSIONS IN MILLIMETERS AND PARANTHETICALLY IN INCHES

MDXXCEA

NOTES: A. Each pin centreline is located within 0,25 (0.010) of its true longitudinal position.
B. Body molding flash of up to 0,15 (0.006) may occur in the package lead plane.

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