

June 1997 Revised April 1999

## 74VHCT138A 3-to-8 Decoder/Demultiplexer

## **General Description**

The VHCT138A is an advanced high speed CMOS 3-to-8 DECODER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs  $(A_0, A_1 \text{ and } A_2)$  determine which one of the outputs  $(\overline{O}_0 - \overline{O}_7)$  will go LOW. When enable input  $E_3$  is held LOW or either  $\overline{E}_1$  or  $\overline{E}_2$  is held HIGH, decoding function is inhibited and all outputs go HIGH.  $E_3$ ,  $\overline{E}_1$  and  $\overline{E}_2$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems. Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the sup-

ply voltage and to the output pins with  $V_{CC}=0$ V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

#### **Features**

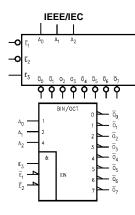
- High Speed:  $t_{PD} = 7.6$  ns (typ) at  $V_{CC} = 5V$
- $\blacksquare$  Low power dissipation:  $I_{CC}=4~\mu\text{A}$  (max.) at  $T_A=25^{\circ}\text{C}$
- Power down protection is provided on all inputs and
- Pin and function compatible with 74HCT138

## **Ordering Code:**

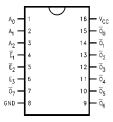
Order Number	Package Number	Package Description
74VHCT138AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74VHCT138ASJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT138AMTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT138AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## **Logic Symbols**



#### **Connection Diagram**



## **Pin Descriptions**

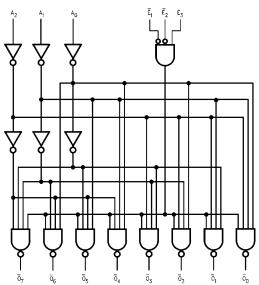
Pin Names	Description
A <sub>0</sub> -A <sub>2</sub>	Address Inputs
$\overline{E}_1 - \overline{E}_2$	Enable Inputs
E <sub>3</sub>	Enable Input
$\overline{O}_0 - \overline{O}_7$	Outputs

## **Truth Table**

Inputs					Outputs									
Ē <sub>1</sub>	E <sub>2</sub>	E <sub>3</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	O <sub>0</sub>	$\overline{O}_0$ $\overline{O}_1$ $\overline{O}_2$ $\overline{O}_3$ $\overline{O}_4$ $\overline{O}_5$ $\overline{O}_6$ $\overline{O}_7$							
Н	Х	Х	Χ	Χ	Χ	Н	Н	Н	Н	Н	Н	Н	Н	
Х	Н	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н	
Х	Х	L	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н	
L	L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	
L	L	Н	Н	L	L	Н	L	Н	Н	Н	Н	Н	Н	
L	L	Н	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	
L	L	Н	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н	
L	L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	

$$\begin{split} & H = \text{HIGH Voltage Level} \\ & L = \text{LOW Voltage Level} \\ & X = \text{Immaterial} \end{split}$$

# **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## **Absolute Maximum Ratings**(Note 1)

# Recommended Operating Conditions (Note 5)

 $\begin{tabular}{lll} Supply Voltage (V_{CC}) & -0.5V to +7.0V \\ DC Input Voltage (V_{IN}) & -0.5V to +7.0V \\ \end{tabular}$ 

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>) 4.5V to +5.5V Input Voltage (V<sub>IN</sub>) 0V to +5.5V

DC Output Voltage (V<sub>OUT</sub>)

-0.5V to 7.0V Output Voltage (V<sub>OUT</sub>)

(Note 2) (Note 3)

-0.5V to V<sub>CC</sub>+ 0.5V (Note 3)

(Note 3)  $0V \text{ to } V_{CC}$  (Note 2) 0V to 5.5V

Input Diode Current ( $I_{IK}$ ) Output Diode Current ( $I_{OK}$ )

Operating Temperature (T<sub>OPR</sub>)

0V to 5.5V -40°C to +85°C

Output Diode Current (I<sub>OK</sub>)
(Note 4)

 $\pm 20$  mA Input Rise and Fall Time ( $t_{\rm r},\,t_{\rm f}$ )

DC Output Current (I<sub>OUT</sub>)

(Soldering, 10 seconds)

 $\pm 25 \text{ mA}$   $V_{CC} = 5.0 \text{V} \pm 0.5 \text{V}$ 

0 ~ 20 ns/V

DC  $V_{CC}$ /GND Current ( $I_{CC}$ ) Storage Temperature ( $T_{STG}$ ) Lead Temperature ( $T_L$ ) ±75 mA
-65°C to +150°C

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

260°C ables tions.

-20 mA

**Note 2:** V<sub>CC</sub> = 0V.

Note 3: HIGH or LOW state.  $I_{\rm OUT}$  absolute maximum rating must be

observed.

Note 4:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$  (Outputs Active).

Note 5: Unused inputs must be held HIGH or LOW. They may not float.

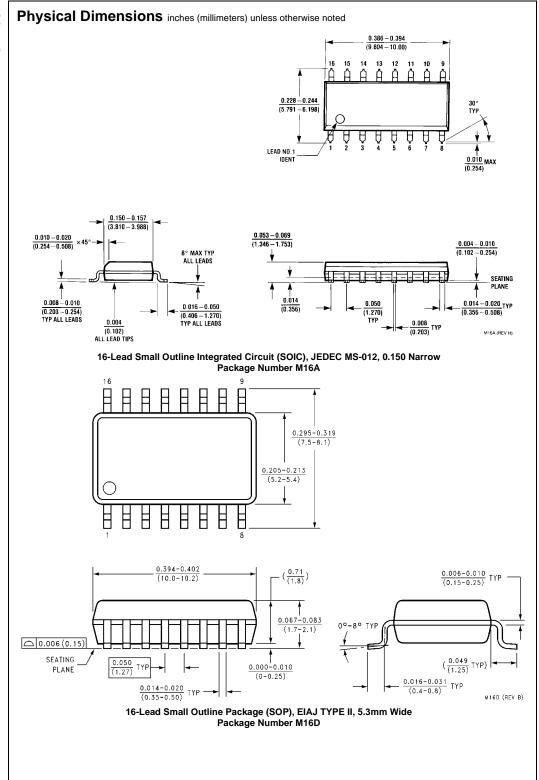
## **DC Electrical Characteristics**

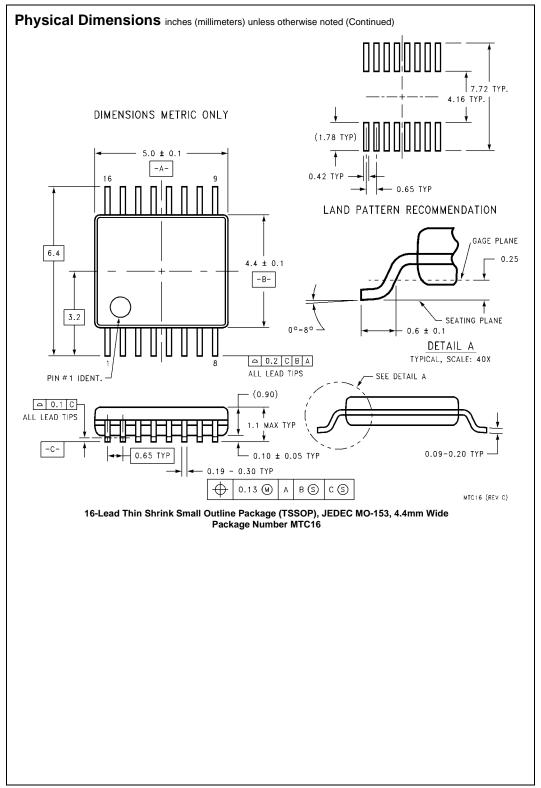
Symbol	Parameter	V <sub>cc</sub>	T <sub>A</sub> = 25°C			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	
Symbol	raiametei	(V)	Min	Тур	Max	Min	Max	Ullits	Conditions	
V <sub>IH</sub>	HIGH Level Input Voltage	4.5 – 5.5	2.0			2.0		V		
V <sub>IL</sub>	LOW Level Input Voltage	4.5 – 5.5			0.8		0.8	V		
V <sub>OH</sub>	HIGH Level	4.5	4.4	4.5		4.4		V	$V_{IN} = V_{IH}$ $I_{OH} = -50 \mu A$	
	Output Voltage	4.5	3.94			3.80		· ·	or $V_{IL}$ $I_{OH} = -8 \text{ mA}$	
V <sub>OL</sub>	LOW Level	4.5		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ $I_{OL} = 50 \mu A$	
	Output Voltage	4.5			0.36		0.44	•	or $V_{IL}$ $I_{OL} = 8 \text{ mA}$	
I <sub>IN</sub>	Input Leakage Current	0 – 5.5			±0.1		±1.0	μΑ	V <sub>IN</sub> = 5.5V or GND	
I <sub>CC</sub>	Quiescent Supply Current	5.5			4.0		20.0	μΑ	$V_{IN} = V_{CC}$ or GND	
Гсст	Maximum I <sub>CC/Input</sub>	5.5			1.35		1.50	mA	$V_{in} = 3.4V$ other inputs = $V_{CC}$ or GND	
I <sub>OFF</sub>	Output Leakage Current	0			0.5		5.0	μΑ	V <sub>OUT</sub> = 5.5V	

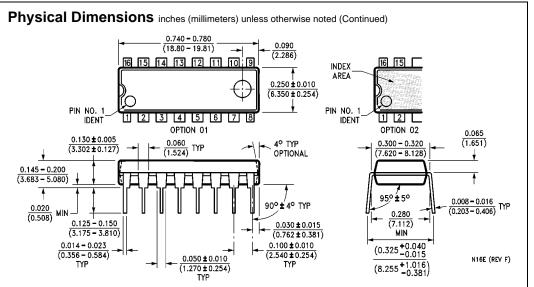
## **AC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	$T_A = 25^{\circ}C$			$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions
			Min	Тур	Max	Min	Max	Omis	Conditions
t <sub>PLH</sub>	Propagation Delay	$5.0 \pm 0.5$		7.6	10.4	1.0	12.0	no	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	$A_n$ to $\overline{O}_n$			8.1	11.4	1.0	13.0	ns	C <sub>L</sub> = 50 pF
t <sub>PLH</sub>	Propagation Delay	$5.0 \pm 0.5$		6.6	9.1	1.0	10.5	no	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	E <sub>3</sub> to $\overline{O}_n$			7.1	10.1	1.0	11.5	ns	C <sub>L</sub> = 50 pF
t <sub>PLH</sub>	Propagation Delay	$5.0 \pm 0.5$		7.0	9.6	1.0	11.0	no	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$			7.5	10.6	1.0	12.0	ns	C <sub>L</sub> = 50 pF
C <sub>IN</sub>	Input Capacitance			4	10		10	pF	V <sub>CC</sub> = Open
C <sub>PD</sub>	Power Dissipation Capacitance			49				pF	(Note 6)

Note 6:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC}$  (opr.) =  $C_{PD}$  \*  $V_{CC}$  \*  $f_{IN}$  +  $I_{CC}$ .







16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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