

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT670** 4 x 4 register file; 3-state

Product specification  
File under Integrated Circuits, IC06

December 1990

## 4 x 4 register file; 3-state

## 74HC/HCT670

## FEATURES

- Simultaneous and independent read and write operations
- Expandable to almost any word size and bit length
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT670 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT670 are 16-bit 3-state register files organized as 4 words of 4 bits each. Separated read and write address inputs (R<sub>A</sub>, R<sub>B</sub> and W<sub>A</sub>, W<sub>B</sub>) and enable inputs (R<sub>E</sub> and W<sub>E</sub>) are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs (D<sub>0</sub> to D<sub>3</sub>). The W<sub>A</sub> and W<sub>B</sub> inputs determine

the location of the stored word. When the  $\overline{W_E}$  input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the  $\overline{W_E}$  input is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs (Q<sub>0</sub> to Q<sub>3</sub>). D<sub>n</sub> and W<sub>n</sub> inputs are inhibited when  $\overline{W_E}$  is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual read address inputs (R<sub>A</sub> and R<sub>B</sub>). The addressed word appears at the four outputs when the  $\overline{R_E}$  is LOW. Data outputs are in the high impedance OFF-state when  $\overline{R_E}$  is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Design of the read enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the enable and address inputs of each device in parallel.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	23	23	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	122	124	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \quad \text{where:}$$

f<sub>i</sub> = input frequency in MHz  
 f<sub>o</sub> = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>;  
 for HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
5, 4	R <sub>A</sub> , R <sub>B</sub>	read address inputs
8	GND	ground (0 V)
10, 9, 7, 6	Q <sub>0</sub> to Q <sub>3</sub>	data outputs
11	$\overline{RE}$	3-state output read enable input (active LOW)
12	$\overline{WE}$	write enable input (active LOW)
14, 13	W <sub>A</sub> , W <sub>B</sub>	write address inputs
15, 1, 2, 3	D <sub>0</sub> to D <sub>3</sub>	data inputs
16	V <sub>CC</sub>	positive supply voltage

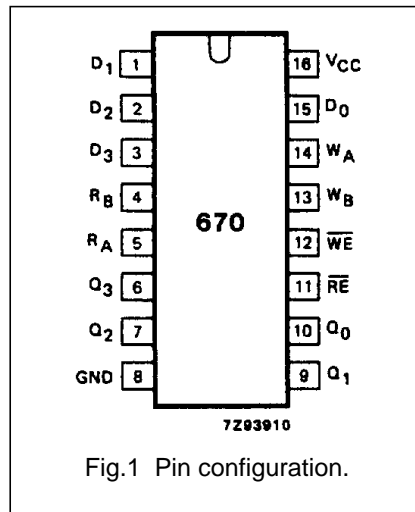


Fig.1 Pin configuration.

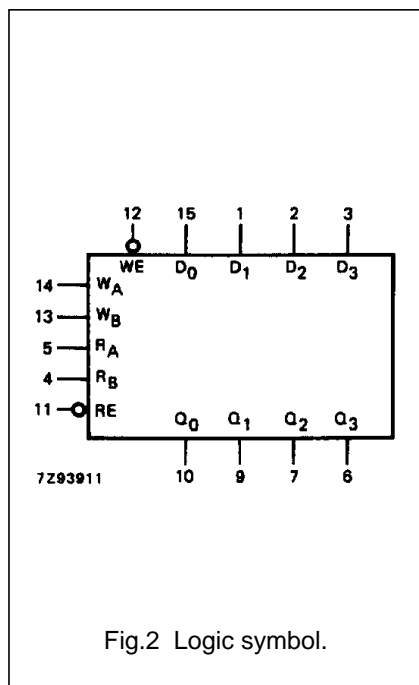


Fig.2 Logic symbol.

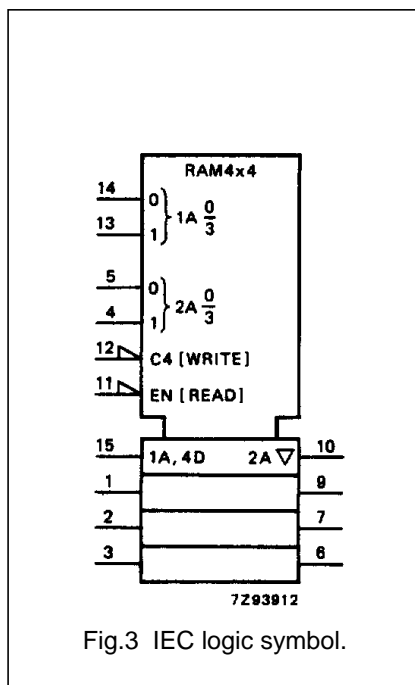


Fig.3 IEC logic symbol.

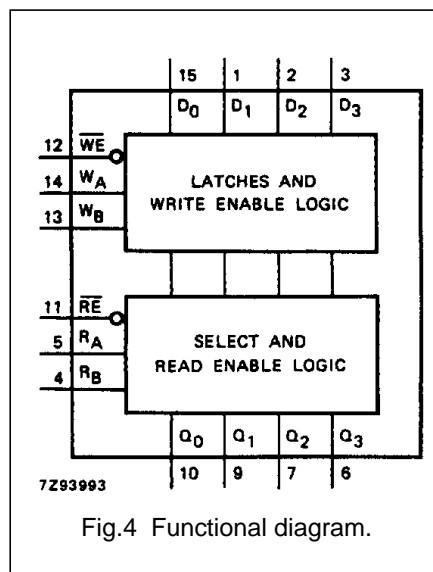


Fig.4 Functional diagram.

WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES <sup>(1)</sup>
	$\overline{WE}$	D <sub>n</sub>	
write data	L	L	L
	L	H	H
data latched	H	X	no change

Note

- The write address (W<sub>A</sub> and W<sub>B</sub>) to the "internal latches" must be stable while  $\overline{WE}$  is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT
	$\overline{RE}$	INTERNAL LATCHES <sup>(1)</sup>	
read	L	L	L
	L	H	H
disabled	H	X	Z

Notes

- The selection of the "internal latches" by read address (R<sub>A</sub> and R<sub>B</sub>) are not constrained by  $\overline{WE}$  or  $\overline{RE}$  operation.  
 H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 Z = high impedance OFF-state

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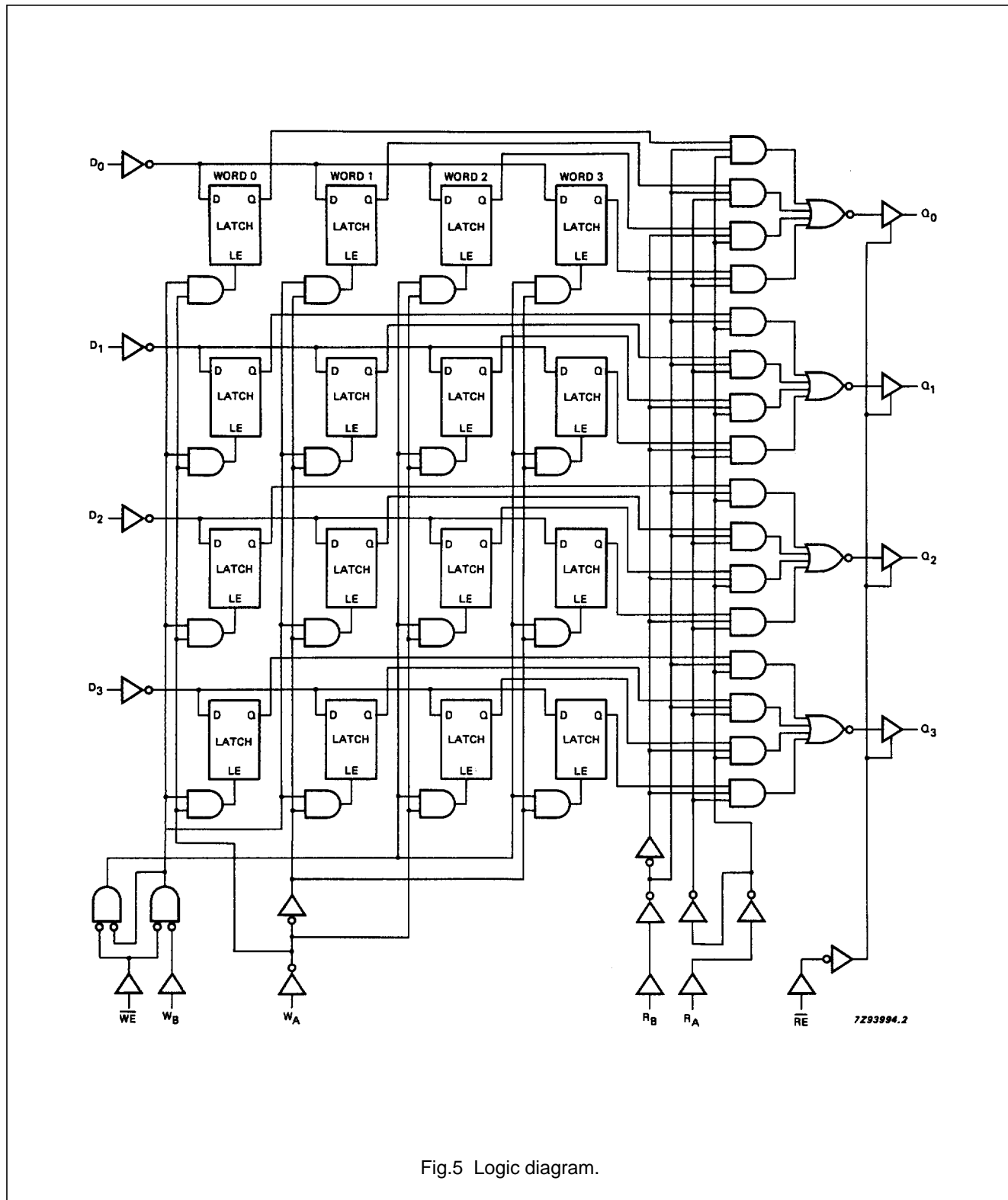


Fig.5 Logic diagram.

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay R <sub>A</sub> , R <sub>B</sub> to Q <sub>n</sub>		58 21 17	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{WE}$ to Q <sub>n</sub>		77 28 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		74 27 22	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{RE}$ to Q <sub>n</sub>		39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{RE}$ to Q <sub>n</sub>		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	write enable pulse width LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time D <sub>n</sub> to $\overline{WE}$	60 12 10	3 1 1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time W <sub>A</sub> , W <sub>B</sub> to $\overline{WE}$	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t <sub>h</sub>	hold time D <sub>n</sub> to $\overline{WE}$	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
t <sub>h</sub>	hold time W <sub>A</sub> , W <sub>B</sub> to $\overline{WE}$	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
t <sub>latch</sub>	latch time $\overline{WE}$ to R <sub>A</sub> , R <sub>B</sub>	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.8

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.25
$\overline{WE}$ , W <sub>A</sub>	0.40
W <sub>B</sub>	0.60
R <sub>A</sub>	0.70
R <sub>B</sub>	1.10
$\overline{RE}$	1.35

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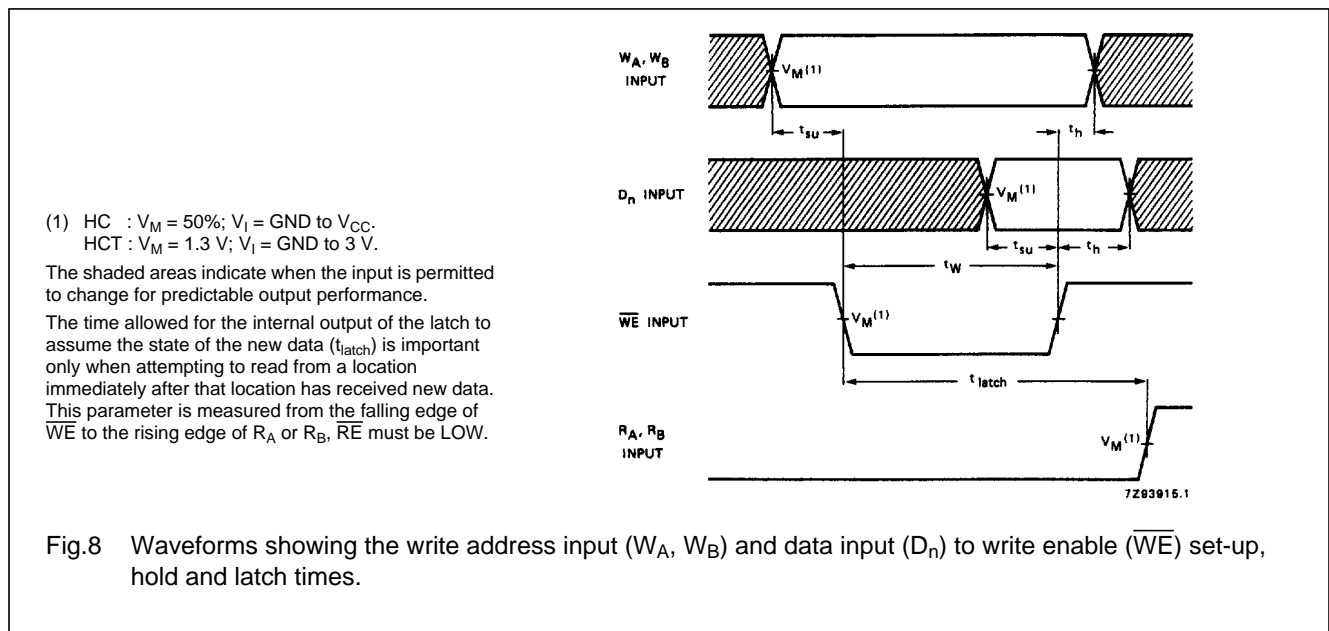
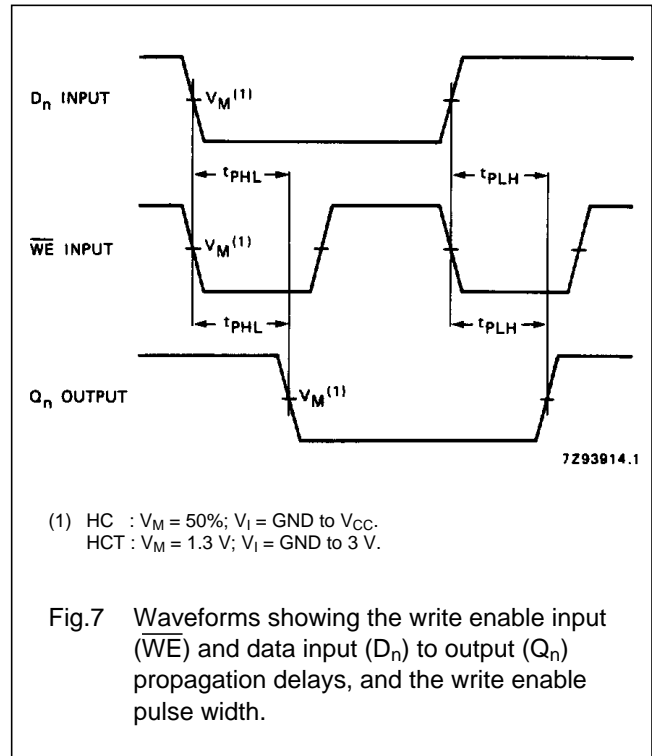
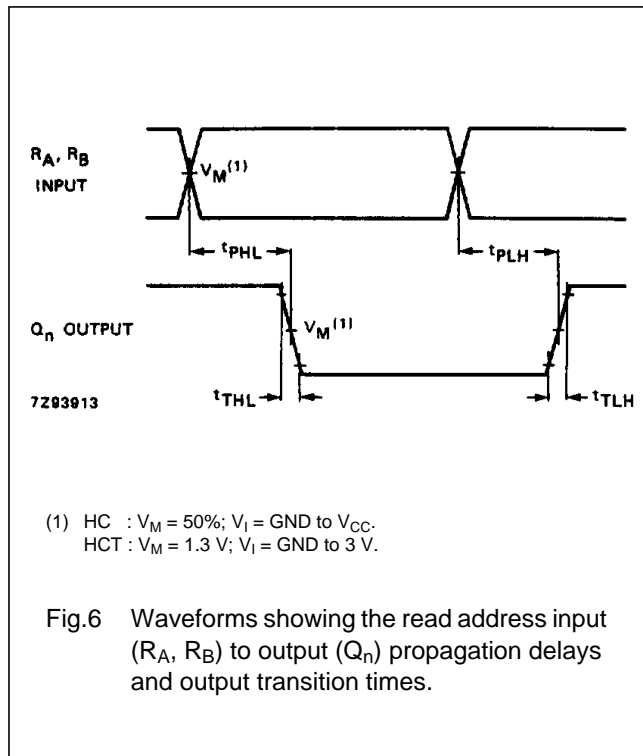
**AC CHARACTERISTICS FOR 74HCT**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay R <sub>A</sub> , R <sub>B</sub> to Q <sub>n</sub>		21	40		50		60	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{WE}$ to Q <sub>n</sub>		28	50		63		75	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to Q <sub>n</sub>		27	50		63		75	ns	4.5	Fig.7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time RE to Q <sub>n</sub>		18	35		44		53	ns	4.5	Fig.9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{RE}$ to Q <sub>n</sub>		19	35		44		53	ns	4.5	Fig.9
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6
t <sub>W</sub>	write enable pulse width LOW	18	9		23		27		ns	4.5	Fig.8
t <sub>su</sub>	set-up time D <sub>n</sub> to $\overline{WE}$	12	4		15		18		ns	4.5	Fig.8
t <sub>su</sub>	set-up time W <sub>A</sub> , W <sub>B</sub> to $\overline{WE}$	12	-2		15		18		ns	4.5	Fig.8
t <sub>h</sub>	hold time D <sub>n</sub> to $\overline{WE}$	5	-1		5		5		ns	4.5	Fig.8
t <sub>h</sub>	hold time W <sub>A</sub> , W <sub>B</sub> to $\overline{WE}$	5	0		5		5		ns	4.5	Fig.8
t <sub>latch</sub>	latch time $\overline{WE}$ to R <sub>A</sub> , R <sub>B</sub>	25	11		31		38		ns	4.5	Fig.8

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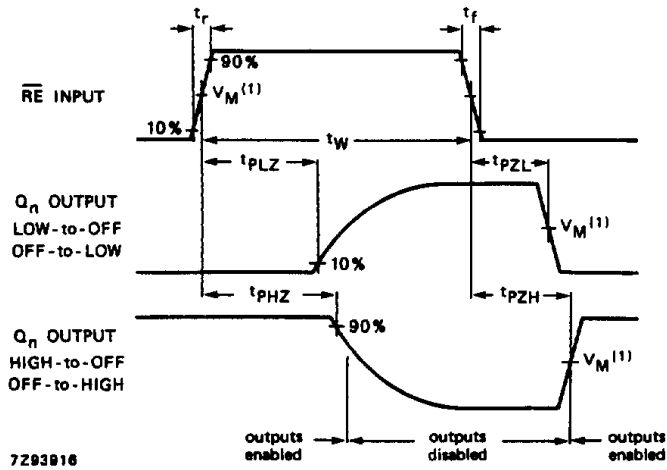
AC WAVEFORMS





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(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT :  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.9 Waveforms showing the read enable ( $\overline{RE}$ ) to output ( $Q_n$ ) enable and disable times, and the read enable pulse width.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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