# LF147JAN Wide Bandwidth Quad JFET Input Operational Amplifier

**Check for Samples: LF147JAN**

## FEATURES

- **Internally Trimmed Offset Voltage: 5 mV Max**
- **Low Input Bias Current: 50 pA Typ.**
- **Low Input Noise Current: 0.01 pA/√Hz Typ.**
- **Wide Gain Bandwidth: 4 MHz Typ.**
- **High Slew Rate: 13 V/μs Typ.**
- **Low Supply Current: 7.2 mA Typ.**
- **High Input Impedance: $10^{12}\Omega$ Typ.**
- **Low Total Harmonic Distortion:**
  - **$A_V$ = 10, $R_L$ = 10KΩ, $V_O$ = $20V_{P-P}$**
  - **BW = 20Hz — 20KHz ≤0.02% Typ.**
- **Low 1/f Noise Corner: 50 Hz Typ.**
- **Fast Settling Time to 0.01%: 2 μs Typ.**

## DESCRIPTION

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage ( BI-FET™ II technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

### Connection Diagram

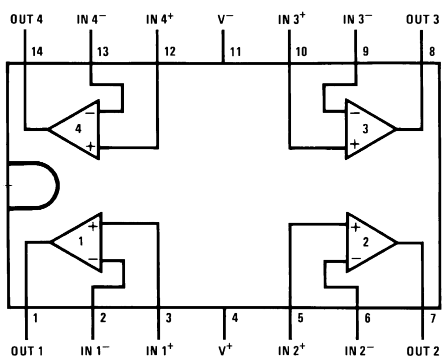



**Figure 1. CDIP Package**
**Top View**
**See Package Number J**

## Simplified Schematic

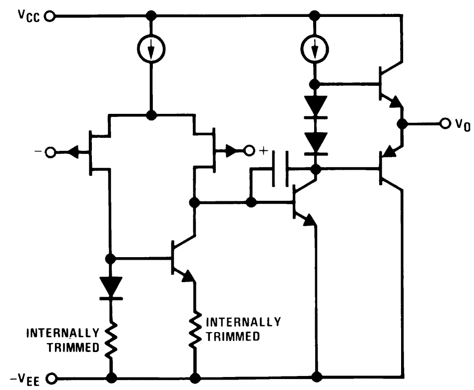
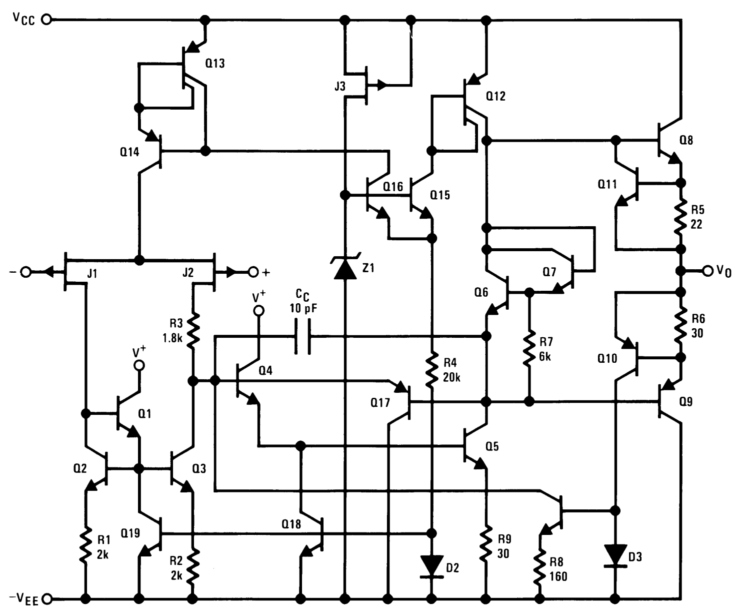



**Figure 2. ¼ Quad**

## Detailed Schematic




These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[1]

| | |
|---|---|
| Supply Voltage | ±18V |
| Differential Input Voltage | ±30V |
| Input Voltage Range[2] | ±15V |
| Output Short Circuit Duration[3] | Continuous |
| Power Dissipation[4][5] | 900 mW |
| $T_J$ max | 150°C |
| $\theta_{JA}$ CDIP | 70°C/W |
| Operating Temperature Range | $-55°C \leq T_A \leq 125°C$ |
| Storage Temperature Range | $-65°C \leq T_A \leq 150°C$ |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| ESD[6] | 900V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{Jmax}$ (maximum junction temperature), $\theta_{JA}$ (Package junction to ambient thermal resistance), and $T_A$ (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} — T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.
(6) Human body model, 1.5 kΩ in series with 100 pF.

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage Range | ±5V to ±15V |

## Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

| Subgroup | Description | Temp (°C) |
|---|---|---|
| 1 | Static tests at | 25 |
| 2 | Static tests at | 125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | 25 |
| 5 | Dynamic tests at | 125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | 25 |
| 8A | Functional tests at | 125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | 25 |
| 10 | Switching tests at | 125 |
| 11 | Switching tests at | -55 |
| 12 | Settling Time at | 25 |

## LF147JAN Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified: $V_{CC}$ = ±15V, $V_{CM}$ = 0V

| Symbol | Parameter | Conditions | Notes | Min | Max | Unit | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input Offset Voltage | $+V_{CC}$ = 26V, $-V_{CC}$ = -4V, $V_{CM}$ = -11V | | -5.0 | 5.0 | mV | 1 |
| | | | | -7.0 | 7.0 | mV | 2, 3 |
| | | $+V_{CC}$ = 4V, $-V_{CC}$ = -26V, $V_{CM}$ = 11V | | -5.0 | 5.0 | mV | 1 |
| | | | | -7.0 | 7.0 | mV | 2, 3 |
| | | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = 0V | | -5.0 | 5.0 | mV | 1 |
| | | | | -7.0 | 7.0 | mV | 2, 3 |
| | | $+V_{CC}$ = 5V, $-V_{CC}$ = -5V, $V_{CM}$ = 0V | | -5.0 | 5.0 | mV | 1 |
| | | | | -7.0 | 7.0 | mV | 2, 3 |
| $\pm I_{IB}$ | Input Bias Current | $+V_{CC}$ = 26V, $-V_{CC}$ = -4V, $V_{CM}$ = -11V | | -0.4 | 0.2 | nA | 1 |
| | | | | -10 | 50 | nA | 2 |
| | | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = 0V | | -0.2 | 0.2 | nA | 1 |
| | | | | -10 | 50 | nA | 2 |
| | | $+V_{CC}$ = 4V, $-V_{CC}$ = -26V, $V_{CM}$ = 11V | | -0.2 | 1.2 | nA | 1 |
| | | | | -10 | 70 | nA | 2 |
| $I_{IO}$ | Input Offset Current | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = 0V | | -0.1 | 0.1 | nA | 1 |
| | | | | -20 | 20 | nA | 2 |
| +PSRR | Power Supply Rejection Ratio | $-V_{CC}$ = -15V, $+V_{CC}$ = 20V to 10V | | 80 | | dB | 1, 2, 3 |
| -PSRR | Power Supply Rejection Ratio | $+V_{CC}$ = 15V, $-V_{CC}$ = -20V to -10V | | 80 | | dB | 1, 2, 3 |
| CMRR | Input Voltage Common Mode Rejection | $\pm V_{CC}$ = ±4V to ±26V, $V_{CM}$ = -11V to +11V | | 80 | | dB | 1, 2, 3 |
| $+I_{OS}$ | Output Short Circuit Current | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = -10V, t ≤ 25mS | | -80 | | mA | 1, 2, 3 |
| $-I_{OS}$ | Output Short Circuit Current | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = 10V, t ≤ 25mS | | | 80 | mA | 1, 2, 3 |
| $I_{CC}$ | Supply Current | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V | | | 14 | mA | 1, 2 |
| | | | | | 16 | mA | 3 |
| Delta $V_{IO}$ / Delta T | Input Offset Voltage Temp. Sensitivity | 25°C ≤ $T_A$ ≤ +125°C | See [(1)] | -30 | 30 | µV/°C | 2 |
| | | -55°C ≤ $T_A$ ≤ 25°C | See [(1)] | -30 | 30 | µV/°C | 3 |
| $+V_{OP}$ | Output Voltage Swing | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $R_L$=10KΩ, $V_{CM}$ = -15V | | 12 | | V | 4, 5, 6 |
| | | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $R_L$=2KΩ, $V_{CM}$ = -15V | | 10 | | V | 4, 5, 6 |
| $-V_{OP}$ | Output Voltage Swing | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $R_L$=10KΩ, $V_{CM}$ = 15V | | | -12 | V | 4, 5, 6 |
| | | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $R_L$ = 2KΩ, $V_{CM}$ = 15V | | | -10 | V | 4, 5, 6 |
| $+A_{VS}$ | Open Loop Voltage Gain | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $R_L$ = 2KΩ, $V_O$ = 0 to 10V | | 50 | | V/mV | 4 |
| | | | | 25 | | V/mV | 5, 6 |
| $-A_{VS}$ | Open Loop Voltage Gain | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $R_L$ = 2KΩ, $V_O$ = 0 to -10V | | 50 | | V/mV | 4 |
| | | | | 25 | | V/mV | 5, 6 |
| $A_{VS}$ | Open Loop Voltage Gain | $+V_{CC}$ = 5V, $-V_{CC}$ = -5V, $R_L$ = 10KΩ, $V_O$ = ±2V | | 20 | | V/mV | 4, 5, 6 |

(1) Calculated parameters.

## LF147JAN Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified: $V_{CC}$ = ±15V

| Symbol | Parameter | Conditions | Notes | Min | Max | Unit | Sub-groups |
|---|---|---|---|---|---|---|---|
| +SR | Slew Rate | $V_I$ = -5V to +5V | | 7 | | V/µS | 7 |
| | | | | 5 | | V/µS | 8A, 8B |
| -SR | Slew Rate | $V_I$ = +5V to -5V | | 7 | | V/µS | 7 |
| | | | | 5 | | V/µS | 8A, 8B |
| $TR_{TR}$ | Transient Response Rise Time | AV=1, $V_I$=50mV, $C_L$= 100pF, $R_L$=2KΩ | | | 200 | nS | 7, 8A, 8B |
| $TR_{OS}$ | Transient Response Overshoot | AV=1, $V_I$=50mV, $C_L$= 100pF, $R_L$=2KΩ | | | 40 | % | 7, 8A, 8B |
| $NI_{BB}$ | Noise Broadband | BW = 10Hz to 15KHz, $R_S$ = 0Ω | | | 15 | $\mu V_{RMS}$ | 7 |
| $NI_{PC}$ | Noise Popcorn | BW = 10Hz to 15KHz, $R_S$ = 100KΩ | | | 80 | $\mu V_{PK}$ | 7 |
| $C_S$ | Channel Separation | $R_L$ = 2KΩ | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, A to B | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, A to C | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, A to D | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, B to A | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, B to C | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, B to D | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, C to A | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, C to B | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, C to D | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, D to A | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, D to B | | 80 | | dB | 7 |
| | | $R_L$ = 2KΩ, $V_I$ = ±10V, D to C | | 80 | | dB | 7 |
| $\pm t_S$ | Settling Time | $A_V$ = 1 | | | 1,500 | nS | 12 |

## LF147JAN Electrical Characteristics Drift Values

The following conditions apply, unless otherwise specified: DC $\pm V_{CC}$ = ±15V, $V_{CM}$ = 0V, "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only"

| Symbol | Parameters | Conditions | Notes | Min | Max | Unit | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input Offset Voltage | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = 0V | | -1.0 | 1.0 | mV | 1 |
| $+I_{IB}$ | Input Bias Current | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = 0V | | -0.1 | 0.1 | nA | 1 |
| $-I_{IB}$ | Input Bias Current | $+V_{CC}$ = 15V, $-V_{CC}$ = -15V, $V_{CM}$ = 0V | | -0.1 | 0.1 | nA | 1 |

## Typical Performance Characteristics

**Input Bias Current**

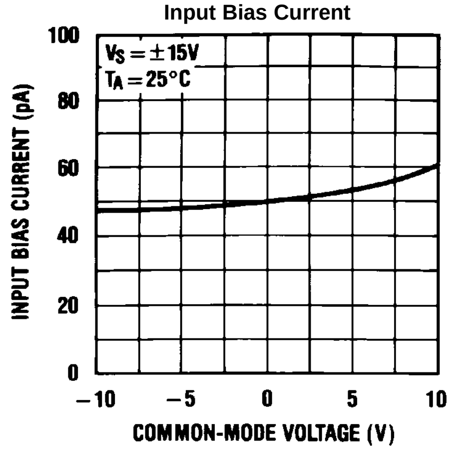



**Figure 3.**

**Input Bias Current**

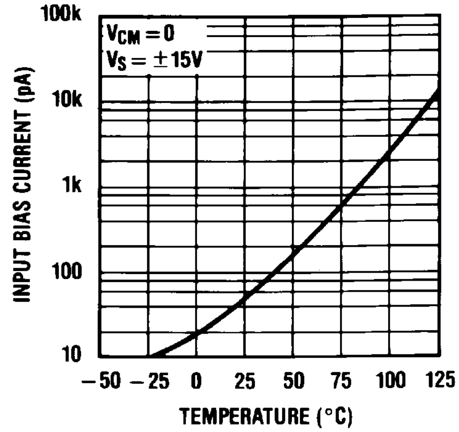



**Figure 4.**

**Supply Current**

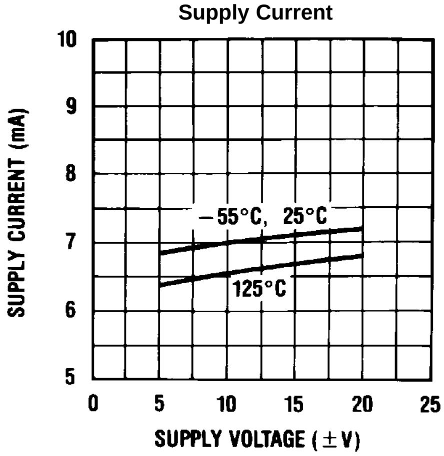



**Figure 5.**

**Positive Common-Mode Input Voltage Limit**

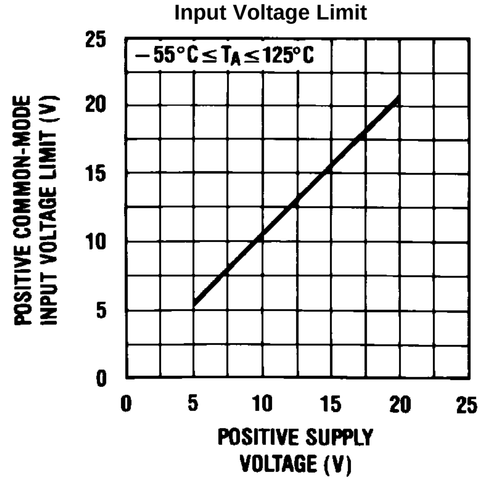



**Figure 6.**

**Negative Common-Mode Input Voltage Limit**

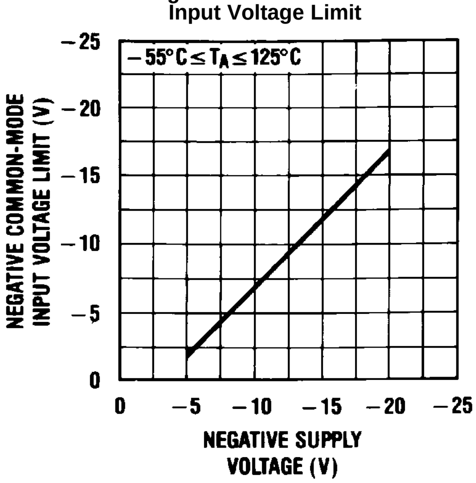



**Figure 7.**

**Positive Current Limit**

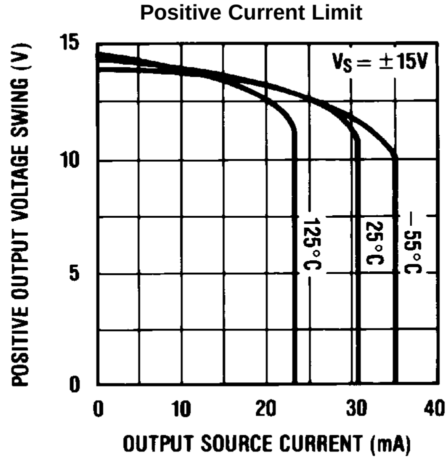



**Figure 8.**

## Typical Performance Characteristics (continued)

**Negative Current Limit**

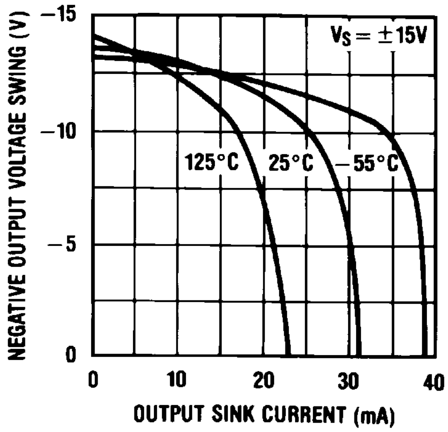



**Figure 9.**

**Output Voltage Swing**

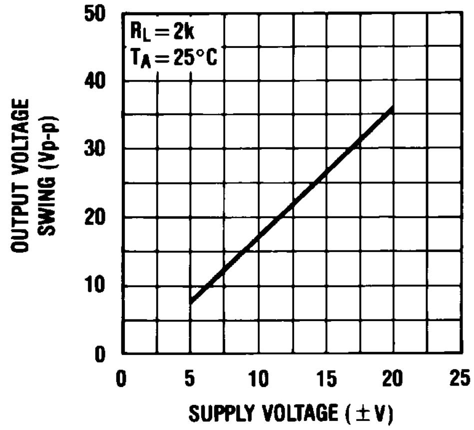



**Figure 10.**

**Output Voltage Swing**

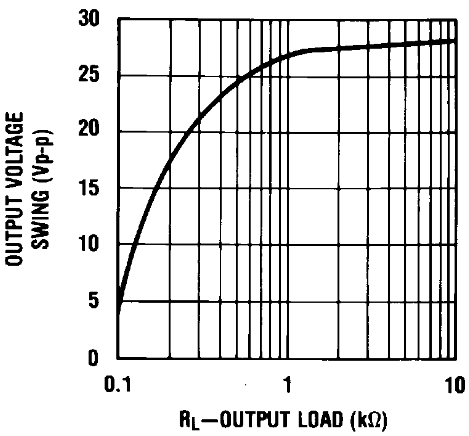



**Figure 11.**

**Gain Bandwidth**

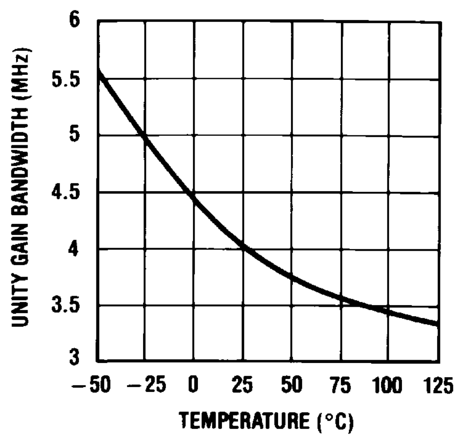



**Figure 12.**

**Bode Plot**

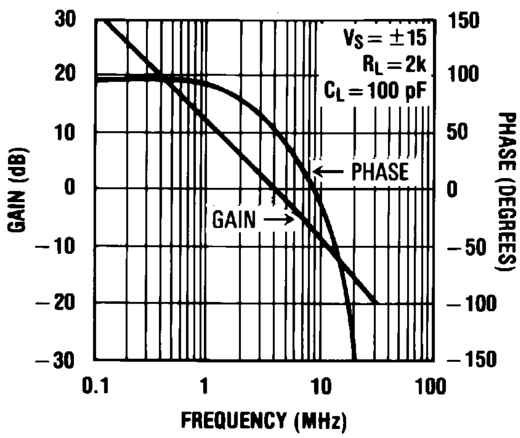



**Figure 13.**

**Slew Rate**

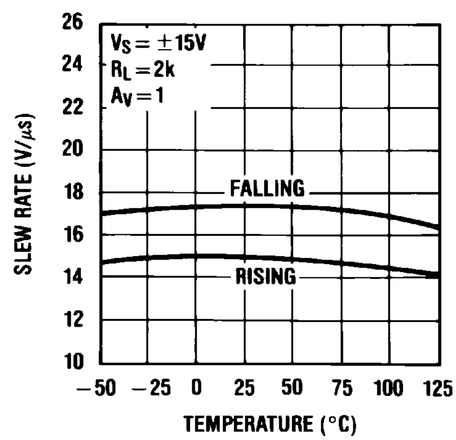



**Figure 14.**

## Typical Performance Characteristics (continued)

Distortion vs Frequency

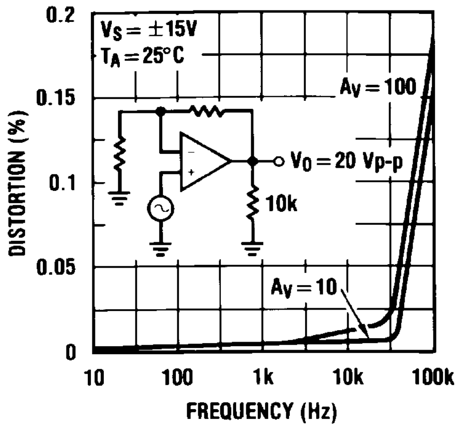



Figure 15.

Undistorted Output Voltage Swing

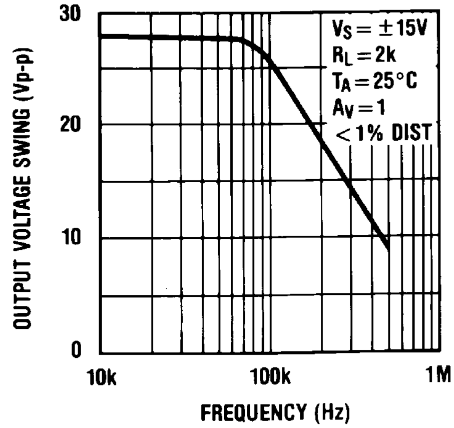



Figure 16.

Open Loop Frequency Response

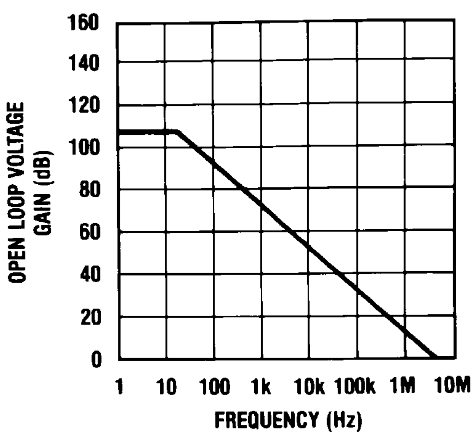



Figure 17.

Common-Mode Rejection Ratio

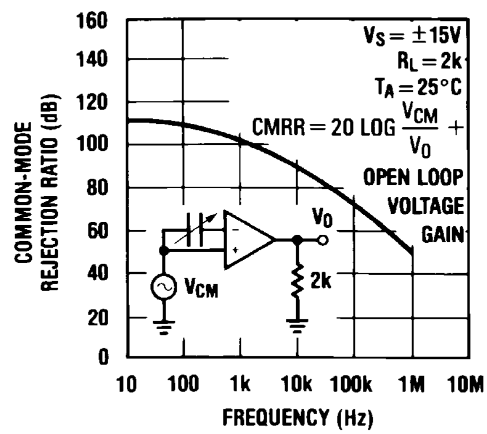



Figure 18.

Power Supply Rejection Ratio

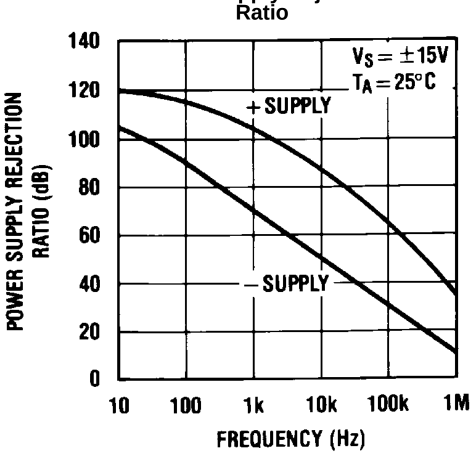



Figure 19.

Equivalent Input Noise Voltage

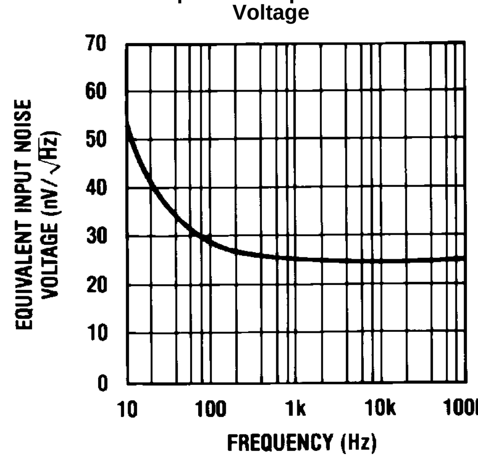



Figure 20.

## Typical Performance Characteristics (continued)

**Open Loop Voltage Gain**

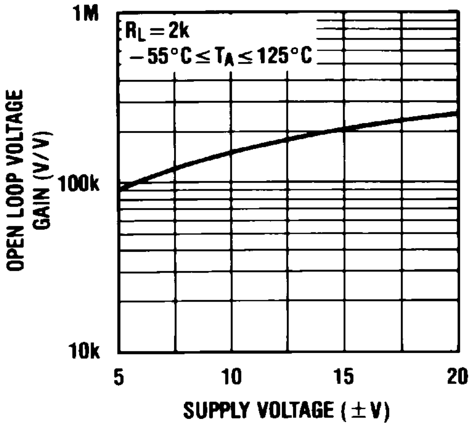



**Figure 21.**

**Output Impedance**

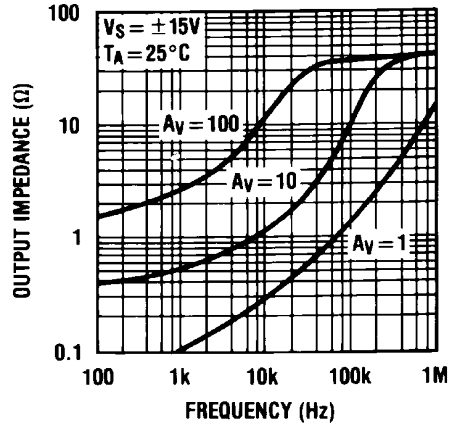



**Figure 22.**

**Inverter Settling Time**

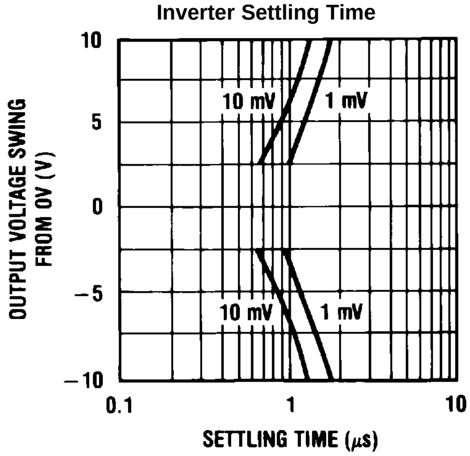



**Figure 23.**

## Pulse Response

$R_L$=2 kΩ, $C_L$=10 pF

**Small Signal Inverting**

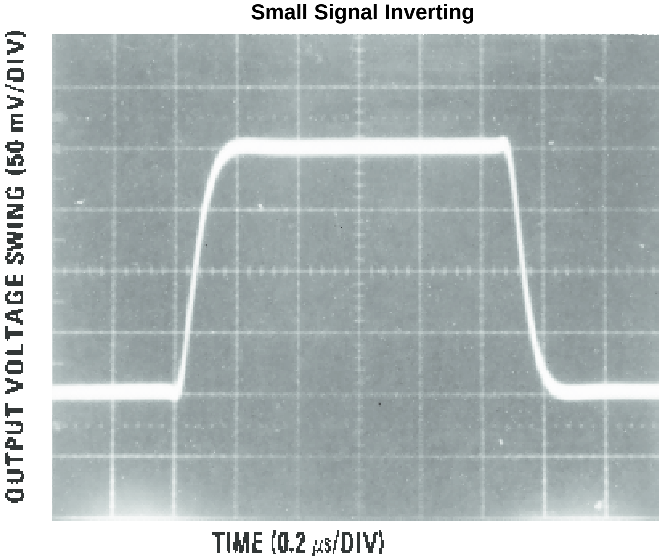



**Figure 24.**

**Small Signal Non-Inverting**

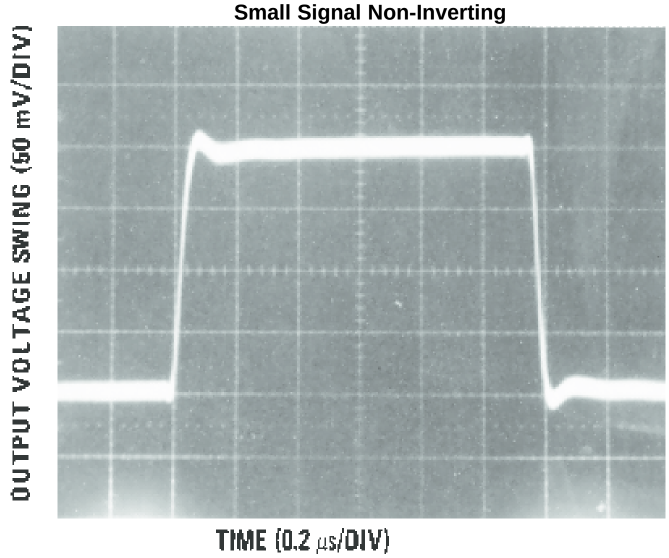



**Figure 25.**

## Pulse Response (continued)

$R_L$=2 kΩ, $C_L$=10 pF

**Large Signal Inverting**

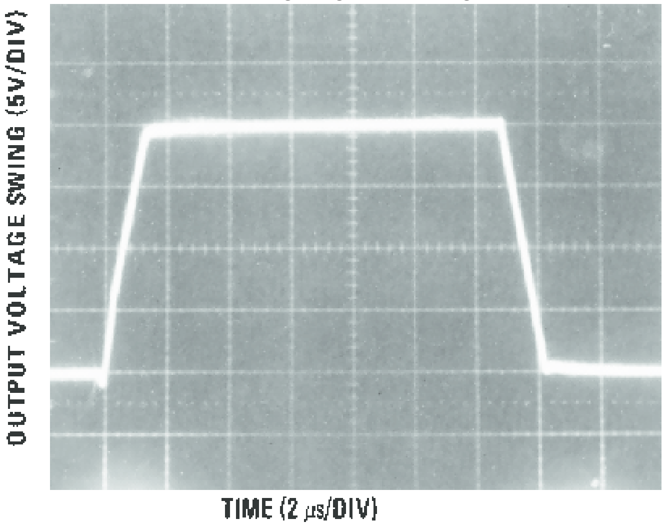



**Figure 26.**

**Large Signal Non-Inverting**

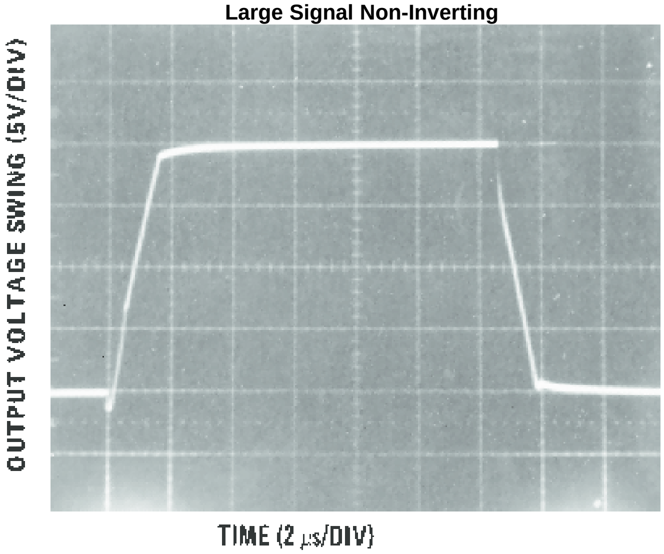



**Figure 27.**

**Current Limit ($R_L$=100Ω)**

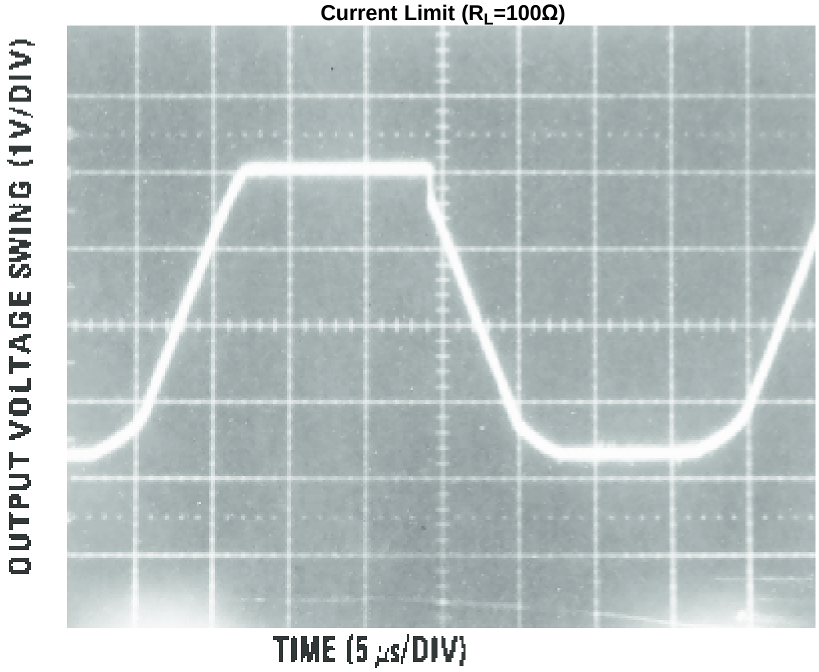



**Figure 28.**

## APPLICATION HINTS

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

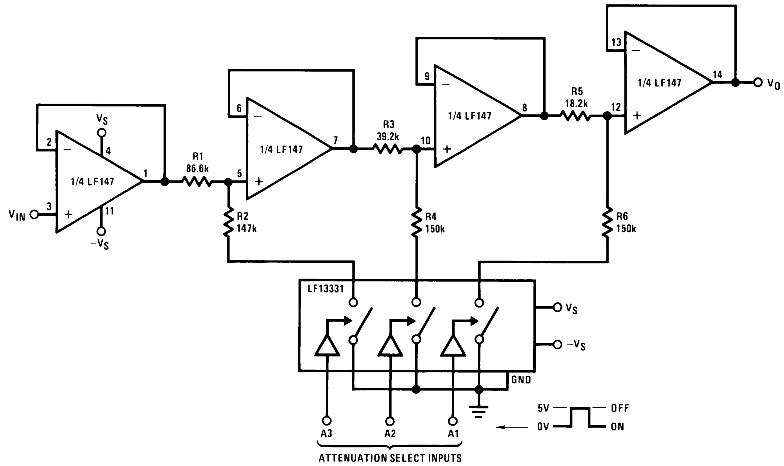
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

## Typical Applications

**Figure 29. Digitally Selectable Precision Attenuator**

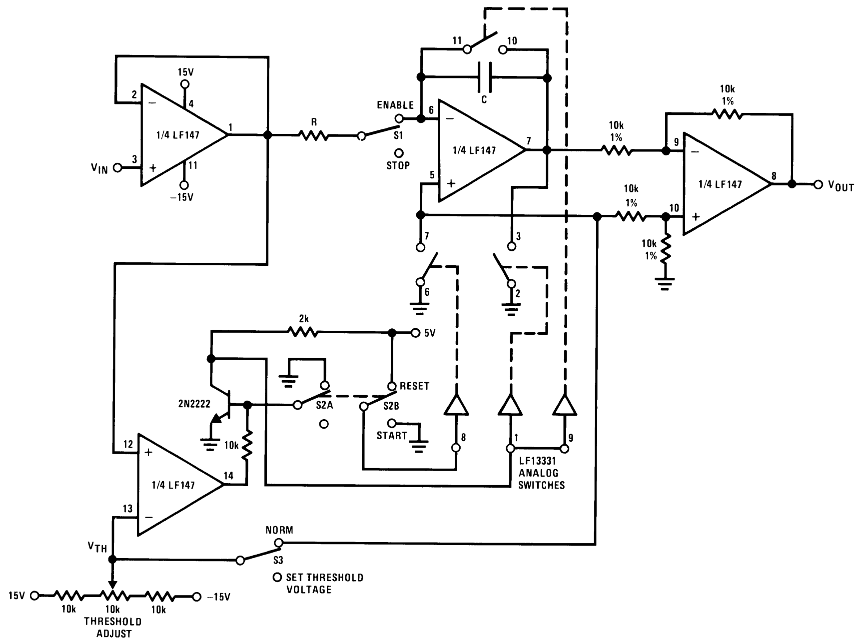



All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
  No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

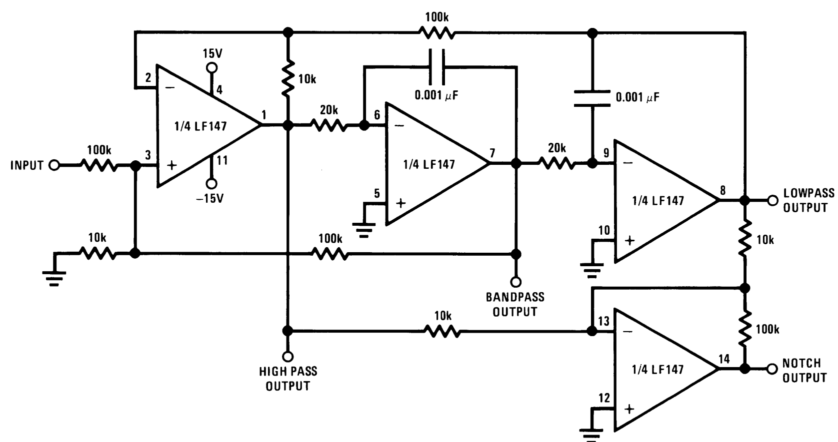
| A1 | A2 | A3 | $V_O$ Attenuation |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | −1 dB |
| 0 | 1 | 0 | −2 dB |
| 0 | 1 | 1 | −3 dB |
| 1 | 0 | 0 | −4 dB |
| 1 | 0 | 1 | −5 dB |
| 1 | 1 | 0 | −6 dB |
| 1 | 1 | 1 | −7 dB |

## Figure 30. Long Time Integrator with Reset, Hold and Starting Threshold Adjustment




- $V_O$ starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:
  $V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$
- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

## Figure 31. Universal State Variable Filter




For circuit shown:
$f_O$=3 kHz, $f_{NOTCH}$=9.5 kHz
Q=3.4
Passband gain:
Highpass – 0.1
Bandpass – 1
Lowpass – 1
Notch – 10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

| Date Released | Revision | Section | Originator | Changes |
|---|---|---|---|---|
| 04/18/05 | A | New Release into corporate format | L. Lytle | 1 MDS datasheets converted into one Corp. datasheet format. MJLF147–X rev 1B1 MDS will be archived |
| 03/20/13 | A | All | | Changed layout of National Data Sheet to TI format |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| JL147BCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | JL147BCA JM38510/11906BCA Q | Samples |
| JM38510/11906BCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | JL147BCA JM38510/11906BCA Q | Samples |
| M38510/11906BCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | Call TI | Level-1-NA-UNLIM | -55 to 125 | JL147BCA JM38510/11906BCA Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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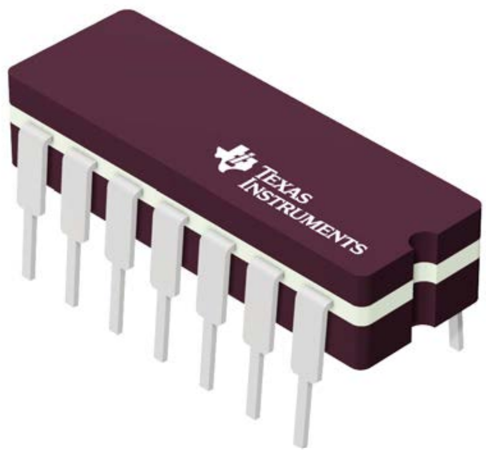
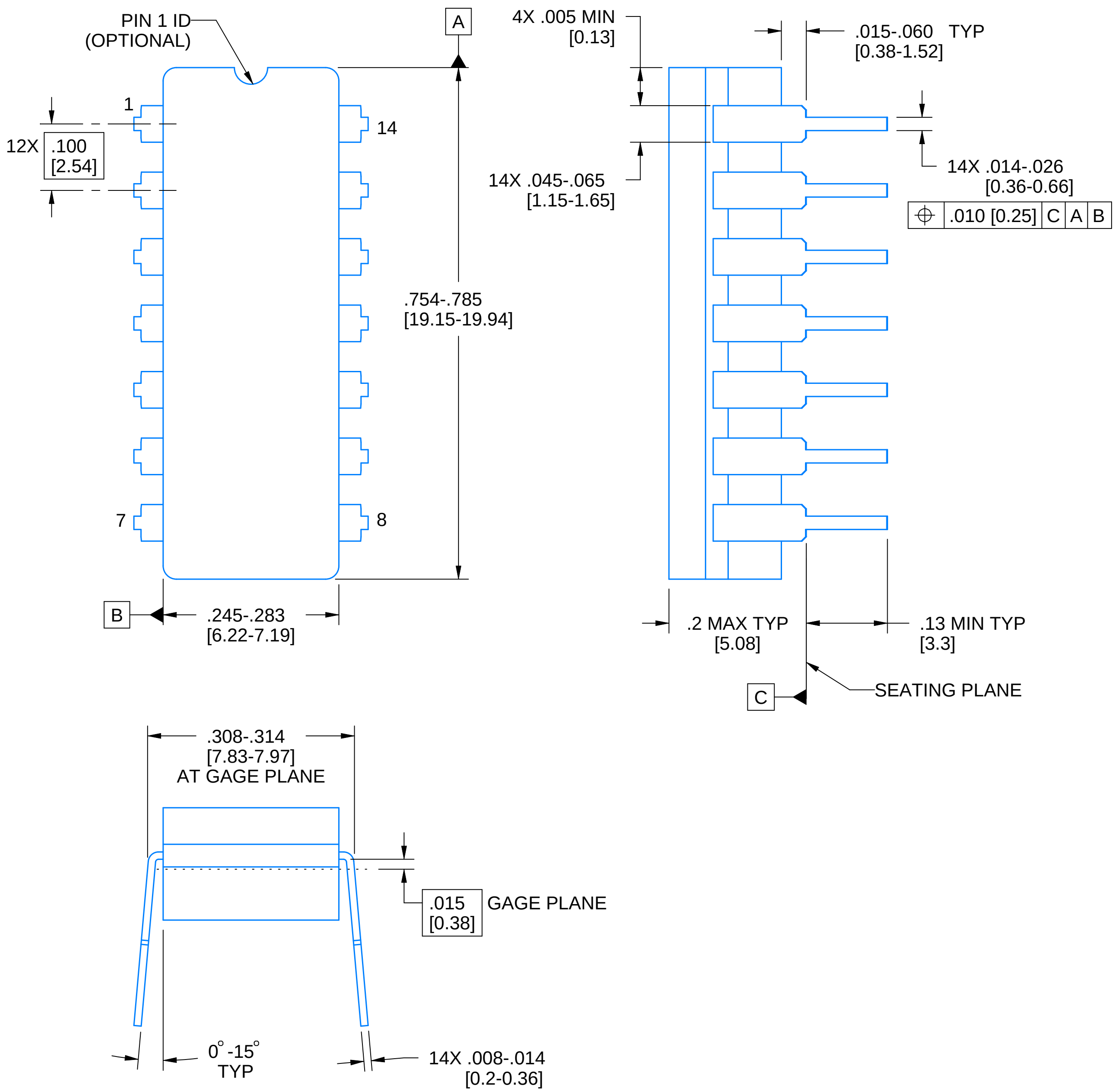
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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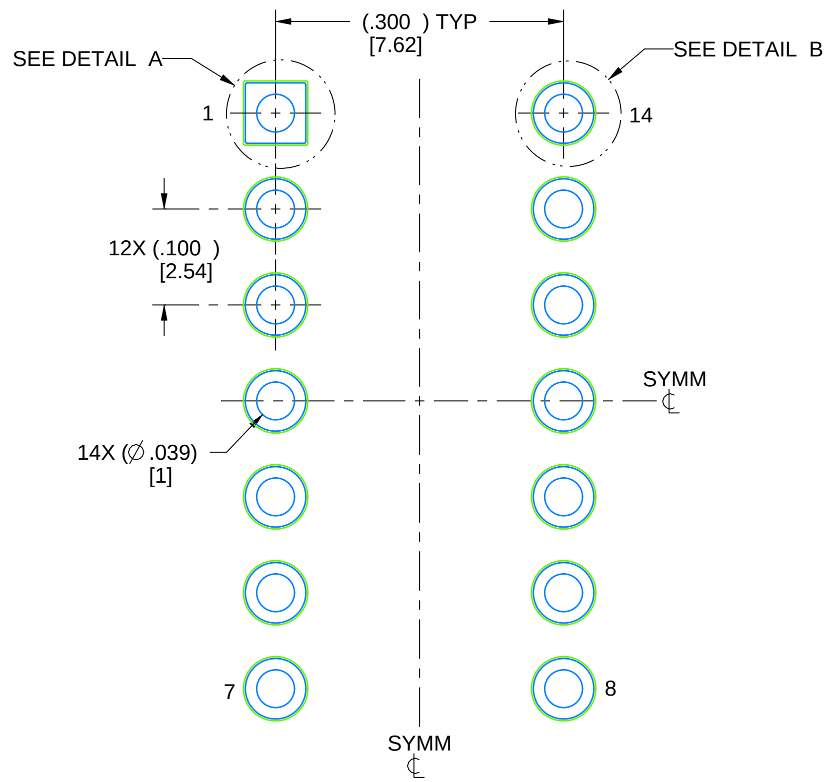
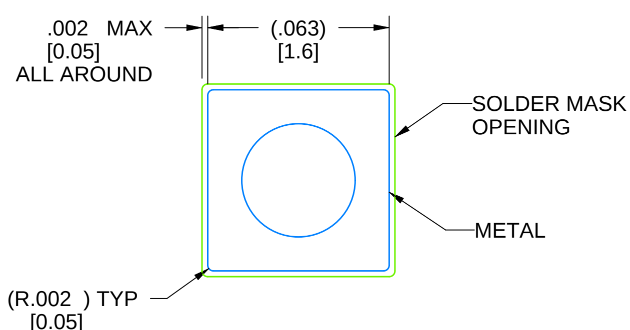
NOTES:

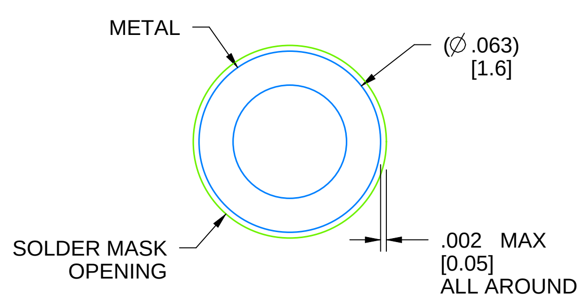
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

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