

### GPI65008DFIC

GaN Power IC in DFN5x6 Package

**Preliminary Datasheet version: 2.0** 

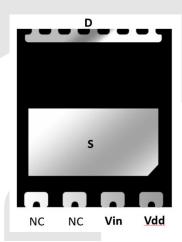
#### **Features**

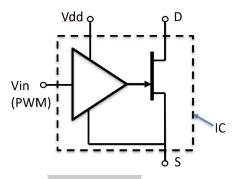
BV <sub>dss</sub>	R <sub>dson</sub>	l <sub>ds</sub>	
650V	170 mΩ	7.5 A	

- Ultra-low Rps(on)
- Ultra-low quiescent leakage current extending batter life
- High dv/dt capability
- Extremely low input capacitance
- Fast switching
- Low Profile

#### **Applications**

- Switching Power Applications
- Power adapters and power delivery chargers





### **Description**

These devices are power IC based on 650 V Power GaN HEMTs using proprietary E-mode GaN on silicon technology. The gate driver is integrated with the main power transistor resulting in fast switching, high system power density and low cost.

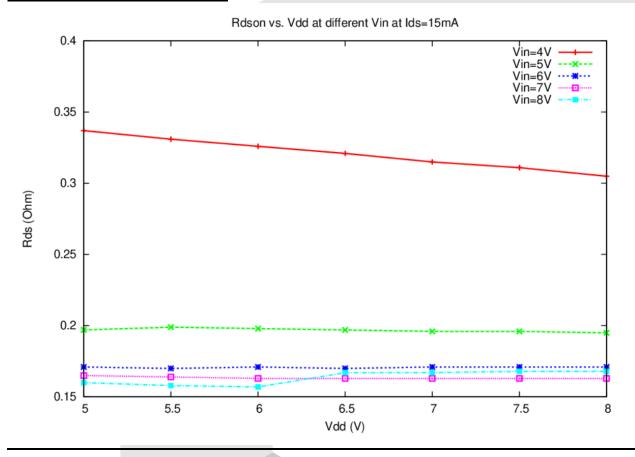
## **Device Characteristics**



Basic Parameters				Test data			
	Parameters		Conditions	Min	Typical	Max	Unit
1	BV <sub>dss</sub>	Drain-Source breakdown voltage	V <sub>gs</sub> =0V I <sub>d</sub> =10uA		650		V
2	R <sub>dson</sub>	Static drain-source on resistance, $T_C = 25^{\circ}C$	V <sub>gs</sub> =6V I <sub>d</sub> =1.8A	165	170	190	mΩ
3	Vdd	Drive supply voltage		5	6.5	8	
4	Vin	PWM input pin voltage		5	6.5	8	
5	Iddq	Drive supply (Vdd) quiescent leakage current	Vdd=6.5V			0.1	mA
Switching Performance			Test data				
	Parameters		Conditions	Min	Typical	Max	Unit
1	t <sub>d(on)</sub>	Turn-on delay time	V <sub>ds</sub> =350V		15		ns
2	t <sub>r</sub>	Rise time	I <sub>d</sub> =2.5A		10		ns
3	t <sub>d(off)</sub>	Turn-off delay time	Vin=5V		10		ns
4	t <sub>f</sub>	Fall time	V <sub>dd</sub> =6.5V		10		ns



# **Electrical Performance**



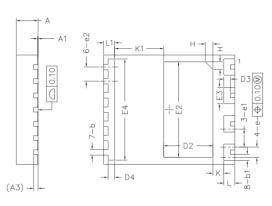


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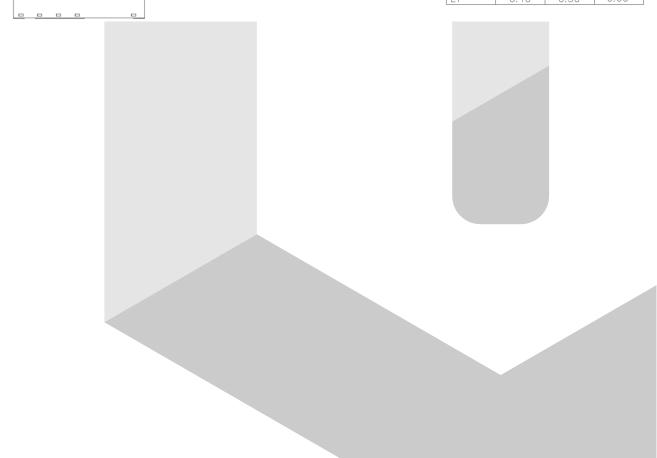
## **Package Information**





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX			
Α	0.90	1.00	1.10			
A1	0.00	0.02	0.05			
А3	0.203REF					
b	0.20	0.30				
b1	0.225	0.275	0.325			
D	5.90	6.00	6.10			
E	4.90	5.00	5.10			
D2	2.15	2.25	2.35			
E2	4.27	4.37	4.47			
D3	0.20	0.30	0.40			
E3	0.65	0.75	0.85			
D4	0.20	0.30	0.40			
E4	4.525	4.625	4.725			
е	0.375	0.475	0.575			
e1	0.725	0.825	0.925			
e2	0.55	0.65	0.75			
Н	0.35REF					
K	0.35	0.50	0.65			
K1	2.10	2.25	2.40			
L	0.40	0.50	0.60			
L1	0.40	0.50	0.60			





# **GaN HEMT Frequently Asked Questions**

1 Q: Can we do pin to pin switch for silicon MOSFET or IGBT?	
A: The short answer is no. GaN HEMT power devices are far superior than the best silico	
devices such as super junction MOSFETs. However, due to different requirements of gat	e
driving voltage and extremely high dv/dt slew rate, special drivers and optimized PCB layout	S
are recommended to minimize the impact from circuit parasitics. Some packaging forms suc	h
as GaNPower's DFN packaged devices offer both sense and force for the source terminal. Also	),
for traditional TO220 packages, please be advised that the pins are arranged as Gate – Source	e
-Drain, and the thermal pad is connected to the source instead of drain.	
2 Q: Are GaN power devices reliable?	
A: GaN power HEMTs have been tested by GaNPower and many other vendors, users an	d
testing facilities to be as reliable (if not better than) silicon counterparts.	
3 Q: How do GaN power devices compare with SiC?	
A: Currently GaN power HEMT devices are most suitable for low to medium voltage (≤1200\	<b>'</b> )
and power (<20KW) applications. GaN is the ideal choice for high frequency applications. Si	С
devices are better choice for high voltage and high-power applications (>20KW).	
4 Q: Do we need to parallel an FRD for applications such as inverters?	
A: GaN devices are different from silicon MOSFET or IGBT in that they have no inherent Pl	N
junction diodes that cause reverse recovery issue. User do not need to parallel an FRD for th	e
purpose of suppressing the body diode reverse recovery effect, since GaN HEMT can operat	e
in both first and third quadrants. However, care should be taken for the dead time power los	S
since the Vsd voltage of GaN HEMT is usually close to 2V. This is especially true when a negative	e
gate voltage is applied.	
5 Q: Can we parallel GaN HEMT devices?	
A: Yes, GaN HEMT is ideal for paralleling, due to positive temperature coefficient of Rdson	
and slightly positive temperature coefficient of threshold voltage.	