TM3415
P-CHANNEL ENHANCEMENT MOSFET

General Description

The TM3415 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch applications.

Product Summary

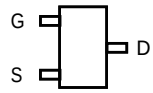
V_{DS}	-20V
I_D (at V_{GS}=-4.5V)	-4A
$R_{DS(ON)}$ (at V_{GS}= -4.5V)	< 41mΩ
$R_{DS(ON)}$ (at V_{GS}= -2.5V)	< 53mΩ
$R_{DS(ON)}$ (at V_{GS}= -1.8V)	< 65mΩ

ESD protected

100% UIS Tested

100% R_g Tested

TM3415
SOT-23
Top View



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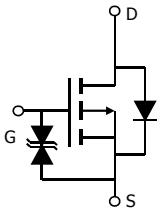


Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A=25℃	I_D	-4	A
	T_A=70℃		-3.5	
Pulsed Drain Current [C]		I_{DM}	-30	
Power Dissipation [B]	T_A=25℃	P_D	1.5	W
	T_A=70℃		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	65	80	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		85	100	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	43	52	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0V			-1	μA
		T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±8V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.3	-0.57	-0.9	V
$I_{D(ON)}$	On state drain current	V_{GS}=-4.5V, V_{DS}=-5V	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-4A		34	41	mΩ
		T_J=125℃		49	59	
		V_{GS}=-2.5V, I_D=-4A		42	53	mΩ
		V_{GS}=-1.8V, I_D=-2A		52	65	mΩ
		V_{GS}=-1.5V, I_D=-1A		61		mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-4A		20		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.64	-1	V
I_S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-10V, f=1MHz	600	751	905	pF
C_{oss}	Output Capacitance		80	115	150	pF
C_{rss}	Reverse Transfer Capacitance		48	80	115	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	6	13	20	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=-4.5V, V_{DS}=-10V, I_D=-4A	7.4	9.3	11	nC
Q_{gs}	Gate Source Charge		0.8	1	1.2	nC
Q_{gd}	Gate Drain Charge		1.3	2.2	3.1	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-4.5V, V_{DS}=-10V, R_L=2.5Ω, R_{GEN}=3Ω		13		ns
t_r	Turn-On Rise Time			9		ns
$t_{D(off)}$	Turn-Off DelayTime			19		ns
t_f	Turn-Off Fall Time			29		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-4A, dI/dt=500A/μs	20	26	32	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-4A, dI/dt=500A/μs	40	51	62	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

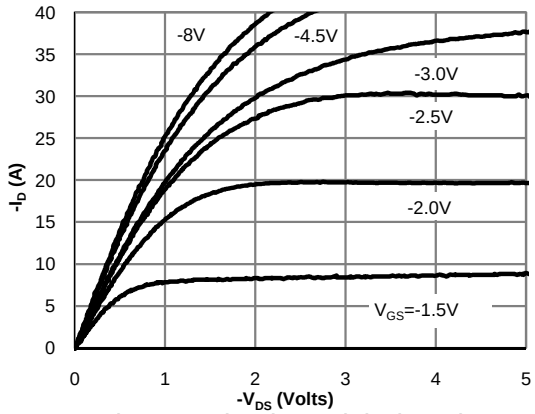


Fig 1: On-Region Characteristics (Note E)

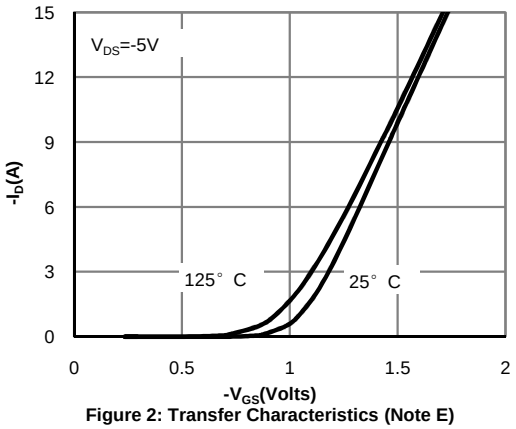


Figure 2: Transfer Characteristics (Note E)

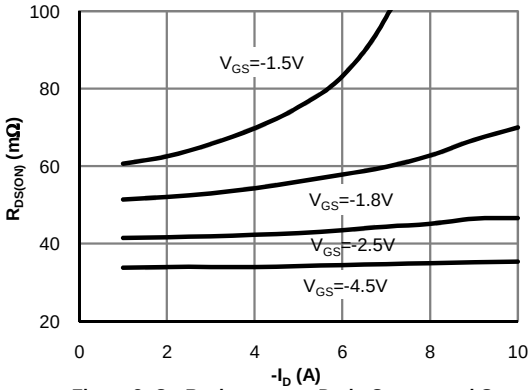


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

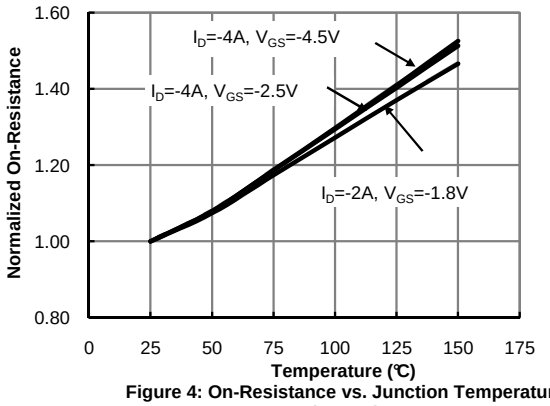


Figure 4: On-Resistance vs. Junction Temperature (Note E)

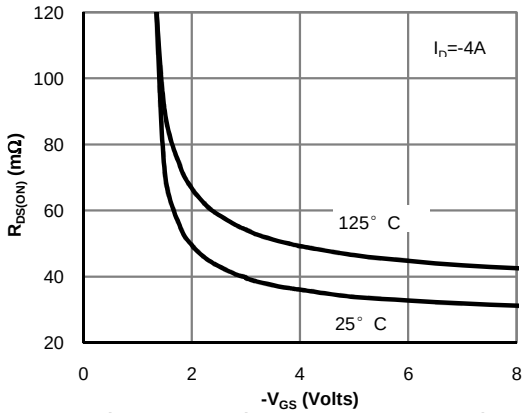


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

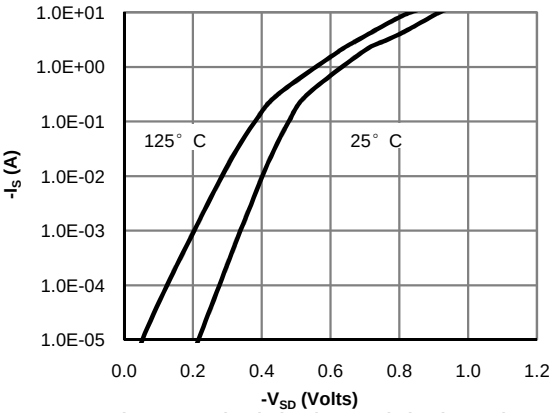


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

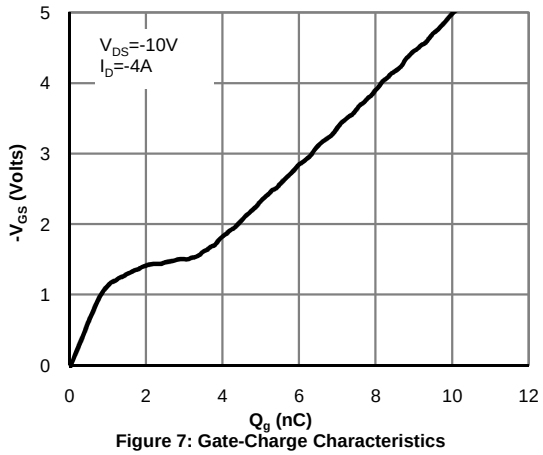


Figure 7: Gate-Charge Characteristics

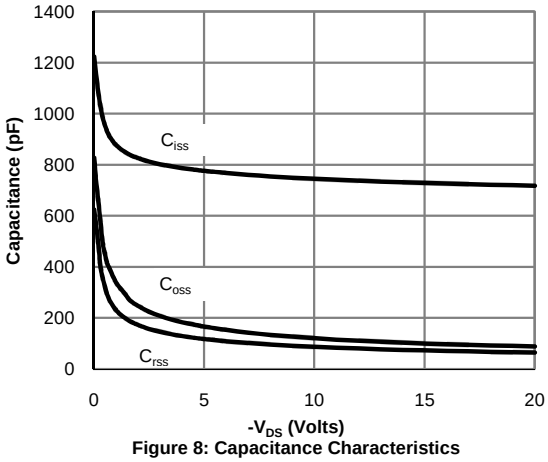


Figure 8: Capacitance Characteristics

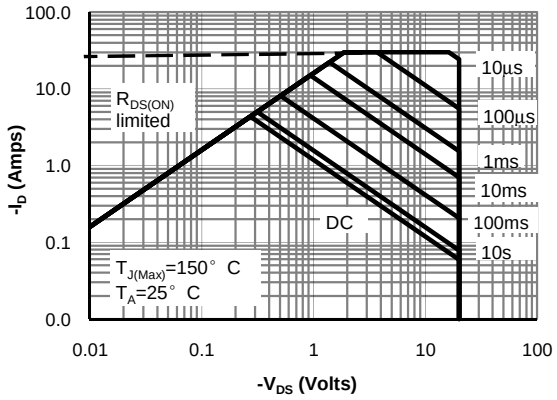


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

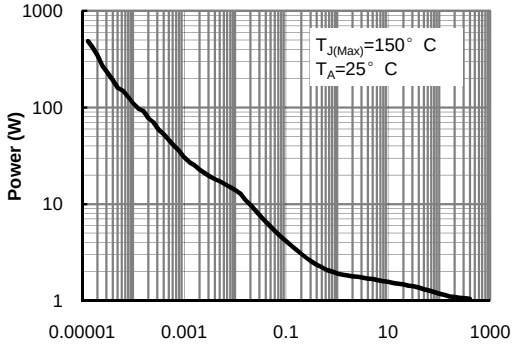


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

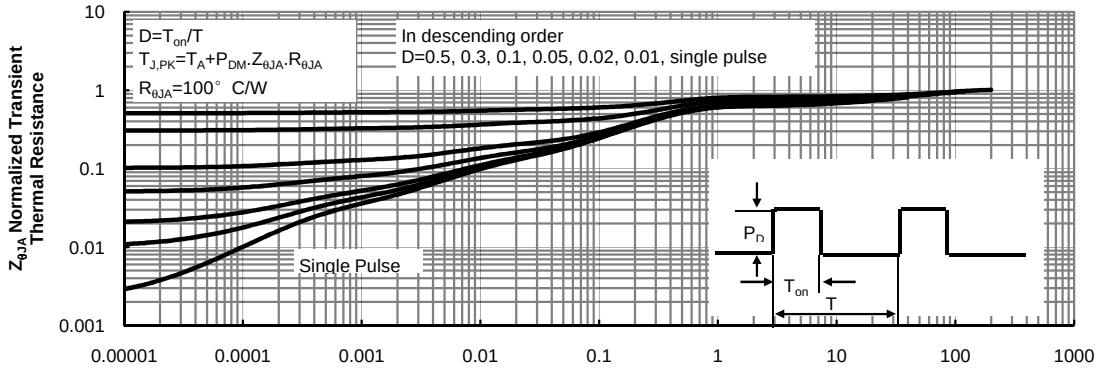
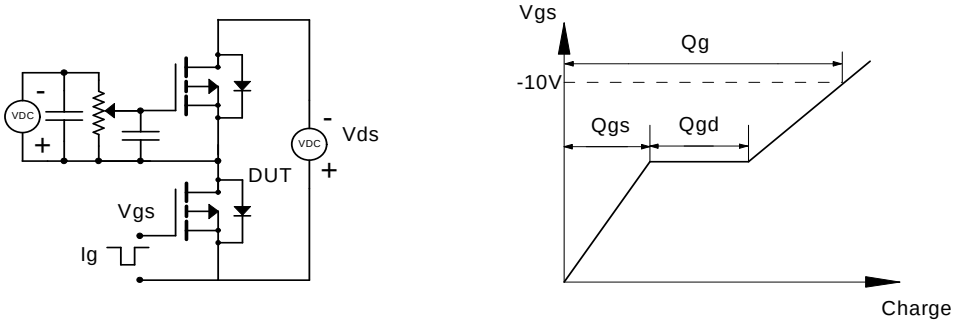
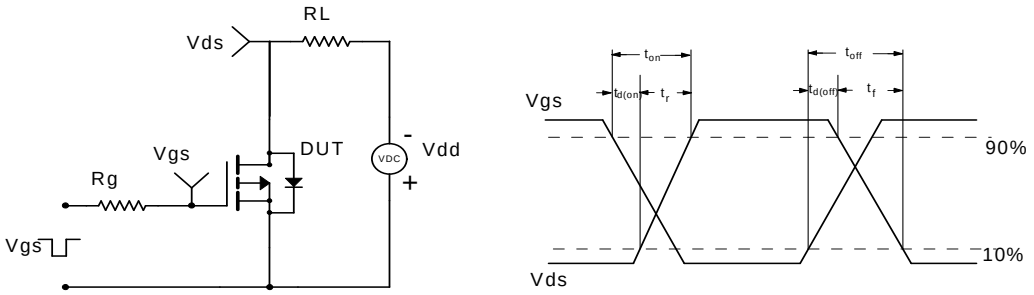


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

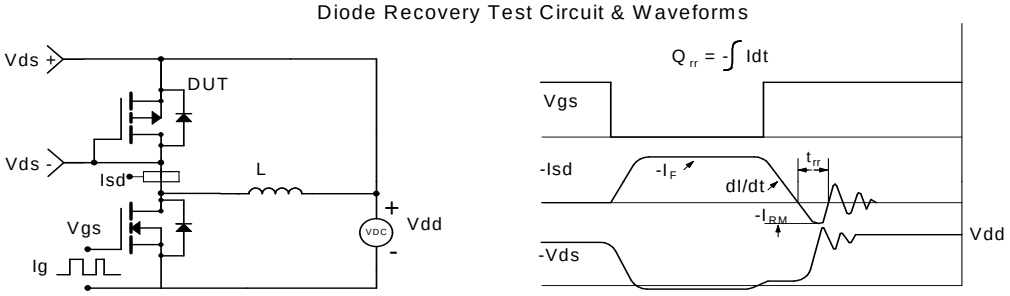
Gate Charge Test Circuit & Waveform



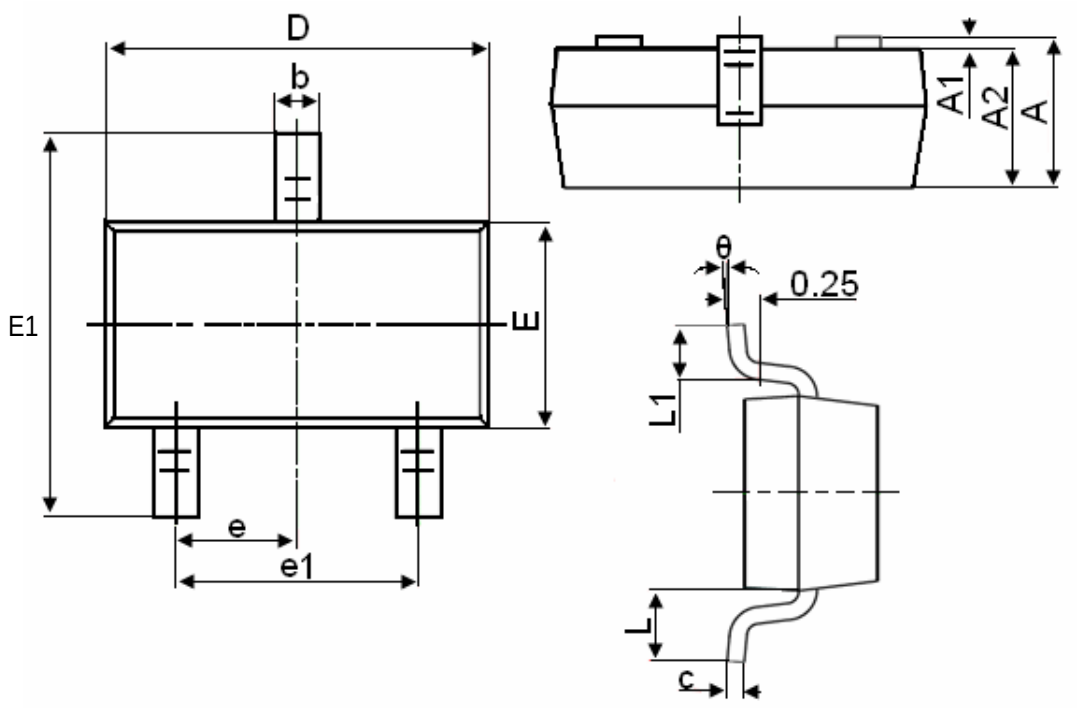
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



SOT-23 Package Information



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.