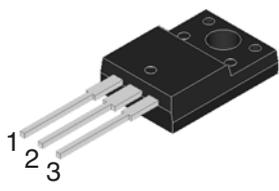
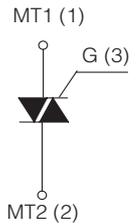


LOGIC LEVEL TRIAC

<p>TO-220F (FULLY ISOLATED CASE)</p>  	<p>On-State Current 16 Amp</p>	<p>Gate Trigger Current < 10 mA</p>	
	<p>Off-State Voltage 400 V ÷ 800 V</p>		
	<p>FEATURES</p> <ul style="list-style-type: none"> • Glass/passivated die junctions • Medium current Triac • Ideal for automated placement • Low thermal resistance • High surge current capability • Low forward voltage drop • Solder dip 260°C, 10s • Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC • Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C 		  RoHS COMPLIANT
	<p>MECHANICAL DATA</p> <ul style="list-style-type: none"> • Case: TO-220F. Epoxy meets UL 94V-0 flammability rating. • Polarity: As marked on the body. • Terminals: Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test. 		
<p>TYPICAL APPLICATIONS</p> <p>Logic level versions are designed to interface directly with low power drivers such as microcontrollers.</p>			

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95^\circ C$	16	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz ($t = 16.7$ ms)	176	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz ($t = 20$ ms)	160	A
I^2t	Fusing Current	$t_p = 10$ ms, Half Cycle	128	A ² s
I_{GM}	Peak Gate Current	20 μ s max. $T_j = 125^\circ C$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125^\circ C$	1	W
di/dt	Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$, $t_r \leq 100$ ns $f = 120$ Hz, $T_j = 125^\circ C$	50	A/ μ s
T_j	Operating Temperature		(-40 +125)	°C
T_{stg}	Storage Temperature		(-40 +150)	°C
T_{sld}	Soldering Temperature	10s max	260	°C
V_{iso}	R.M.S. isolation voltage 50/60 Hz sinusoidal waveform		2.500	Vac

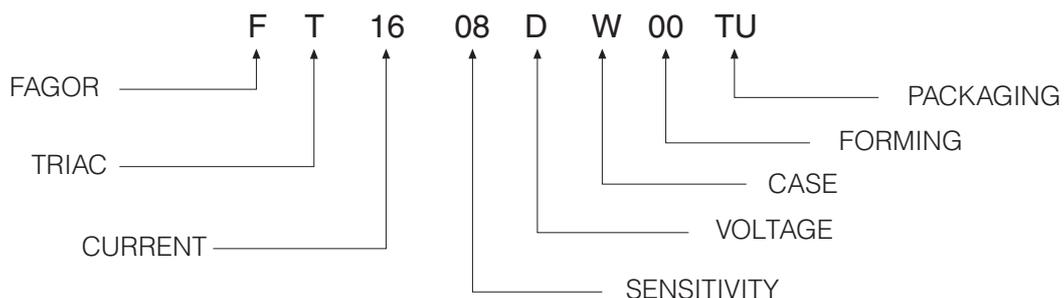
SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	400	600	800	V

LOGIC LEVEL TRIAC
Electrical Characteristics at Tamb = 25 °C

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY		Unit
					08	09	
I _{GT} ⁽¹⁾	Gate Trigger Current	V _D = 12 V _{DC} , R _L = 33Ω, T _j = 25 °C	Q1÷Q3	MAX	10	10	mA
			Q4	MAX		10	mA
V _{GT}	Gate Trigger Voltage	V _D = 12 V _{DC} , R _L = 33Ω, T _j = 25 °C	Q1÷Q3	MAX	1.3		V
			Q1÷Q4	MAX	1.3		V
V _{GD}	Gate Non Trigger Voltage	V _D = V _{DRM} , R _L = 3.3 KΩ, T _j = 125 °C	Q1÷Q3	MIN	0.2		V
			Q1÷Q4	MIN	0.2		V
I _H ⁽²⁾	Holding Current	I _T = 100 mA, Gate open, T _j = 25 °C		MAX	15	20	mA
I _L	Latching Current	I _G = 1.2 I _{GT} , T _j = 25 °C	Q1,Q3	MAX	25		mA
			Q1,Q3,Q4	MAX		20	mA
			Q2	MAX	30	25	mA
dV/dt ⁽²⁾	Critical Rate of Voltage Rise	V _D = 0.67 x V _{DRM} , Gate open T _j = 125 °C		MIN	40	50	V/μs
(di/dt) _c ⁽²⁾	Critical Rate of Current Rise	(dv/dt) _c = 0.1 V/μs T _j = 125 °C (dv/dt) _c = 10 V/μs T _j = 125 °C without snubber T _j = 125 °C		MIN	8.5	2.5	A/ms
				MIN	3.0	1.5	A/ms
				MIN			
V _{TM} ⁽²⁾	On-state Voltage	I _T = 22.5 Amp, t _p = 380 μs, T _j = 25 °C		MAX	1.55		V
V _{t(o)} ⁽²⁾	Threshold Voltage	T _j = 125 °C		MAX	0.77		V
r _d ⁽²⁾	Dynamic resistance	T _j = 125 °C		MAX	30		mΩ
I _{DRM} /I _{RRM}	Off-State Leakage Current	V _D = V _{DRM} , T _j = 125 °C		MAX	2		mA
		V _R = V _{RRM} , T _j = 25 °C		MAX	5		μA
R _{th(j-c)}	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.7		°C/W
R _{th(j-a)}	Thermal Resistance Junction-Ambient				50		°C/W

(1) Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

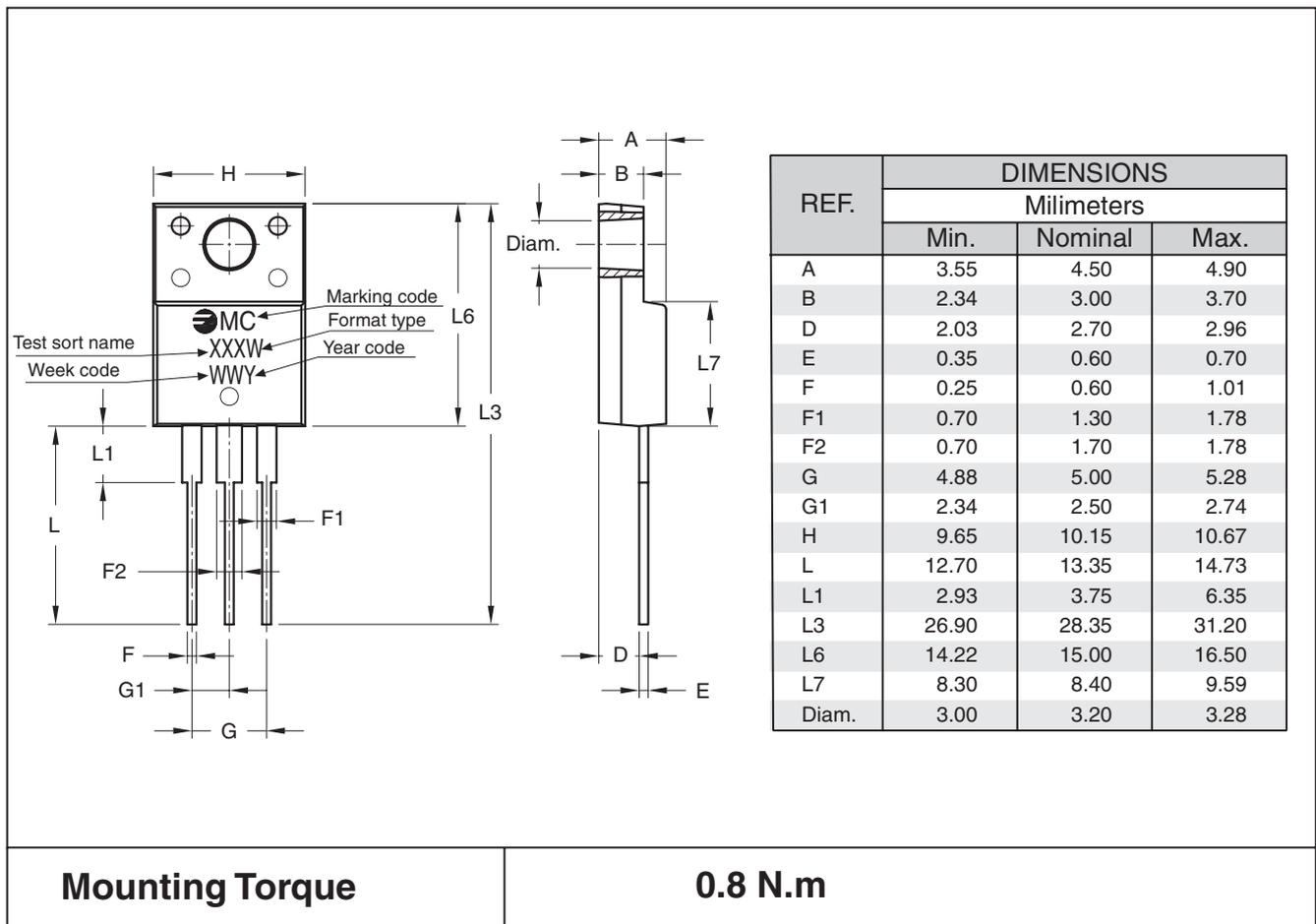
Part Number Information


LOGIC LEVEL TRIAC

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT1608MW 00TU	TU	TUBE	1,000	2.00

Package Outline Dimensions: (mm) TO-220F



LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle)

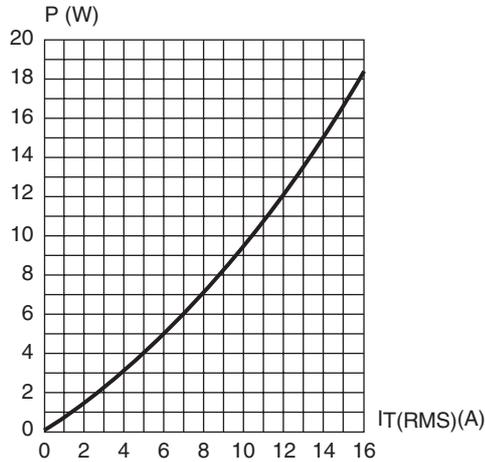


Fig. 2: RMS on-state current versus case temperature (full cycle).

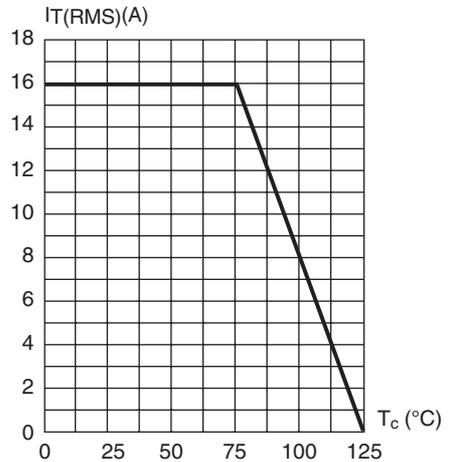


Fig. 3: Relative variation of thermal impedance versus pulse duration.

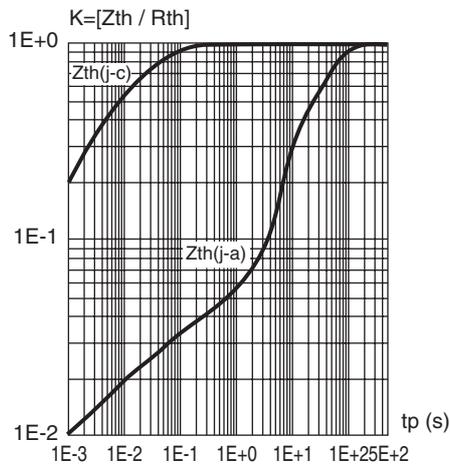


Fig. 4: On-state characteristics (maximum values)

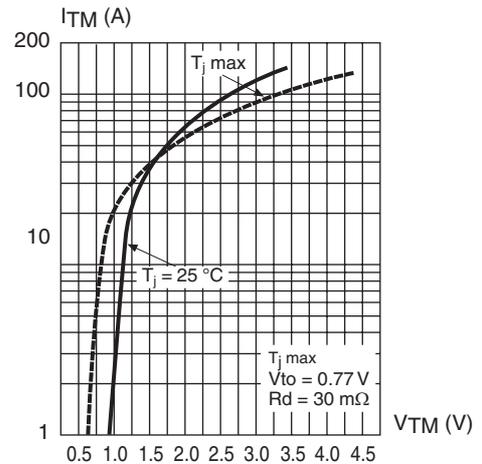


Fig. 5: Surge peak on-state current versus number of cycles

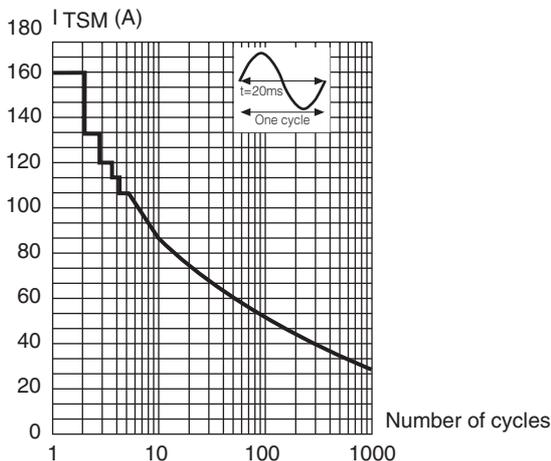
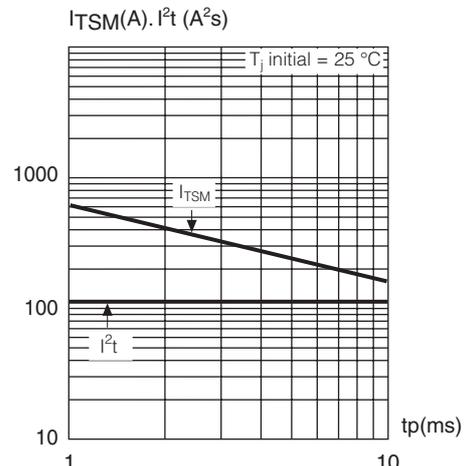


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I²t.



LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

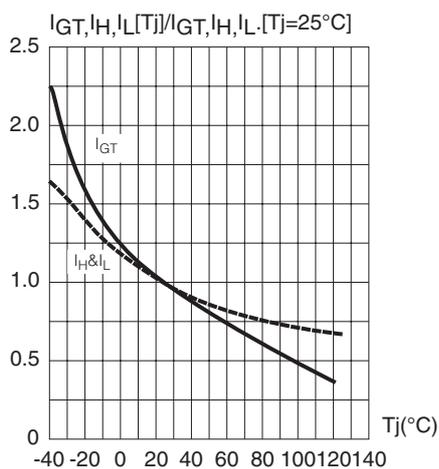


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

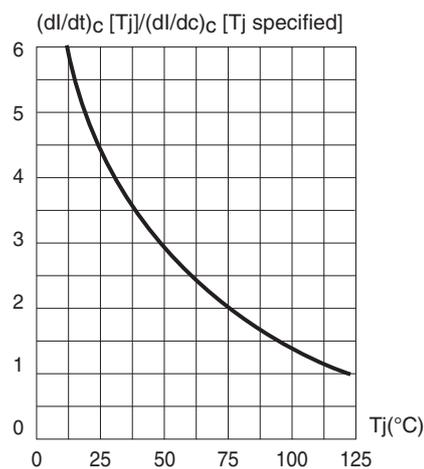
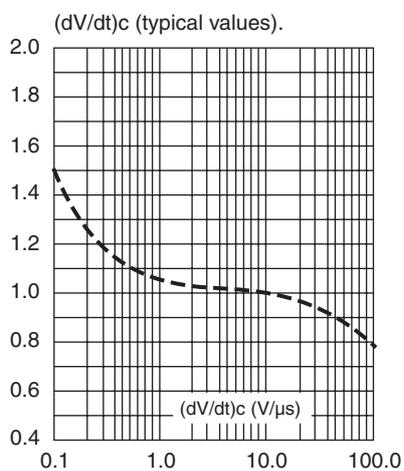


Fig. 9: Relative variation of critical rate of decrease of main current versus



LOGIC LEVEL TRIAC**Revision History**

Date	Revision	Description of Changes
Abr-2005	0	Original Data Sheet
Feb-2016	1	200V and 700V eliminated

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