UTRON

UT62L12916(I)

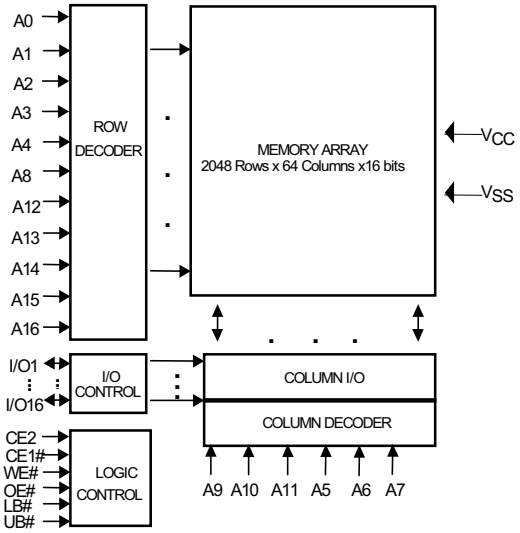
Preliminary Rev. 0.5

128K X 16 BIT LOW-POWER CMOS SRAM

FEATURES

- High speed access time : 70,100 ns (max.)
- Low power consumption :
- Operating : 5 mA (Icc1,max.)
  Standby : 80uA (max) L-version
  25uA (max) LL-version
- Single 2.7-3.3 V_{CC} power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three- state outputs
- Data Rentention Voltage: 1.5 V (min)
- Data byte controll: LB#(I/O1-I/O8)
  UB#(I/O9-I/O16)
- Package :
  48-pin Ball Tiny BGA (6mmx8mm)
- Product Family : UT62L12916
  UT62L12916I

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
CE1#,CE2	Chip Select Inputs
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower-byte Control(I/O1~I/O8)
UB#	Upper-byte Control(I/O9~I/O16)
V_{CC}	Power Supply
V_{SS}	Ground
N.C	No Connection

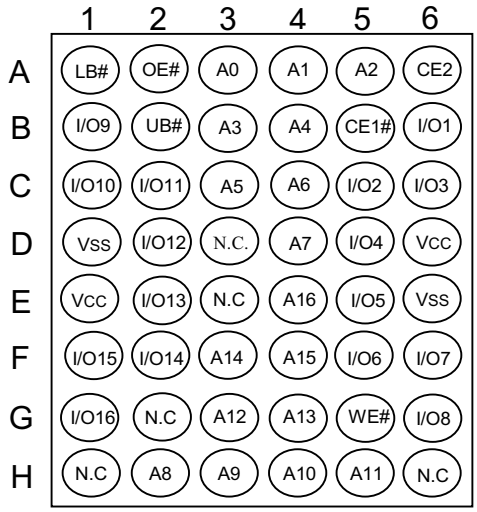
GENERAL DESCRIPTION

The UT62L12916(I) is a 2,097,152-bit low power CMOS static random access memory organized as 131,072 words by 16 bits.

The UT62L12916(I) is designed for low power application. It is particularly well suited for high density low power system application.

The UT62L12916(I) operates from a single 2.7V-3.3V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL		RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}		-0.3 to +4.6	V
Operating Temperature	TA	UT62L12916	0 to +70	℃
		UT62L12916(I)	-40 to +85	℃
Storage Temperature	T_{STG}		-65 to +150	℃
Power Dissipation	P_D		1.0~1.5	W
DC Output Current	I_{OUT}		20	mA
Soldering Temperature	T_{SOLDER}		260 • 10	℃ • sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE2	CE1#	OE#	WE#	LB#	UB#	I/O1~I/O8	I/O9~I/O16	SUPPLY CURRENT
Not Selected	L	X	X	X	X	X	Hight-Z	Hight-Z	I_{SB},I_{SB1}
	X	H	X	X	X	X	Hight-Z	Hight-Z	I_{SB},I_{SB1}
	X	X	X	X	H	H	Hight-Z	Hight-Z	I_{SB},I_{SB1}
Output Disable	H	L	H	H	X	X	Hight-Z	Hight-Z	I_{CC1},I_{CC2}
	H	L	H	H	X	L	Hight-Z	Hight-Z	
Read	H	L	L	H	L	H	Dout	Hight-Z	I_{CC1},I_{CC2}
	H	L	L	H	H	L	Hight-Z	Dout	
	H	L	L	H	L	L	Dout	Dout	
Write	H	L	X	L	L	H	Din	Hight-Z	I_{CC1},I_{CC2}
	H	L	X	L	H	L	Hight-Z	Din	
	H	L	X	L	L	L	Din	Din	

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (VCC = 2.7V-3.3V ,TA = 0℃ to 70℃/-40℃ to 85℃(I))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	Vcc			2.7	3.0	3.3	V
Input High Voltage	V_{IH}			2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$			-	1	μA
Output Leakage Current	I_{LO}	VSS ≦VI/O ≦VCC CE1# =VIH (min) , CE2 =VIL (min) or OE#(min)= VIH or WE #=VIL (max)		- 1	-	1	μA
Output High Voltage	V_{OH}	IOH = - 1.0mA		2.2	-	-	V
Output Low Voltage	V_{OL}	IOL= 2.1mA		-	-	0.4	V
Operating Power Supply Courrent	I_{CC}	CE2= VIH,CE1#= VIL , VIN = VIH or VIL, $I_{I/O}$ = 0mA		-	-	3	mA
Average Operating Current	I_{CC1}	Cycle time=1us,100% duty,$I_{I/O}$=0mA CE1# ≦0.2V,CE2≧VCC-0.2V VIN≧Vcc-0.2V or VIN≦0.2V		-	-	5	mA
	I_{CC2}	Cycle time=min,100% duty,$I_{I/O}$=0mA CE1# =VIL, CE2= VIH, VIN=VIH OR VIL		-	-	35	mA
Standby Power	I_{SB}	CE1#=VIH (min) or CE2= VIH		-	-	0.5	mA
Supply Current	I_{SB1}	CE1#≧VCC-0.2V or CE2≦0.2V	L-Version	-	-	80	uA
			LL-Version	-	-	25	uA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L=30pF+ 1TTL Load

AC ELECTRICAL CHARACTERISTICS (VCC = 2.7V-3.3V , TA = 0℃ to 70℃/-40℃ to 85℃(I))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L12916(I)-70		UT62L12916(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	70	-	100	-	ns
Address Access Time	t_{AA}	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	35	-	50	ns
UB#,LB# Access Time	t_{BA}	-	70	-	100	ns
Chip Enable to Output in Low-Z	t_{CLZ} *	10	-	10	-	ns
Output Enable to Output in Low-Z	T_{OLZ} *	5	-	5	-	ns
UB#,LB# Enable to Output in Low-z	t_{BLZ}	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}*	-	25	-	30	ns
Output Disable to Output in High-Z	t_{OHZ}*	-	25	-	30	ns
UB#,LB# Disable to Output in High-Z	t_{BHZ}	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	ns

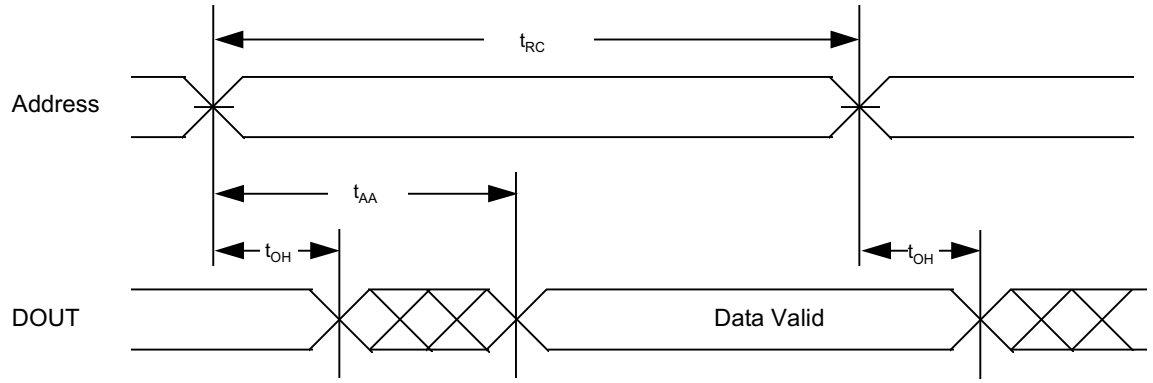
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L12916(I)-70		UT62L12916(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	60		80	-	ns
Chip Enable to End of Write	t_{CW}	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
UB#,LB# Enable to End of Write	t_{BW}	60	-	80	-	ns
Write Pulse Width	t_{WP}	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	30	-	40	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	60	-	80	-	ns
Write to Output in High-Z	t_{WHZ}*	0	15	0	15	ns

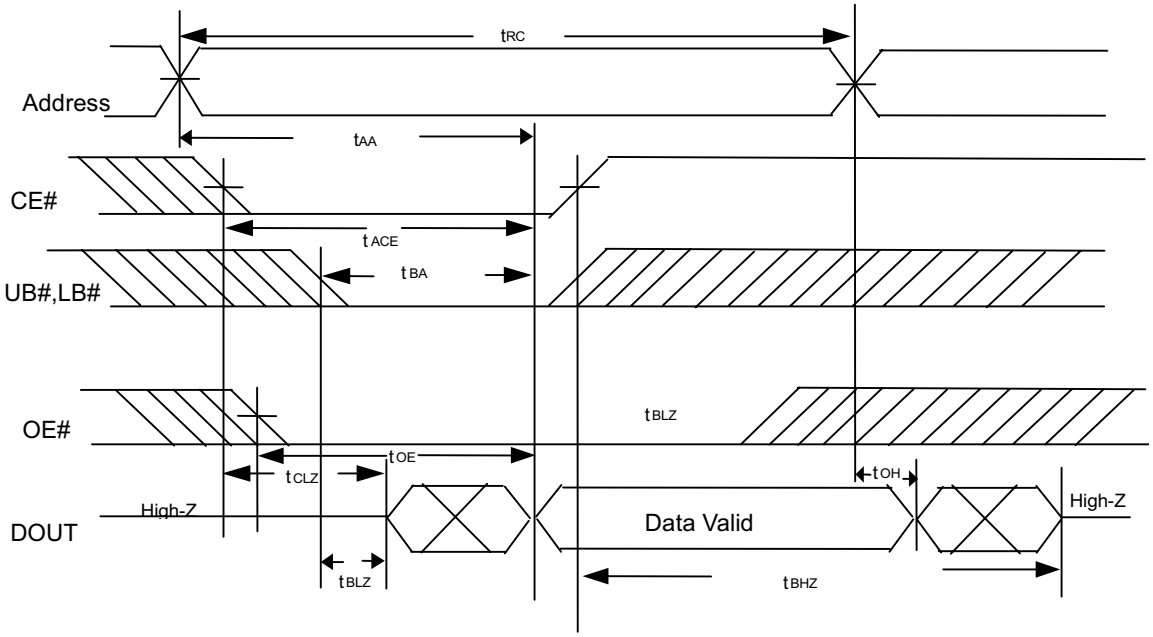
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)

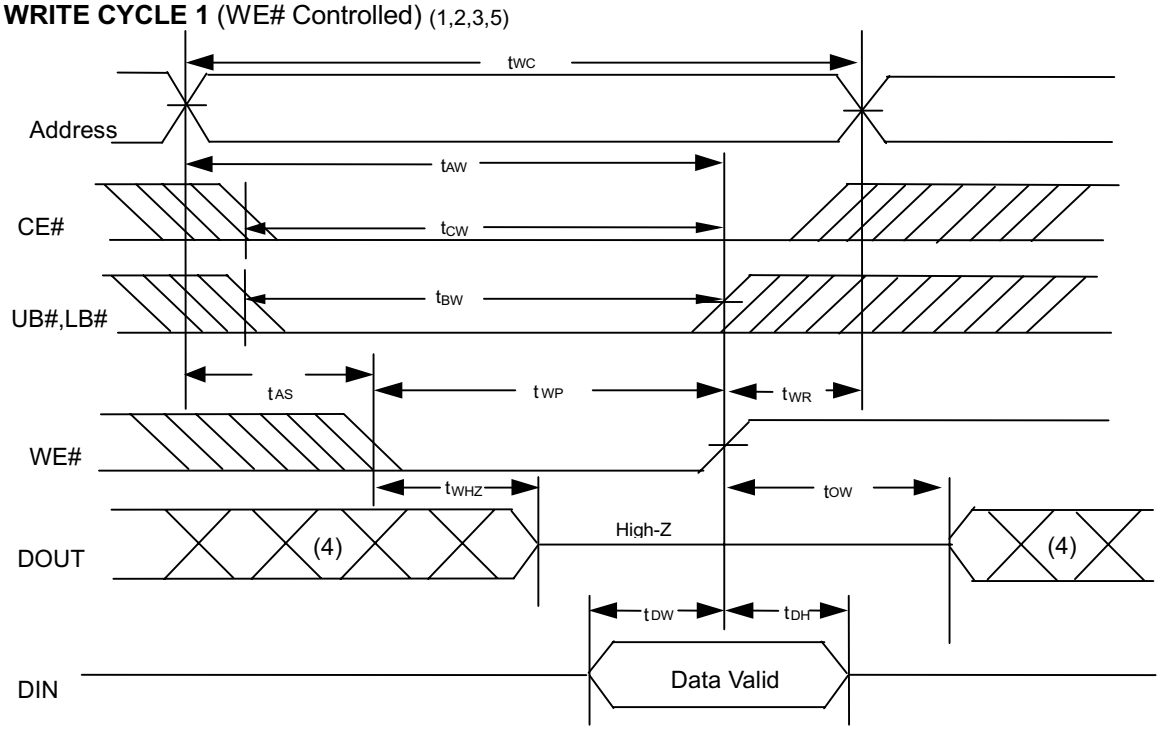


READ CYCLE 2 (CE#, OE# Controlled) (1,3,5,6)

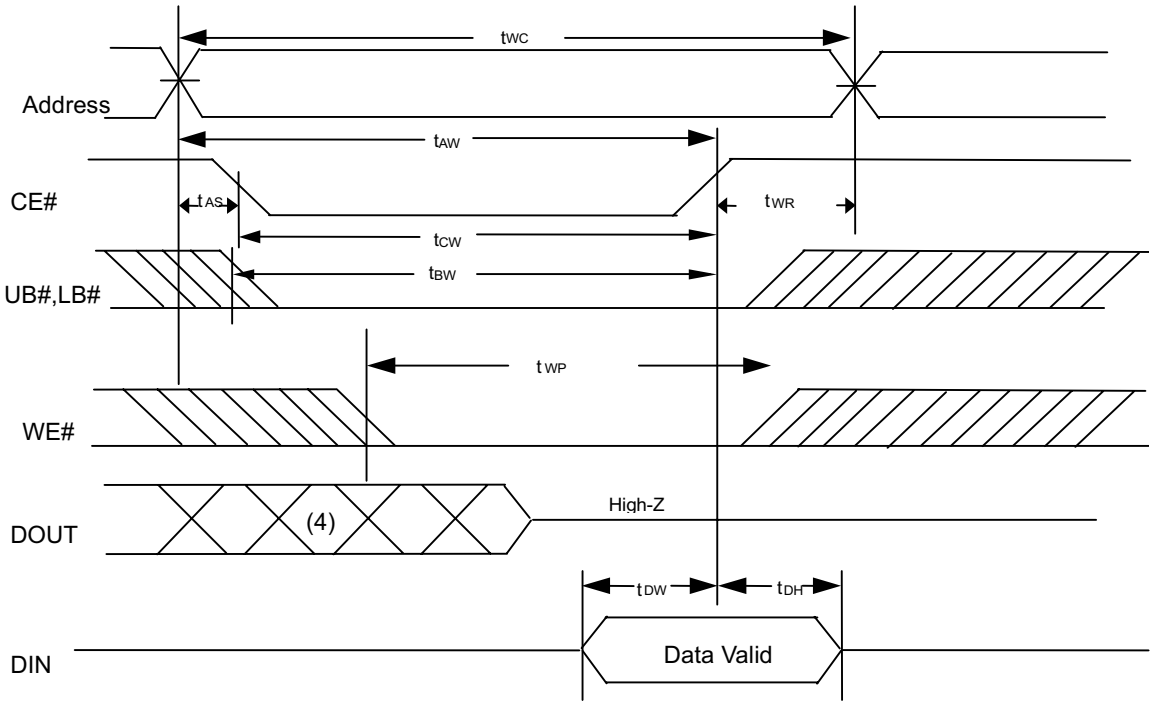


Notes :
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE#=V_{IL} and UB#=V_{IH} and ,LB#= V_{IL}
3. Address must be valid prior to or coincident with CE# and (UB# and, or LB#) transition now.
4. OE# = V_{IL}.
5. t_{CLZ} , t_{OLZ}, t_{CHZ}, and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)



WRITE CYCLE 2 (CE#) (1,2,5)

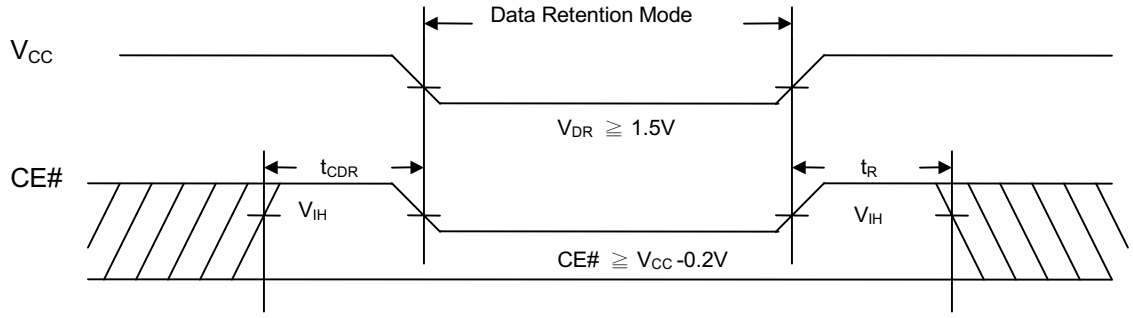


Notes :
1. WE# or CE# must be HIGH during all address transitions.
2. A write occurs during the overlap of a low CE# and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the CE# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = 0℃ to 70℃/-40℃ to 85℃(I))

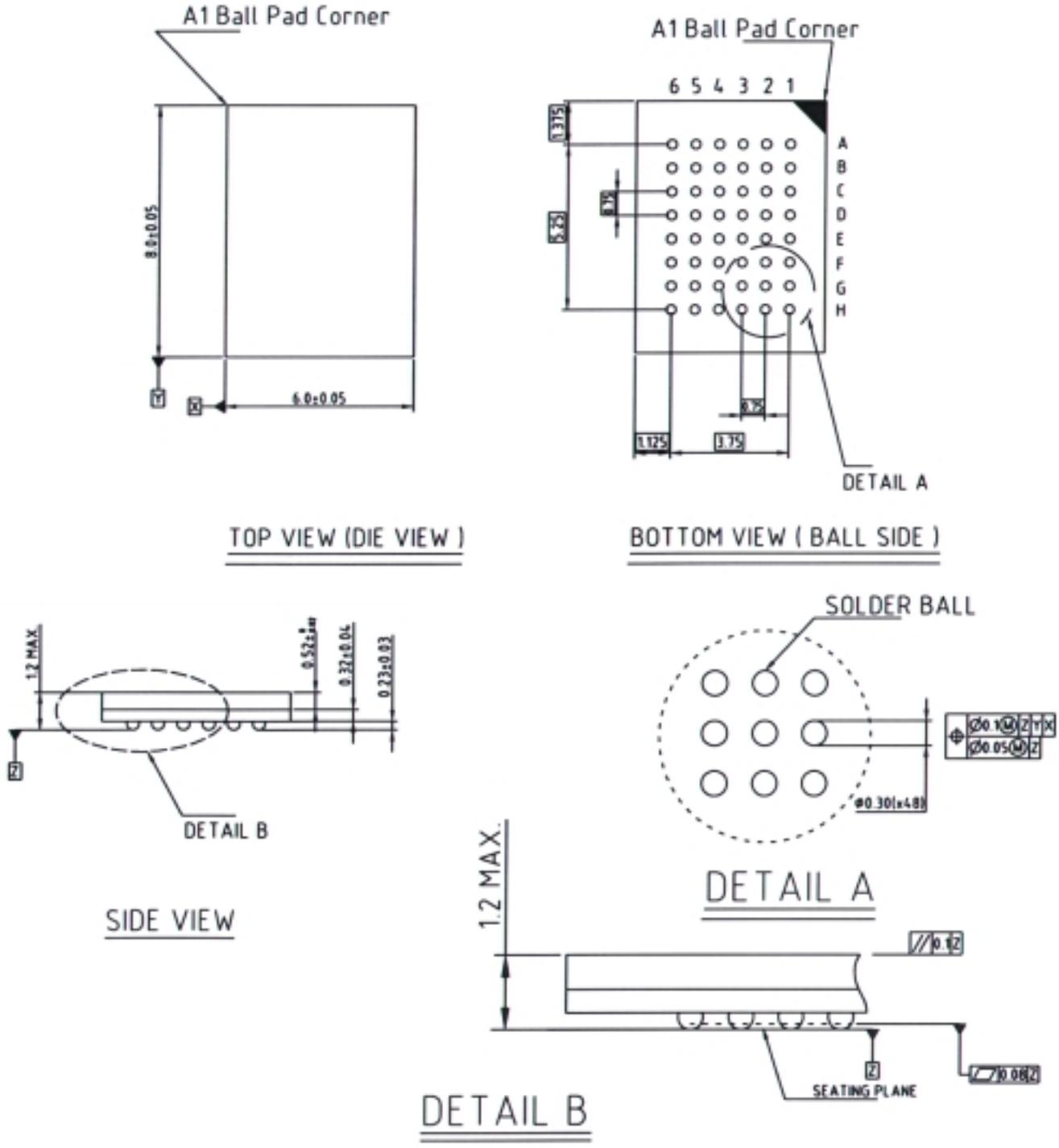
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	CE1# ≧ VCC-0.2V or CE2≦0.2V	1.5	-	-	V
Data Retention Current	I_{DR}	Vcc=1.5V CE1# ≧VCC-0.2V or CE2≦0.2V	-	-	10	uA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms(below)	0	-	-	ms
Recovery Time	t_R		5	-	-	ms

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION

48 BALL 6.0X8.0mm , 0.75mm BALL PITCH, TFBGA PACKAGE OUTLINE DIMENSION



ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) max	PACKAGE
UT62L12916BS-70L	70	80	48PIN BGA
UT62L12916BS-70LL	70	25	48PIN BGA
UT62L12916BS-100L	100	80	48PIN BGA
UT62L12916BS-100LL	100	25	48PIN BGA