High Speed Dual Low Side Driver

FEATURES

- **Two Independent Gate Drivers**
- **Wide Operating Range: 6.5V to 20V**
- **Input Voltages up to V_{CC}**
- **Compatible with 3.3V and 5V Logic Input**
- **Short Delay Time: 50ns at V_{CC} = 15V**
- **Output Rise and Fall Time of 25ns with 1000pF Load at V_{CC} = 15V**
- **Low Supply Current: 100μA at V_{CC} = 15V**
- **Leadfree, RoHS Compliant**

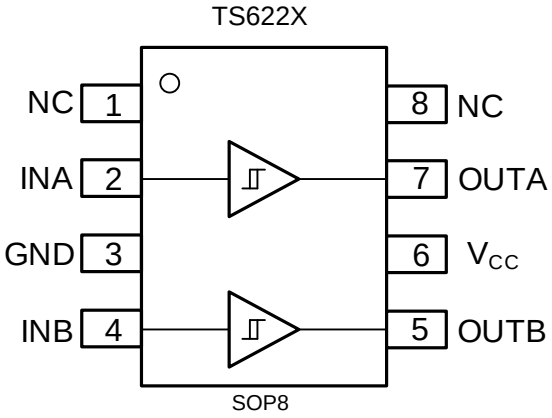
APPLICATIONS

- **Switching Mode Power Supplies**
- **Motor Drivers**
- **General Purpose Dual Low Side Drivers**

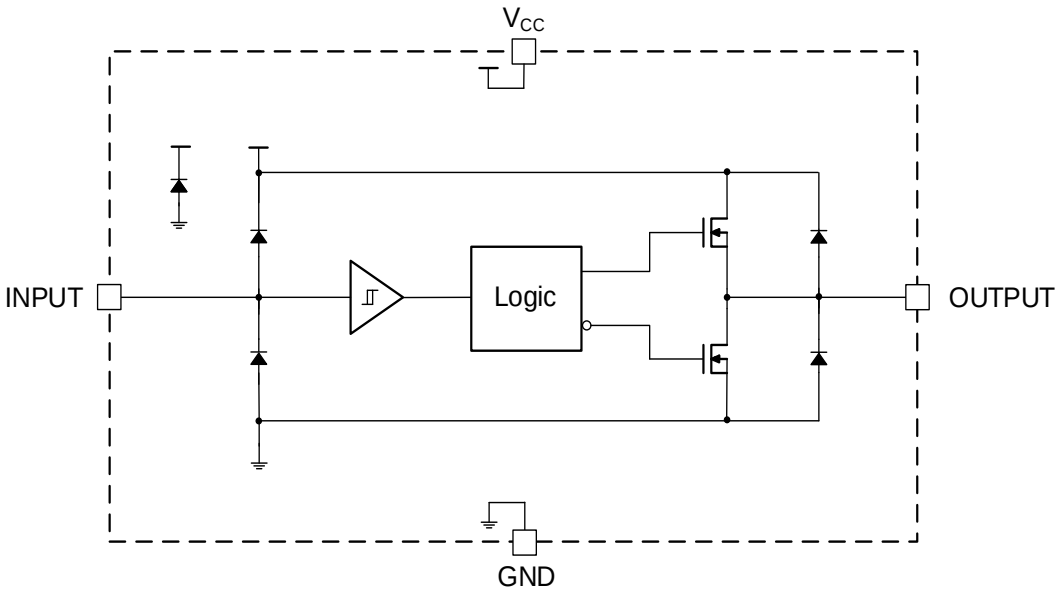
PRODUCT DESCRIPTION

The TS6226/TS6227/TS6228 family are dual channel, high speed power MOSFET and IGBT drivers, which are designed for applications that require low current signals to drive large capacitive loads with high speed. The input current is very low so that it is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum rise and fall time. Excellent latch immune performance is obtained.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Product	Part Number	Eco Plan	Package	Container, Pack Qty
TS622X	TS622XSOP8R	RoHS	SOP8	Reel, 2500

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

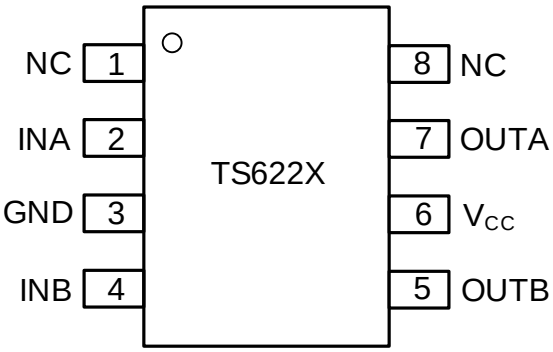
Parameter	Min	Max	Unit
V_{CC} to GND	-0.3	20	V
Input Voltage	-0.3	V_{CC} + 0.3	V
Output Voltage	-0.3	V_{CC} + 0.3	V
Logic Input Voltage	-0.3	V_{CC} + 0.3	V
Package Power Dissipation@ $T_A \leq 50°C$		500	mW
Thermal Resistance, Junction to Ambient		200	˚C/W
Junction Temperature	-40	150	˚C
Storage Temperature	-55	150	˚C
Lead Temperature (Soldering, 10s)		300	˚C
Operating Temperature	-40	125	˚C
ESD HBM	±4kV Class 3A（MIL-STD-883J Method 3015.9）		
ESD MM	±400V Class 3（JEDEC EIA/JESD22-A115）		
ESD CDM	±1500V Class C3（JEDEC EIA/JESD22-C101F）		
IC Latch-Up Test at Room Temperature	500mA @125˚C Class II, Level A （JEDEC STANDARD NO.78E NOVEMBER 2016）		

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

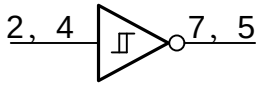
ESD CAUTION

ESD (Electrostatic Discharge) sensitive device Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjects to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

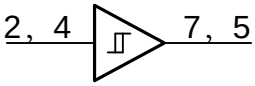


TS6226



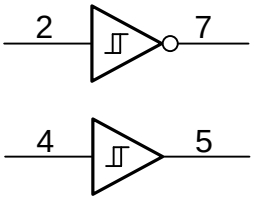
INVERTING

TS6227



NON-INVERTING

TS6228

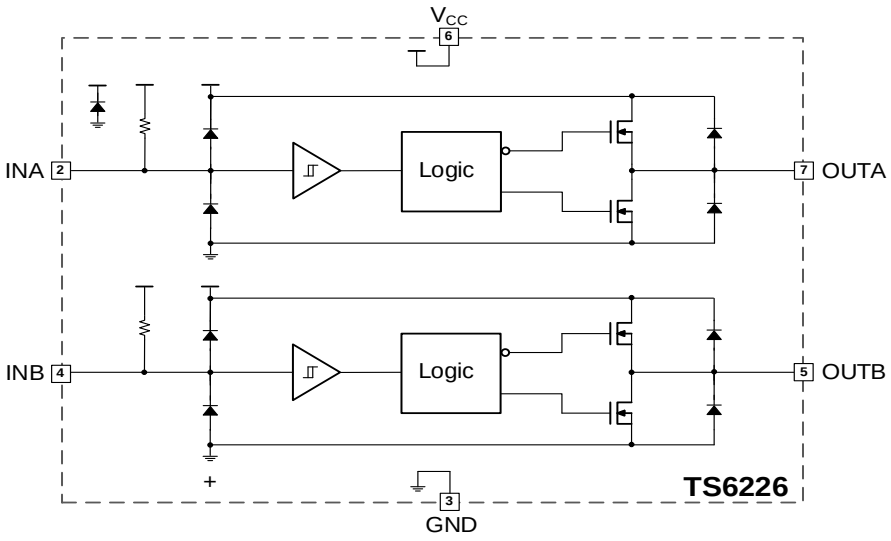


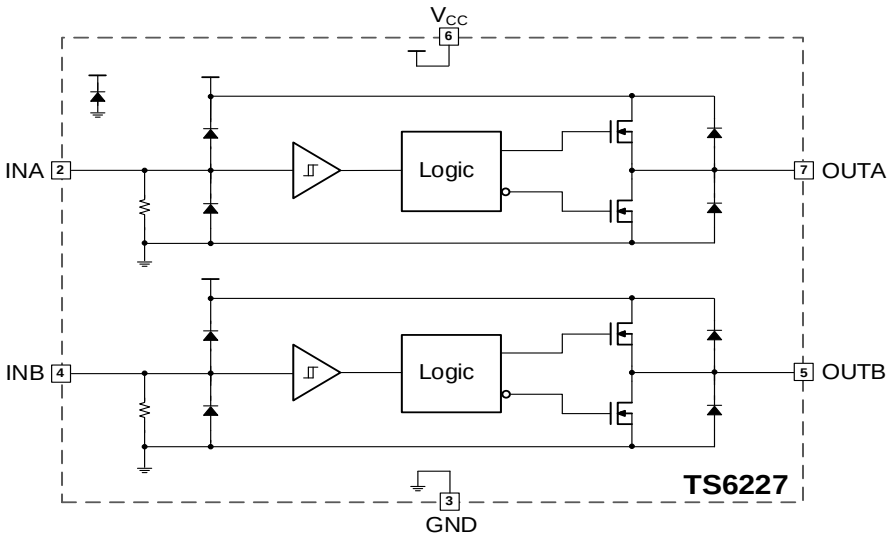
DIFFERENTIAL

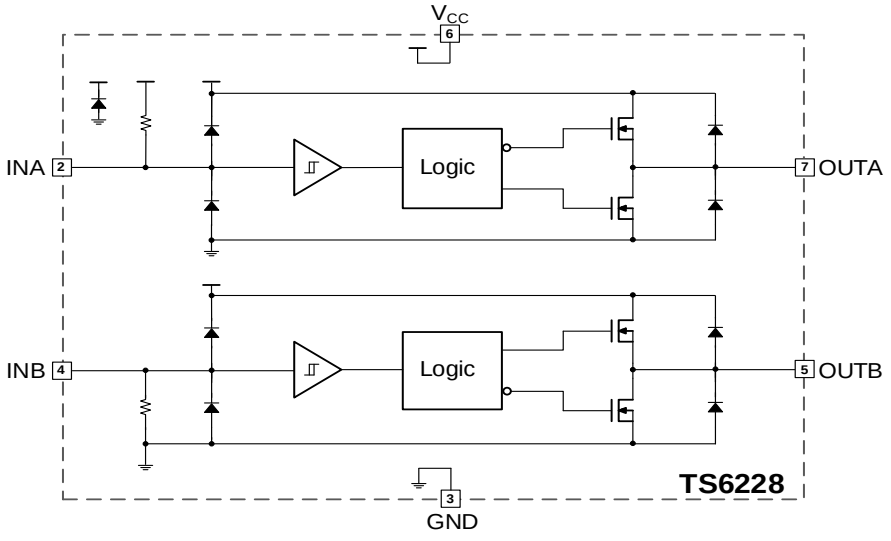
PIN DEFINITIONS

Pin No	Symbol	Function
1	NC	No Connection
2	INA	Logic Input of Channel A
3	GND	Ground
4	INB	Logic Input of Channel B
5	OUTB	Output of Channel B
6	V_{CC}	Power Supply
7	OUTA	Output of Channel A
8	NC	No Connection

BLOCK DIAGRAM







ELECTRICAL CHARACTERISTICS

At T_A = +25°C, and V_{CC} = 15V (unless otherwise noted)

Parameter		Testing Conditions	Min	Typ	Max	Unit
Power Supply						
I_{Q+}	Quiescent Supply Current	INA = INB = 5V		100	200	μA
I_{Q-}		INA = INB = 0V		80	180	
V_{CC_Clamp}	V_{CC} Zener Clamp Voltage	I_{Q+} = 5mA		22.0		V
Input Characteristics						
V_{IH}	Logic 1 Input Voltage		2.5			V
V_{IL}	Logic 0 Input Voltage				0.8	
I_{IN+}	Logic 1 Input Current	IN = 0V (TS6226) IN = 5V (TS6227) INA = 0V / INB = 5V (TS6228)		5	15	μA
I_{IN-}	Logic 0 Input Current	IN = 5V (TS6226) IN = 0V (TS6227) INA = 5V / INB = 0V (TS6228)	-30	-10		
Output Characteristics						
V_{OH_0mA}	High Output Voltage	I_O = 0mA	13.2			V
V_{OH_20mA}		I_O = 20mA		13.0		
V_{OH_60mA}		I_O = 60mA		12.6		
V_{OH_200mA}		I_O = 200mA		11.7		
V_{OL_20mA}	Low Output Voltage	I_O = 20mA			0.15	
V_{OL_60mA}		I_O = 60mA		0.06		
V_{OL_200mA}		I_O = 200mA		0.22		
I_{O+}	Peak Output Current	IN = 0V, OUT = 0V (TS6226) IN = 5V, OUT = 0V (TS6227) INA = 0V, OUTA = 0V (TS6228) INB = 5V, OUTB = 0V (TS6228)		2.3		A
I_{O-}		IN = 5V, OUT = V_{CC} (TS6226) IN = 0V, OUT = V_{CC} (TS6227) INA = 5V, OUTA = V_{CC} (TS6228) INB = 0V, OUTB = V_{CC} (TS6228)		3.3		
Switching Time Characteristics						
t_{on}	Turn-on Propagation Delay	Refer to Figure 10 & Figure 11		50	95	ns
t_{off}	Turn-off Propagation Delay			50	95	
t_r	Output Rise Time			25	55	
t_f	Output Fall Time			25	55	

TYPICAL CHARACTERISTICS

At V_{CC} = 15V, C_{LOAD} = 1000pF, T_A = 25°C (unless otherwise noted)

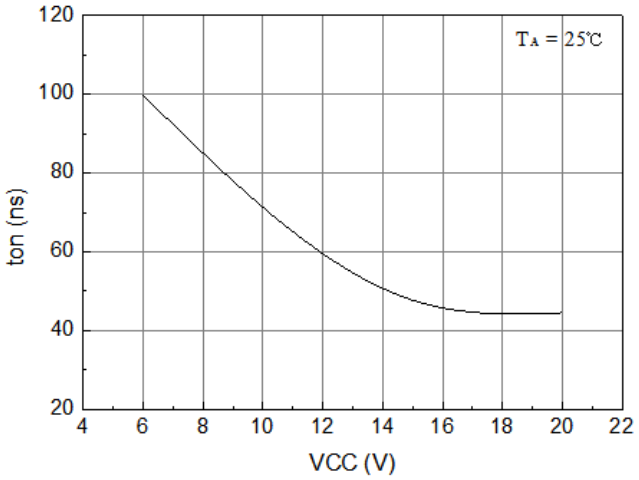


Figure 1. Turn-on Propagation Delay vs V_{CC}

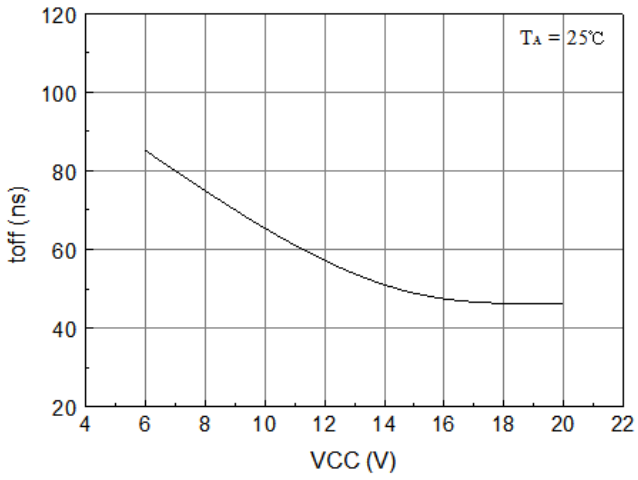


Figure 2. Turn-off Propagation Delay vs V_{CC}

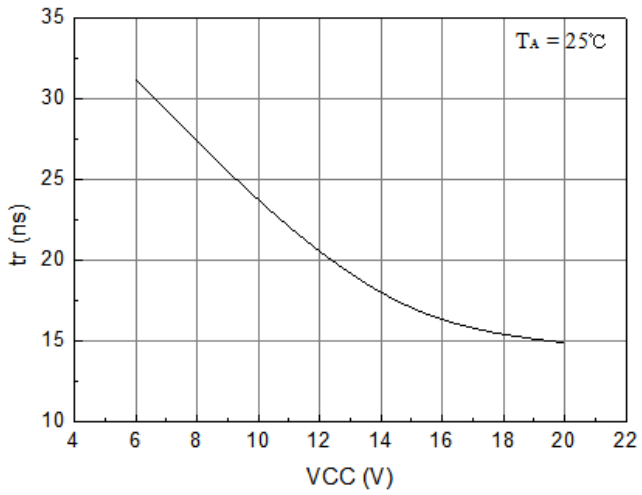


Figure 3. Output Rise Time vs V_{CC}

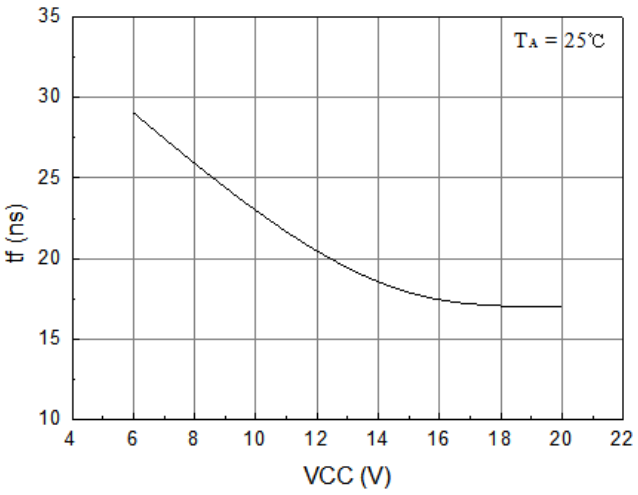


Figure 4. Output Fall Time vs V_{CC}

TYPICAL CHARACTERISTICS (CONTINUED)

At V_{CC} = 15V, C_{LOAD} = 1000pF, T_A = 25°C (unless otherwise noted)

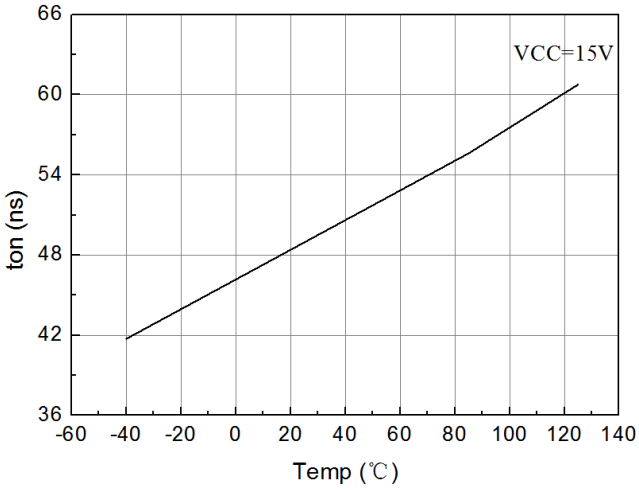


Figure 5. Turn-on Propagation Delay vs Temp

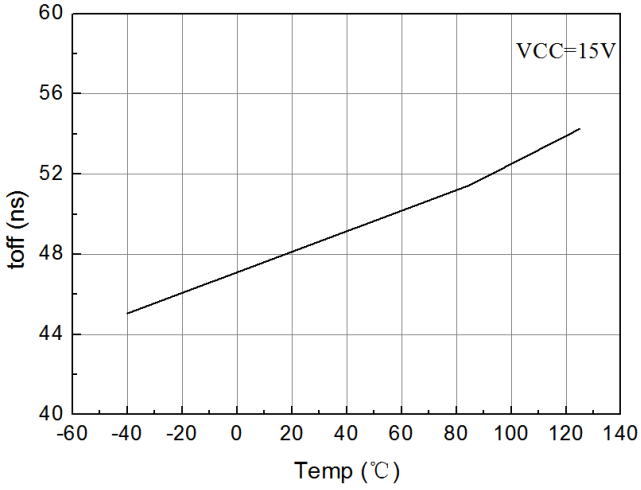


Figure 6. Turn-off Propagation Delay vs Temp

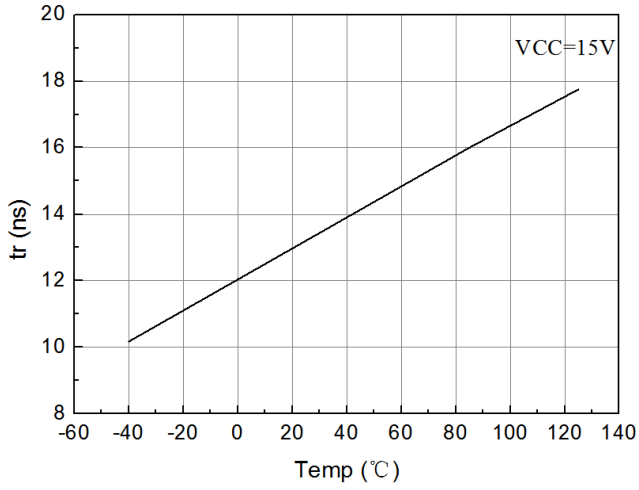


Figure 7. Output Rise Time vs Temp

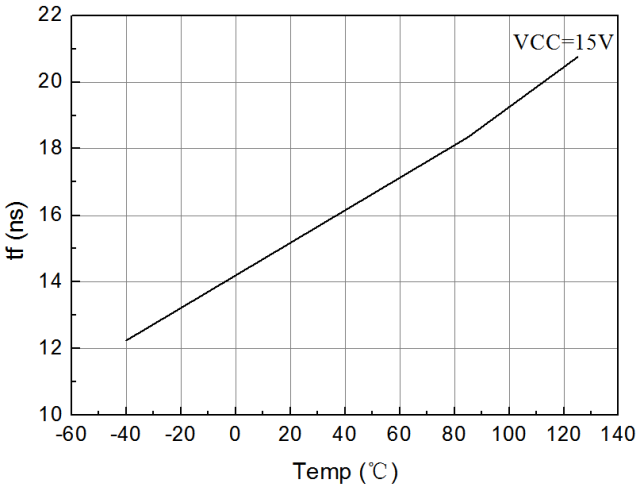


Figure 8. Output Fall Time vs Temp

APPLICATION NOTES & ADDITIONAL DETAILS

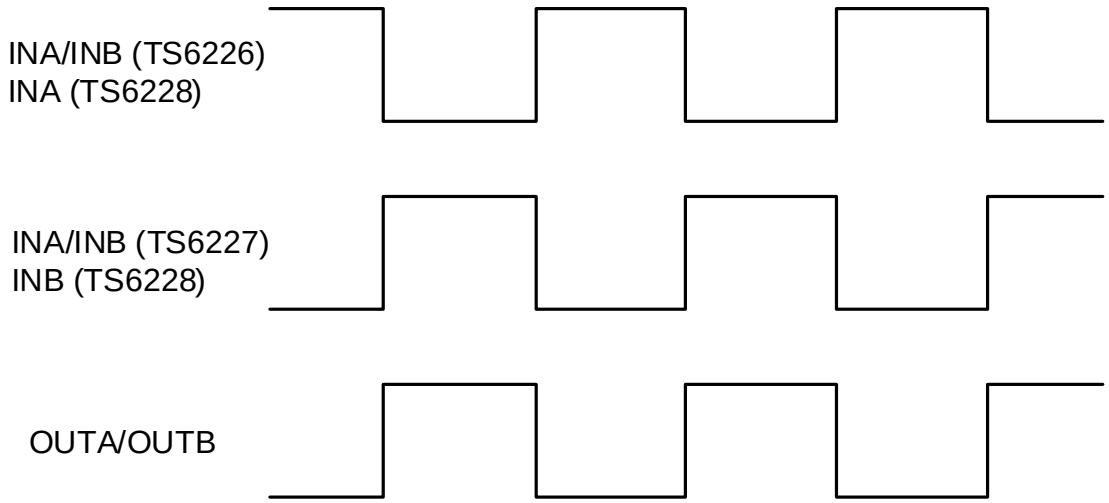


Figure 9. Input / Output Timing Diagram

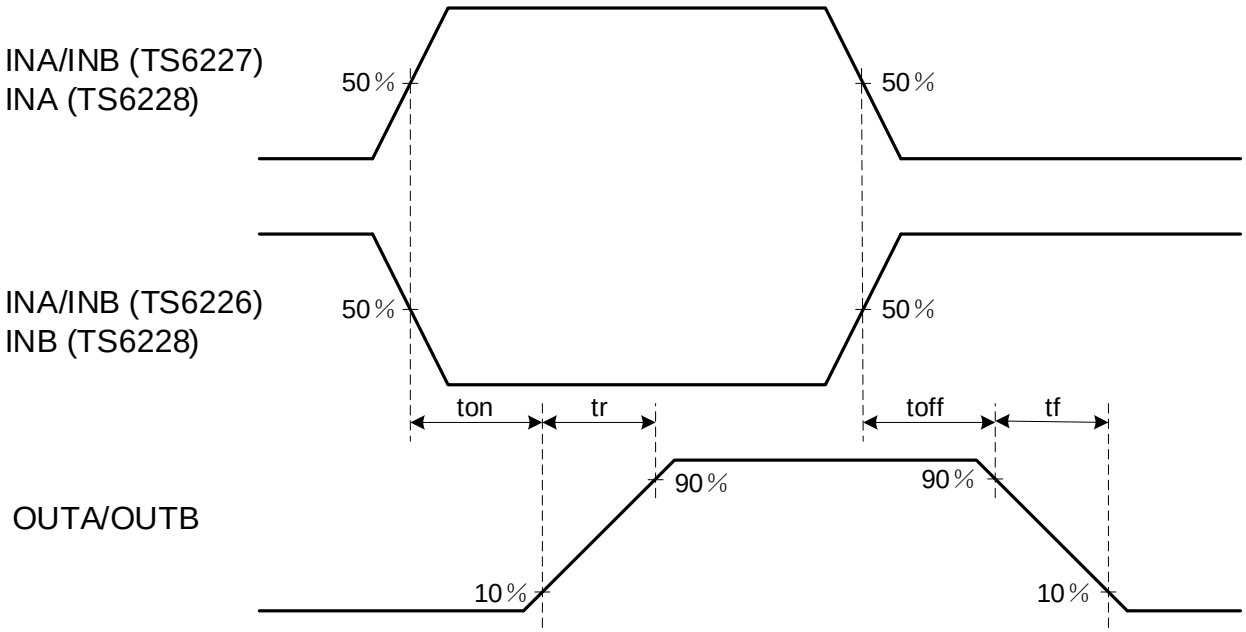


Figure 10. Switching Time Waveform Definitions

APPLICATION NOTES & ADDITIONAL DETAILS (CONTINUED)

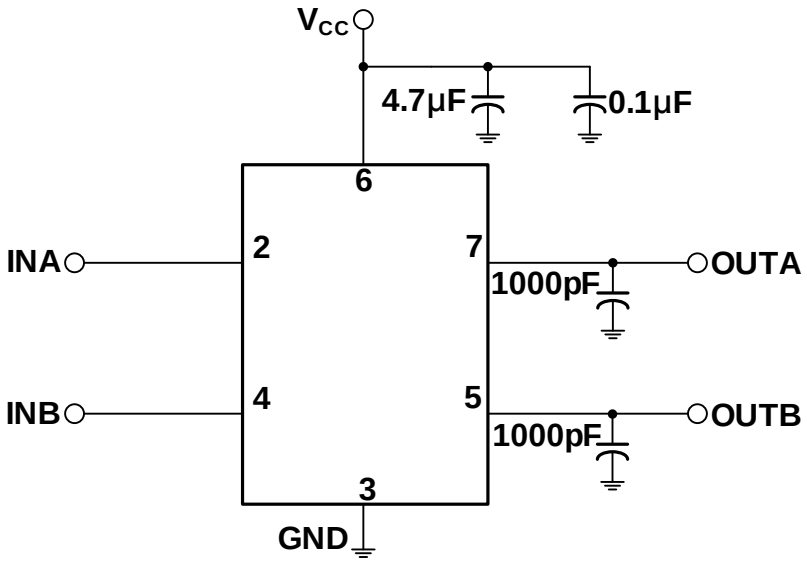
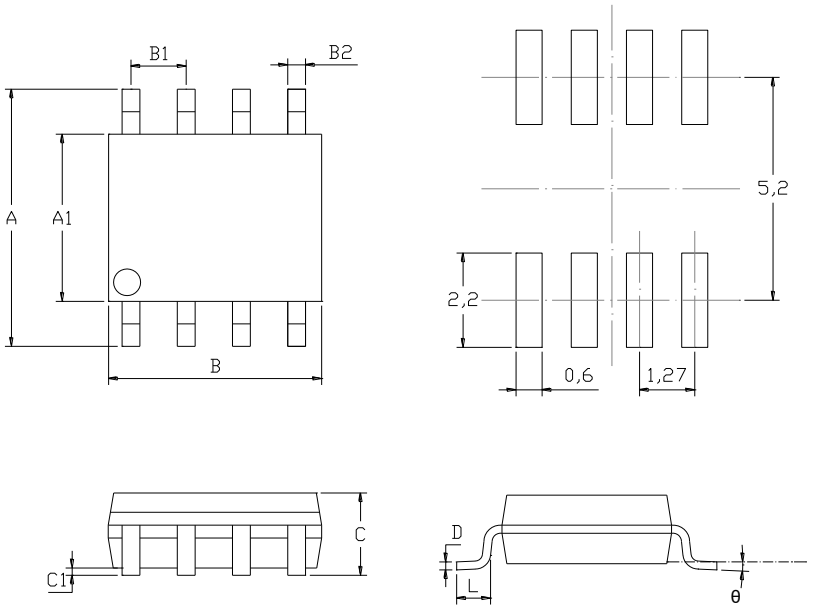


Figure 11. Test Circuit for Switching Time

MECHANICAL DIMENSIONS

SOP8 PACKAGE MECHANICAL DRAWING

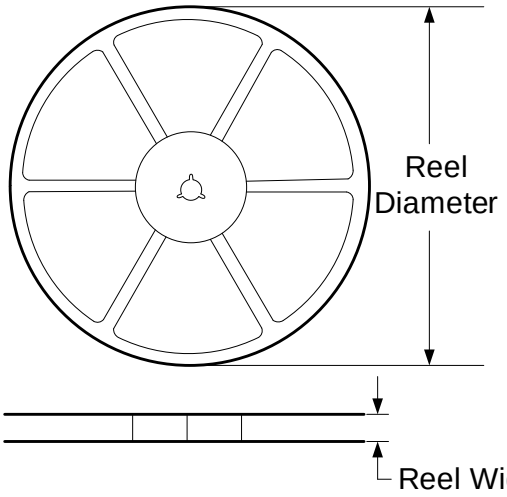


SOP8 PACKAGE MECHANICAL DATA

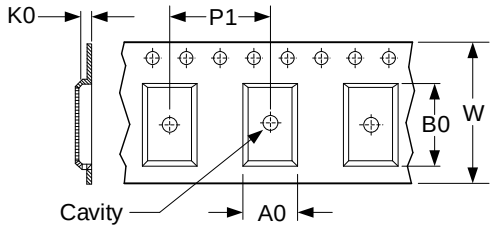
symbol	dimensions			
	millimeters		inches	
	min	max	min	max
A	5.800	6.200	0.228	0.244
A1	3.800	4.000	0.150	0.157
B	4.700	5.100	0.185	0.201
B1	1.270		0.050	
B2	0.330	0.510	0.013	0.020
C		1.750		0.069
C1	0.100	0.250	0.004	0.010
L	0.400	1.270	0.016	0.050
D	0.170	0.250	0.007	0.010
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS

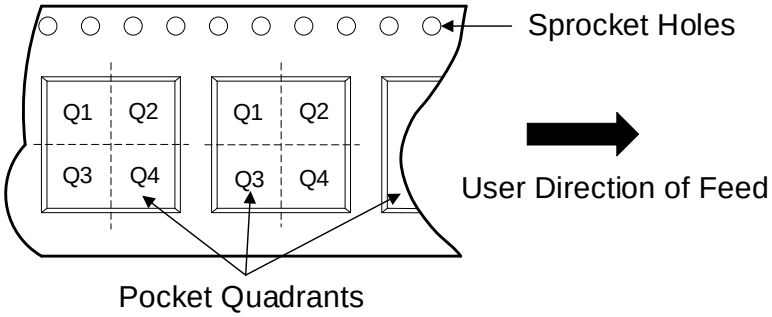


TAPE DIMENSIONS



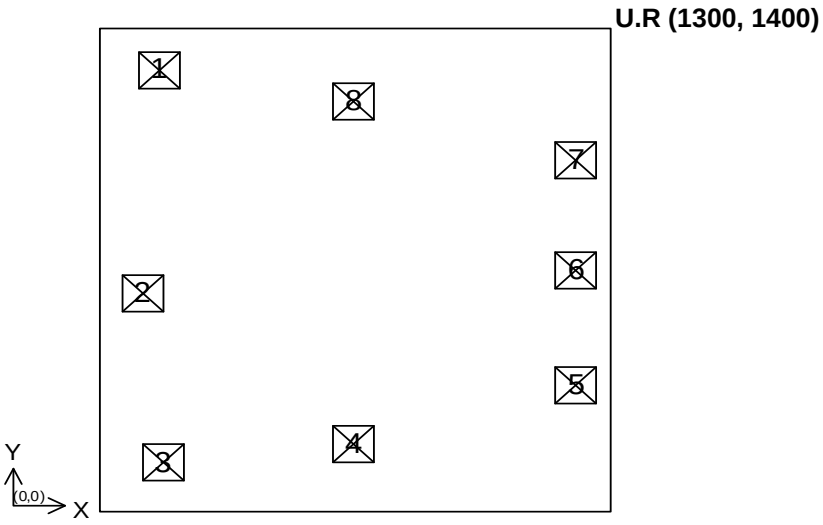
A0	Dimensioon designed to accommodate the component width
B0	Dimensioon designed to accommodate the component length
K0	Dimensioon designed to accommodate the component width thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadran
TS6226SOP8R	SOP8	8	2500	330.0	12.4	6.4	5.4	2.1	8.0	12.0	Q1
TS6227SOP8R	SOP8	8	2500	330.0	12.4	6.4	5.4	2.1	8.0	12.0	Q1
TS6228SOP8R	SOP8	8	2500	330.0	12.4	6.4	5.4	2.1	8.0	12.0	Q1

LAYOUT INFORMATION



Chip size: 1360 µm X 1460 µm (inclusive scribe)
User Pads: 80 µm X 80 µm
Scribe Lane width: 60 µm x 60 µm

PADS DESCRIPTION

PAD NO.	PAD NAME	DESCRIPTION	PAD LOCTION
1	INA	Input of Channel A	(134, 1306.5)
2	GND	Ground	(72.5, 639.5)
3	INB	Input of Channel B	(134, 93.5)
4	OUTB	Output of Channel B	(626, 171.5)
5	V_{CC}	Power Supply	(1217.5, 319)
6			(1217.5, 700)
7			(1217.5, 1081)
8	OUTA	Output of Channel A	(626, 1228.5)

REVISION HISTORY

NOTE: Page numbers for previous revisions may be different from that of the current version.

2020/9/8 — REV KY1.0.6 to REV KY1.0.7

Added notice to ABSOLUTE MAXIMUM RATINGS ……2
Updated the format of ELECTRICAL CHARACTERISTICS ……3
Delete DIP8 package ……1

2020/9/23 — REV KY1.0.7 to REV KY1.1.7

Added LAYOUT INFORMATION and PADS DESCRIPTION……12

2020/12/11 — REV KY1.1.7 to REV KY1.2.7

Updated Figure 10 ……8

CONTACT INFORMATION

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