

# ADS131A0x 双通道或四通道 24 位 128kSPS 同步采样 $\Delta$ - $\Sigma$ ADC

## 1 特性

- 双通道或四通道同步采样差分输入
- 数据速率：高达 128kSPS
- 高性能：
  - 单通道精度：在 10,000:1 动态范围内优于 0.1%
  - 有效分辨率：20.6位 (8kSPS)
  - 总谐波失真 (THD)：50Hz 和 60Hz 频率下为 -100dB
- 集成的负电荷泵 允许绝对输入电压低于接地值
- 灵活的模拟电源选项：
  - 采用负电荷泵：3.0V 至 3.45V
  - 单极电源：3.3V 至 5.5V
  - 双极电源： $\pm 2.5V$
- 数字电源：1.65V 至 3.6V
- 低温漂内部基准电压：6ppm/ $^{\circ}C$
- 模数转换器 (ADC) 自检
- 通信时的循环冗余校验 (CRC) 和汉明码错误校正
- 多个 SPI 数据接口模式：
  - 异步中断
  - 同步主从接口
- 封装：32 引脚 TQFP
- 工作温度范围： $-40^{\circ}C$  至  $+125^{\circ}C$

## 2 应用

- 电源保护：断路器和继电器保护
- 电能计量：单相、多相、电能质量
- 测试和测量
- 电池测试系统
- 数据采集系统

## 3 说明

ADS131A02 和 ADS131A04 器件为双通道和四通道同步采样 24 位  $\Delta\Sigma$  模数转换器 (ADC)。ADS131A02 或 ADS131A04 具有宽动态范围、最高 128kSPS 的可扩展数据速率以及内置故障监控器等特性，这使得它非常适合能源监控、电网保护和控制等应用。ADC 输入端可以单独直接接入电阻分压器网络、电流互感器或 Rogowski 线圈，以测量电压或电流。这两款器件具有灵活的电源选项（包括内部负电荷泵），可最大限度提高有效分辨率，非常适合宽动态范围应用。

这两款器件提供异步和同步主从接口选项，可为多个器件串联而成的单一系统灵活实施 ADC 配置。接口上配有多种接口检查、ADC 启动检查和数据完整性检查功能，可报告 ADC 中的错误以及数据传输期间的错误。

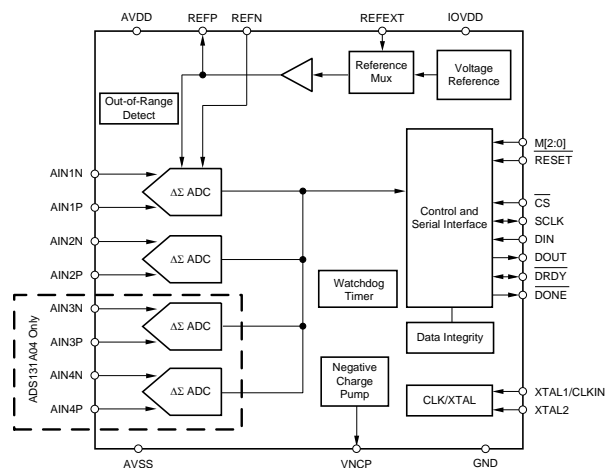
这种完整的模拟前端 (AFE) 解决方案采用 32 引脚 TQFP 封装，其额定工业温度范围为  $-40^{\circ}C$  至  $+125^{\circ}C$ 。

### 器件信息<sup>(1)</sup>

| 器件型号      | 封装        | 封装尺寸 (标称值)      |
|-----------|-----------|-----------------|
| ADS131A0x | TQFP (32) | 5.00mm x 5.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

### 简化框图



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4 修订历史记录

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| • 已更改 将文档标题从双通道或四通道 24 位同步采样 $\Delta-\Sigma$ ADC 更改为双通道或四通道 24 位 128kSPS 同步采样 $\Delta-\Sigma$ ADC  | 1    |
| • 已更改 $V_{AVDD}$ 改为 AVDD, $V_{AVSS}$ 改为 AVSS, $V_{GND}$ 改为 GND, 且 $V_{IOVDD}$ 改为 IOVDD (全文通改)  | 1    |
| • 已更改 特性部分   | 1    |
| • 已更改 说明 部分中)  | 1    |
| • Deleted footnote 2   | 6    |
| • Changed AVDD, AVSS, VNCP, and XTAL2 pin descriptions and footnote 1 for clarity  | 6    |
| • Changed CAP to GND Power supply voltage parameter specifications from $GND - 0.3 V$ to $0.3 V$ for the minimum specification and from $GND + 2.0 V$ to $2.0 V$ for the maximum specification | 7    |
| • Changed Analog input voltage parameter descriptions from REFEXT to AVDD to REFEXT and from REFN input to AVSS to REFN  | 7    |
| • Changed Digital input voltage parameter description to include the names of the digital input pins   | 7    |
| • Deleted CMRR footnote from Recommended Operating Conditions table  | 8    |
| • Added symbol to Reference input voltage parameter  | 8    |
| • Changed Offset drift parameter typical specification from $1.2 \mu V/^{\circ}C$ to $2.5 \mu V/^{\circ}C$ and maximum specification from $3 \mu V/^{\circ}C$ to $4 \mu V/^{\circ}C$           | 9    |
| • Changed Gain drift parameter typical specification from $0.25 \text{ ppm}/^{\circ}C$ to $0.5 \text{ ppm}/^{\circ}C$  | 9    |
| • Deleted separate AVDD PSRR specification for the ADS131A02   | 9    |

## 修订历史记录 (接下页)

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| • Changed <i>Reference buffer offset</i> parameter typical specification from 170 $\mu\text{V}$ to 250 $\mu\text{V}$ .....   | 9  |
| • Changed <i>Reference buffer offset drift</i> parameter typical specification from 1.1 $\mu\text{V}/^\circ\text{C}$ to 4 $\mu\text{V}/^\circ\text{C}$ and maximum specification from 4.3 $\mu\text{V}/^\circ\text{C}$ to 7 $\mu\text{V}/^\circ\text{C}$ ..... | 9  |
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| • Deleted <i>VNCP</i> parameter minimum specification and changed typical specification from $-1.95\text{ V}$ to $-2\text{ V}$ .....   | 10 |
| • Changed <i>Electrical Characteristics</i> table so all <i>Power-Supply</i> subsections are condensed to one <i>Power-Supply</i> subsection.....  | 10 |
| • Changed <i>free-air</i> to <i>ambient</i> in condition statements of <i>Timing Requirements</i> tables.....  | 12 |
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| • Changed <i>Input Overage and Underrange Detection</i> section for clarity .....  | 30 |
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| • Changed <i>External Reference Driver</i> figure.....   | 31 |
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**修订历史记录 (接下页)**

|   |    |
|---|----|
| • Changed first sentence of <i>Layout Example</i> section .....         | 83 |
| • Changed <i>ADS131A0x Layout Example</i> figure to improve layout..... | 83 |

**Changes from Revision B (September 2016) to Revision C**
**Page**

|   |    |
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| • 已更改 将文档标题从用于电源监视、控制和保护的模拟前端更改为同步采样 $\Delta\Sigma$ ADC.....  | 1  |
| • 已更改 将噪声性能特性 中第二个子项目符号从 <i>ENOB</i> 更改为有效分辨率.....  | 1  |
| • 已更改 有效位数改为有效分辨率 (说明部分) .....  | 1  |
| • Changed format of <i>Absolute Maximum Ratings</i> table; specification values did not change..... | 7  |
| • Changed title of <i>Multiple Device Effective Resolution Histogram</i> figure .....               | 17 |
| • Changed <i>Noise Measurements</i> section .....   | 22 |

**Changes from Revision A (March 2016) to Revision B**
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|  |    |
|--|----|
| • 将 ADS131A02 发布为生产数据 .....  | 1  |
| • Changed AC Performance, <i>PSRR</i> , <i>THD</i> , and <i>SFDR</i> parameters in <i>Electrical Characteristics</i> table: added rows for ADS131A02 and added ADS131A04 to rows specific to that device ..... | 9  |
| • Changed title of <a href="#">Figure 31</a> and <a href="#">Figure 32</a> : added ADS131A04 .....   | 20 |
| • Added <a href="#">Figure 33</a> and <a href="#">Figure 34</a> .....  | 21 |
| • Changed <i>Noise Measurements</i> section: changed <a href="#">Equation 1</a> , <a href="#">Equation 2</a> , <a href="#">Table 1</a> , and <a href="#">Table 3</a> .....                                     | 22 |
| • Added footnote to <a href="#">Figure 43</a> .....  | 31 |
| • Changed R2 and R3 values in footnote of <a href="#">Figure 44</a> .....  | 31 |
| • Changed <i>Cyclic Redundancy Check (CRC)</i> section .....   | 39 |
| • Changed description of M2 pin functionality in <i>Hamming Code Error Correction</i> section .....  | 40 |
| • Changed description of M0 pin functionality in <i>SPI Interface</i> section .....  | 42 |
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| • Changed <a href="#">Table 15</a> : changed register bits of row 00h, default setting and register bits of row 01h, and changed bits 2-0 of 11h, 12h, 13h, and 14h rows .....                                 | 55 |
| • Changed ID_MSB: ID Control Register MSB and ID_LSB: ID Control Register LSB registers .....  | 56 |
| • Changed bits 2-0 of all ADCx: ADC Channel Digital Gain Configuration Registers .....   | 66 |

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**Page**

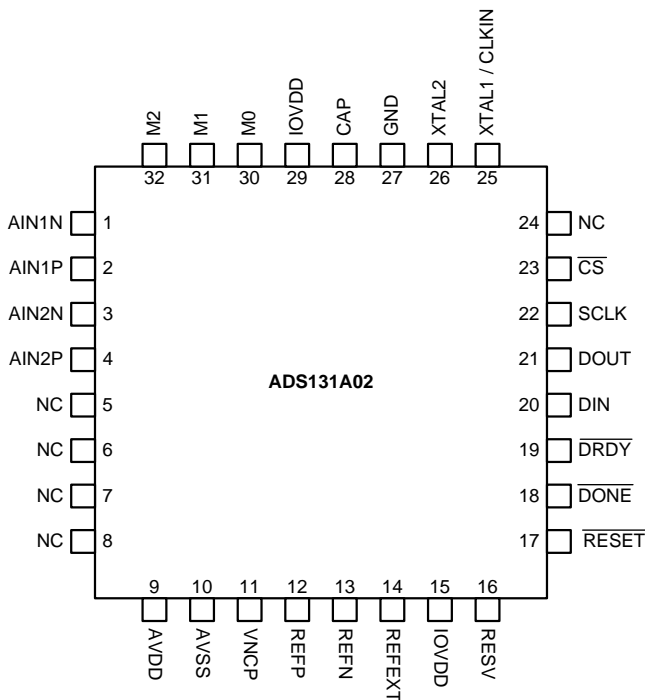
|                             |   |
|-----------------------------|---|
| • 将 ADS131A04 发布为生产数据 ..... | 1 |
|-----------------------------|---|

## 5 Device Comparison Table

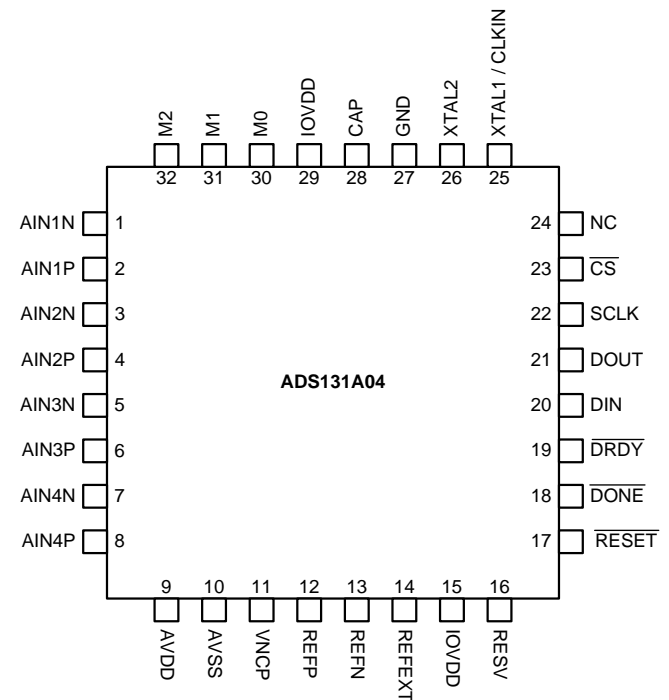
| PRODUCT   | NO. OF ADC CHANNELS | MAXIMUM SAMPLE RATE (kSPS) |
|-----------|---------------------|----------------------------|
| ADS131A02 | 2                   | 128                        |
| ADS131A04 | 4                   | 128                        |

## 6 Pin Configuration and Functions

**ADS131A02: PBS Package  
32-Pin TQFP  
Top View**



**ADS131A04: PBS Package  
32-Pin TQFP  
Top View**



### Pin Functions

| NAME            | PIN NO.   |           | I/O           | DESCRIPTION <sup>(1)</sup>   |
|-----------------|-----------|-----------|---------------|--|
|                 | ADS131A02 | ADS131A04 |               |  |
| AIN1N           | 1         | 1         | Analog input  | Negative analog input 1  |
| AIN1P           | 2         | 2         | Analog input  | Positive analog input 1  |
| AIN2N           | 3         | 3         | Analog input  | Negative analog input 2  |
| AIN2P           | 4         | 4         | Analog input  | Positive analog input 2  |
| AIN3N           | —         | 5         | Analog input  | Negative analog input 3  |
| AIN3P           | —         | 6         | Analog input  | Positive analog input 3  |
| AIN4N           | —         | 7         | Analog input  | Negative analog input 4  |
| AIN4P           | —         | 8         | Analog input  | Positive analog input 4  |
| AVDD            | 9         | 9         | Supply        | Positive analog power supply. Connect a 1- $\mu$ F capacitor to AVSS.              |
| AVSS            | 10        | 10        | Supply        | Negative analog power supply   |
| CAP             | 28        | 28        | Analog output | Digital low-dropout (LDO) regulator output. Connect a 1- $\mu$ F capacitor to GND. |
| $\overline{CS}$ | 23        | 23        | Digital input | Chip select; active low  |

(1) See the [Unused Inputs and Outputs](#) section for unused pin connections.

**Pin Functions (continued)**

| NAME                      | PIN       |           | I/O                  | DESCRIPTION <sup>(1)</sup>  |
|---------------------------|-----------|-----------|----------------------|---|
|                           | NO.       |           |                      |   |
|                           | ADS131A02 | ADS131A04 |                      |   |
| DIN                       | 20        | 20        | Digital input        | Serial data input   |
| $\overline{\text{DONE}}$  | 18        | 18        | Digital output       | Communication done signal; active low   |
| DOUT                      | 21        | 21        | Digital output       | Serial data output. Connect a 100-k $\Omega$ pullup resistor to IOVDD.  |
| $\overline{\text{DRDY}}$  | 19        | 19        | Digital input/output | Data ready; active low; host interrupt and synchronization for multi-devices  |
| GND                       | 27        | 27        | Supply               | Digital ground  |
| IOVDD                     | 15        | 15        | Supply               | Digital I/O supply voltage. Connect a 1- $\mu\text{F}$ capacitor to GND.  |
|                           | 29        | 29        |                      |   |
| M0 <sup>(2)</sup>         | 30        | 30        | Digital input        | Serial peripheral interface (SPI) configuration mode.<br>IOVDD: Asynchronous interrupt mode<br>GND: Synchronous master mode<br>No connection: Synchronous slave mode; use for multi-device mode |
| M1 <sup>(2)</sup>         | 31        | 31        | Digital input        | SPI word transfer size.<br>IOVDD: 32 bit<br>GND: 24 bit<br>No connection: 16 bit  |
| M2 <sup>(2)</sup>         | 32        | 32        | Digital input        | Hamming code enable.<br>IOVDD: Hamming code word validation on<br>GND: Hamming code word validation off<br>No connection: reserved; do not use  |
| NC                        | 5-8       | —         | —                    | Leave floating or connect directly to AVSS.   |
| NC                        | 24        | 24        | Digital output       | No connection   |
| REFEXT                    | 14        | 14        | Analog input         | Buffered external reference voltage input. Connect a 1- $\mu\text{F}$ capacitor to AVSS when using the internal reference.  |
| REFN                      | 13        | 13        | Analog input         | Negative reference voltage. Connect to AVSS.  |
| REFP                      | 12        | 12        | Analog output        | Positive reference voltage output. Connect a 1- $\mu\text{F}$ capacitor to REFN.  |
| $\overline{\text{RESET}}$ | 17        | 17        | Digital input        | System reset; active low  |
| RESV                      | 16        | 16        | Digital input        | Reserved pin; connect to IOVDD  |
| SCLK                      | 22        | 22        | Digital input/output | Serial data clock   |
| VNCP                      | 11        | 11        | Analog output        | Negative charge pump voltage output. Connect a 270-nF capacitor to AVSS when enabling the negative charge pump. Connect directly to AVSS if the negative charge pump is unused.                 |
| XTAL1/CLKIN               | 25        | 25        | Digital input        | Master clock input, crystal oscillator buffer input   |
| XTAL2                     | 26        | 26        | Digital output       | Crystal oscillator connection. Leave this pin unconnected if the crystal oscillator is unused.  |

(2) Mode signal states are latched following a power-on-reset (POR). Tie these pins high or low with a resistance less than 1-k $\Omega$  resistor.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

|                       |   | MIN         | MAX         | UNIT |
|-----------------------|---|-------------|-------------|------|
| Power supply voltage  | AVDD to AVSS (charge pump enabled)  | -0.3        | 3.6         | V    |
|                       | AVDD to AVSS (charge pump disabled)   | -0.3        | 6.0         |      |
|                       | IOVDD to GND  | -0.3        | 3.9         |      |
|                       | AVSS to GND   | -3.0        | 0.3         |      |
|                       | VNCP to AVSS  | -2.5        | 0.3         |      |
|                       | VNCP to AVDD  | -6.0        | 0.3         |      |
|                       | CAP to GND  | -0.3        | 2.0         |      |
| Analog input voltage  | Analog input voltage (charge pump enabled)  | AVSS - 1.65 | AVDD + 0.3  | V    |
|                       | Analog input voltage (charge pump disabled)   | AVSS - 0.3  | AVDD + 0.3  |      |
|                       | REFEXT  | AVSS - 0.3  | AVDD + 0.3  |      |
|                       | REFN  | AVSS - 0.05 | AVSS + 0.05 |      |
| Digital input voltage | $\overline{CS}$ , DIN, $\overline{DRDY}$ , $\overline{RESET}$ , SCLK, XTAL1/CLKIN, M0, M1, M2, RESV | GND - 0.3   | IOVDD + 0.3 | V    |
| Input current         | Continuous, any pin except supply pins  | -10         | 10          | mA   |
| Temperature           | Junction, T <sub>J</sub>  |             | 150         | °C   |
|                       | Storage, T <sub>stg</sub>   | -60         | 150         |      |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±1000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

|  |                                       |  |  | MIN                      | NOM                     | MAX                     | UNIT |
|--|---------------------------------------|--|--|--------------------------|-------------------------|-------------------------|------|
| <b>POWER SUPPLY</b>  |                                       |  |  |                          |                         |                         |      |
| <b>Negative Charge Pump Enabled (VNCPEN<sup>(1)</sup> = 1)</b> |                                       |  |  |                          |                         |                         |      |
| Analog supply voltage  | AVDD to AVSS                          |  |  | 3.0                      | 3.3                     | 3.45                    | V    |
|  | AVDD to GND                           |  |  | 3.0                      | 3.3                     | 3.45                    |      |
|  | AVSS to GND                           |  |  | -0.05                    | 0                       | 0.05                    |      |
| Digital supply voltage <sup>(2)</sup>                          | IOVDD to GND                          |  |  | 1.65                     | 3.3                     | 3.6                     | V    |
| <b>Negative Charge Pump Disabled (VNCPEN = 0)</b>              |                                       |  |  |                          |                         |                         |      |
| Analog supply voltage  | AVDD to AVSS                          |  |  | 3.0                      | 5.0                     | 5.5                     | V    |
|  | AVDD to GND                           |  |  | 1.5                      | 2.5                     | 5.5                     |      |
|  | AVSS to GND                           |  |  | -2.75                    | -2.5                    | 0.05                    |      |
| Digital supply voltage <sup>(2)</sup>                          | IOVDD to GND                          |  |  | 1.65                     | 3.3                     | 3.6                     | V    |
| <b>ANALOG INPUTS</b>   |                                       |  |  |                          |                         |                         |      |
| V <sub>IN</sub>  | Differential input voltage            | V <sub>IN</sub> = V <sub>AINxP</sub> - V <sub>AINxN</sub>            |  | -V <sub>REF</sub> / Gain |                         | V <sub>REF</sub> / Gain | V    |
| V <sub>CM</sub>  | Common-mode input voltage             |  |  | AVSS                     |                         | AVDD                    | V    |
| V <sub>AINxP</sub> , V <sub>AINxN</sub>                        | Absolute input voltage                | VNCPEN = 0   |  | AVSS                     |                         | AVDD                    | V    |
|  |                                       | VNCPEN = 1   |  | AVSS - 1.5               |                         | AVDD                    | V    |
| <b>EXTERNAL REFERENCE</b>                                      |                                       |  |  |                          |                         |                         |      |
| V <sub>REF</sub>   | Reference input voltage               | REFEXT - REFN  |  | 2.0                      | 2.5                     | AVDD - 0.5              | V    |
| V <sub>REFN</sub>  | Reference negative input              |  |  |                          | AVSS                    |                         | V    |
| V <sub>REFEXT</sub>  | External reference positive input     |  |  | V <sub>REFN</sub> + 2.0  | V <sub>REFN</sub> + 2.5 | AVDD - 0.5              | V    |
| <b>EXTERNAL CLOCK SOURCE</b>                                   |                                       |  |  |                          |                         |                         |      |
| f <sub>CLKIN</sub>   | External clock input frequency        | IOVDD > 2.7 V  |  | 0.4                      | 16.384                  | 25                      | MHz  |
|  |                                       | IOVDD ≤ 2.7 V  |  | 0.4                      | 8.192                   | 15.6                    |      |
|  | XTAL clock frequency <sup>(3)</sup>   |  |  |                          | 16.384                  | 16.5                    | MHz  |
| f <sub>SCLK</sub>  | SCLK input to derive f <sub>MOD</sub> | CLKSRC bit = 1, f <sub>SCLK</sub> = f <sub>CLK</sub> , IOVDD > 2.7 V |  | 0.2                      | 16.384                  | 25                      | MHz  |
|  |                                       | CLKSRC bit = 1, f <sub>SCLK</sub> = f <sub>CLK</sub> , IOVDD ≤ 2.7 V |  | 0.2                      | 8.192                   | 15.6                    |      |
| <b>DIGITAL INPUTS</b>  |                                       |  |  |                          |                         |                         |      |
|  | Digital input voltage                 |  |  | GND                      |                         | IOVDD                   | V    |
| <b>TEMPERATURE</b>   |                                       |  |  |                          |                         |                         |      |
| T <sub>A</sub>   | Operating ambient temperature         |  |  | -40                      |                         | 125                     | °C   |

(1) VNCPEN is bit 7 of the A\_SYS\_CFG register.

(2) Tie IOVDD to the CAP pin if IOVDD ≤ 2.0 V.

(3) Set IOVDD &gt; 3.0 V to use a crystal across the XTAL1/CLKIN and XTAL2 pins.

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ADS131A0x  | UNIT |
|-------------------------------|--|------------|------|
|                               |  | PBS (TQFP) |      |
|                               |  | 32 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 77.5       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 19.0       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 30.2       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 30.0       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A        | °C/W |

 (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.



## 7.5 Electrical Characteristics

Minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Typical specifications are at  $T_A = 25^\circ\text{C}$ . All specifications are at  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, and gain = 1 (unless otherwise noted).

| PARAMETER                 |                               | TEST CONDITIONS   | MIN  | TYP        | MAX | UNIT                         |
|---------------------------|-------------------------------|---|--|------------|-----|------------------------------|
| <b>ANALOG INPUTS</b>      |                               |   |  |            |     |                              |
| $C_s$                     | Input capacitance             |   |  | 3.5        |     | pF                           |
| $Z_{\text{in}}$           | Differential input impedance  | $f_{\text{MOD}} = 4.096\text{ MHz}$   |  | 130        |     | k $\Omega$                   |
| <b>ADC PERFORMANCE</b>    |                               |   |  |            |     |                              |
|                           | Resolution                    |   |  | 24         |     | Bits                         |
|                           | Gain                          |   | 1, 2, 4, 8, 16                                 |            |     |                              |
|                           | Data rate                     | $f_{\text{MOD}} = 4.096\text{ MHz}$   | 1  |            | 128 | kSPS                         |
| <b>DC PERFORMANCE</b>     |                               |   |  |            |     |                              |
| Dynamic range             |                               |   | 105  | 111        |     | dB                           |
|                           |                               | $\text{AVDD} - \text{AVSS} = 5\text{ V}$ , $V_{\text{REF}} = 4\text{ V}$ , $\text{VNCPEN}$ bit = 0                                    |  | 115        |     |                              |
|                           |                               | All other settings  | See <a href="#">Noise Measurements</a> section |            |     |                              |
| INL                       | Integral nonlinearity         | Best fit  |  | 8          | 20  | ppm                          |
|                           | Offset error                  |   |  | 500        |     | $\mu\text{V}$                |
|                           | Offset drift                  |   |  | 2.5        | 4   | $\mu\text{V}/^\circ\text{C}$ |
|                           | Gain error                    | Excluding voltage reference and reference buffer error  |  | $\pm 0.03$ |     | % of FS                      |
|                           | Gain drift                    | Excluding voltage reference and reference buffer error  |  | 0.5        | 2   | ppm/ $^\circ\text{C}$        |
| <b>AC PERFORMANCE</b>     |                               |   |  |            |     |                              |
| CMRR                      | Common-mode rejection ratio   | $f_{\text{CM}} = 50\text{ Hz}$ or $60\text{ Hz}$  |  | 100        |     | dB                           |
| PSRR                      | Power-supply rejection ratio  | $\text{AVDD}$ supply, $f_{\text{PS}} = 50\text{ Hz}$ and $60\text{ Hz}$   |  | 80         |     | dB                           |
|                           |                               | $\text{IOVDD}$ supply, $f_{\text{PS}} = 50\text{ Hz}$ and $60\text{ Hz}$  |  | 105        |     |                              |
|                           | Crosstalk                     | $f_{\text{IN}} = 50\text{ Hz}$ and $60\text{ Hz}$   |  | -125       |     | dB                           |
| SNR                       | Signal-to-noise ratio         | $f_{\text{IN}} = 50\text{ Hz}$ or $60\text{ Hz}$ , $V_{\text{REF}} = 2.442\text{ V}$ , $V_{\text{IN}} = -20\text{ dBFS}$ , normalized |  | 111        |     | dB                           |
|                           |                               | $f_{\text{IN}} = 50\text{ Hz}$ or $60\text{ Hz}$ , $V_{\text{REF}} = 4.0\text{ V}$ , $V_{\text{IN}} = -20\text{ dBFS}$ , normalized   |  | 115        |     |                              |
| THD                       | Total harmonic distortion     | $f_{\text{IN}} = 50\text{ Hz}$ or $60\text{ Hz}$ (up to 50 harmonics), $V_{\text{IN}} = -0.5\text{ dBFS}$ , ADS131A02                 |  | -101.5     |     | dB                           |
|                           |                               | $f_{\text{IN}} = 50\text{ Hz}$ or $60\text{ Hz}$ (up to 50 harmonics), $V_{\text{IN}} = -0.5\text{ dBFS}$ , ADS131A04                 |  | -103.5     |     |                              |
| SINAD                     | Signal-to-noise + distortion  | $f_{\text{IN}} = 50\text{ Hz}$ or $60\text{ Hz}$ (up to 50 harmonics), $V_{\text{IN}} = -0.5\text{ dBFS}$                             |  | 101        |     | dB                           |
| SFDR                      | Spurious-free dynamic range   | $f_{\text{IN}} = 50\text{ Hz}$ or $60\text{ Hz}$ (up to 50 harmonics), $V_{\text{IN}} = -0.5\text{ dBFS}$ , ADS131A02                 |  | 102.5      |     | dB                           |
|                           |                               | $f_{\text{IN}} = 50\text{ Hz}$ or $60\text{ Hz}$ (up to 50 harmonics), $V_{\text{IN}} = -0.5\text{ dBFS}$ , ADS131A04                 |  | 105        |     |                              |
| <b>EXTERNAL REFERENCE</b> |                               |   |  |            |     |                              |
|                           | Reference buffer offset       | $T_A = 25^\circ\text{C}$  |  | 250        |     | $\mu\text{V}$                |
|                           | Reference buffer offset drift | $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  |  | 4          | 7   | $\mu\text{V}/^\circ\text{C}$ |
|                           | REFEXT input impedance        |   |  | 50         |     | M $\Omega$                   |

## Electrical Characteristics (continued)

Minimum and maximum specifications apply from  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Typical specifications are at  $T_A = 25^{\circ}\text{C}$ . All specifications are at  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, and gain = 1 (unless otherwise noted).

| PARAMETER                                       |  | TEST CONDITIONS  |                | MIN       | TYP   | MAX       | UNIT          |
|---|--|--|----------------|-----------|-------|-----------|---------------|
| <b>INTERNAL REFERENCE VOLTAGE (REFP – REFN)</b> |  |  |                |           |       |           |               |
| $V_{\text{REF}}$                                | Reference output voltage                             | VREF_4V bit = 0  |                | 2.442     |       |           | V             |
|   |  | VREF_4V bit = 1, AVDD – AVSS > 4.5 V   |                | 4.0       |       |           |               |
|   | Accuracy   |  |                | ±0.1%     |       |           |               |
|   | Temperature drift                                    | Including reference buffer drift, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |                | 6         | 20    |           | ppm/°C        |
|   | Start-up time  | REFEXT = 1- $\mu\text{F}$ to AVSS, settled to 1%   |                | 0.2       |       |           | ms            |
|   |  | REFEXT = 1- $\mu\text{F}$ to AVSS, settled to 0.1%   |                | 1.2       |       |           |               |
|   |  | REFEXT = 1- $\mu\text{F}$ to AVSS, settled to 0.01%  |                | 250       |       |           |               |
|   | REFP source capability                               |  |                | 100       |       |           | $\mu\text{A}$ |
| <b>EXTERNAL CLOCK SOURCE</b>                    |  |  |                |           |       |           |               |
| $f_{\text{ICLK}}$                               | Internal ICLK frequency (SCLK output in master mode) | CLKSRC bit = 0   |                | 0.2       | 8.192 | 12.5      | MHz           |
| $f_{\text{MOD}}$                                | ADC modulator frequency                              | High-resolution mode   | VNCPEN bit = 0 | 0.1       | 4.096 | 4.25      | MHz           |
|   |  |  | VNCPEN bit = 1 | 0.512     | 4.096 | 4.25      |               |
|   |  | Low-power mode   | VNCPEN bit = 0 | 0.1       | 1.024 | 1.05      |               |
|   |  |  | VNCPEN bit = 1 | 0.512     | 1.024 | 1.05      |               |
| <b>DIGITAL INPUT/OUTPUT</b>                     |  |  |                |           |       |           |               |
| $V_{\text{IH}}$                                 | High-level input voltage                             |  |                | 0.8 IOVDD |       | IOVDD     | V             |
| $V_{\text{IL}}$                                 | Low-level input voltage                              |  |                | GND       |       | 0.2 IOVDD | V             |
| $V_{\text{OH}}$                                 | High-level output voltage                            | $I_{\text{OH}} = 1\text{ mA}$  |                | 0.8 IOVDD |       |           | V             |
| $V_{\text{OL}}$                                 | Low-level output voltage                             | $I_{\text{OL}} = -1\text{ mA}$   |                |           |       | 0.2 IOVDD | V             |
| $I_{\text{IN}}$                                 | Input current  | $0\text{ V} < V_{\text{Digital Input}} < \text{IOVDD}$                                     |                | -10       |       | 10        | $\mu\text{A}$ |
| <b>POWER-SUPPLY</b>                             |  |  |                |           |       |           |               |
| VNCP  | Negative charge pump output voltage                  |  |                | -2        | -1.65 |           | V             |
| AVDD current                                    | ADS131A02, high-resolution mode                      | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled                                     |                | 3.2       |       |           | mA            |
|   |  | Negative charge pump disabled  |                | 3         | 3.75  |           |               |
|   | ADS131A04, high-resolution mode                      | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled                                     |                | 4         |       |           |               |
|   |  | Negative charge pump disabled  |                | 4         | 4.7   |           |               |
|   | ADS131A02, low-power mode                            |  |                |           | 0.9   |           |               |
|   | ADS131A04, low-power mode                            |  |                |           | 1.1   |           |               |
| IOVDD current                                   | ADS131A02, high-resolution mode                      | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled                                     |                | 0.6       |       |           | mA            |
|   |  | Negative charge pump disabled  |                | 0.6       | 0.8   |           |               |
|   | ADS131A04, high-resolution mode                      | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled                                     |                | 0.8       |       |           |               |
|   |  | Negative charge pump disabled  |                | 0.8       | 1.0   |           |               |
|   | ADS131A02, low-power mode                            |  |                |           | 0.5   |           |               |
|   | ADS131A04, low-power mode                            |  |                |           | 0.5   |           |               |

## Electrical Characteristics (continued)

Minimum and maximum specifications apply from  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Typical specifications are at  $T_A = 25^\circ\text{C}$ . All specifications are at  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, and gain = 1 (unless otherwise noted).

| PARAMETER         | TEST CONDITIONS                                      |  | MIN | TYP  | MAX  | UNIT |
|-------------------|--|--|-----|------|------|------|
| Power dissipation | ADS131A02, high-resolution mode                      | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled |     | 12.5 |      | mW   |
|                   |  | Negative charge pump disabled                          |     | 17   | 21   |      |
|                   | ADS131A04, high-resolution mode                      | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled |     | 15.8 |      |      |
|                   |  | Negative charge pump disabled                          |     | 22.7 | 26.8 |      |
|                   | ADS131A02, low-power mode                            | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled |     | 4.6  |      |      |
|                   |  | Negative charge pump disabled                          |     | 6.5  |      |      |
|                   | ADS131A04, low-power mode                            | AVDD = 3.3 V, AVSS = 0 V, negative charge pump enabled |     | 5.3  |      |      |
|                   |  | Negative charge pump disabled                          |     | 7.2  |      |      |
|                   | Standby mode, $f_{\text{CLKIN}} = 16.384\text{ MHz}$ |  |     | 2.6  |      |      |

## 7.6 Timing Requirements: Asynchronous Interrupt Interface Mode

over operating ambient temperature range (unless otherwise noted)

|                        |  |                          | 1.65 V ≤ IOVDD ≤ 2.7 V |     | 2.7 V < IOVDD ≤ 3.6 V |     | UNIT |
|------------------------|--|--------------------------|------------------------|-----|-----------------------|-----|------|
|                        |  |                          | MIN                    | MAX | MIN                   | MAX |      |
| t <sub>c</sub> (CLKIN) | External clock period  | Single device            | 64                     |     | 40                    |     | ns   |
|                        |  | Multiple device chaining | 88                     |     | 56                    |     |      |
| t <sub>w</sub> (CP)    | Pulse duration, CLKIN high or low                                  | Single device            | 32                     |     | 20                    |     | ns   |
|                        |  | Multiple device chaining | 44                     |     | 28                    |     |      |
| t <sub>d</sub> (CSSC)  | Delay time, $\overline{CS}$ falling edge to first SCLK rising edge |                          | 16                     |     | 16                    |     | ns   |
| t <sub>d</sub> (SCS)   | Delay time, SCLK falling edge to $\overline{CS}$ falling edge      |                          | 5                      |     | 4                     |     | ns   |
| t <sub>c</sub> (SC)    | SCLK period  | Single device            | 64                     |     | 40                    |     | ns   |
|                        |  | Multiple device chaining | 88                     |     | 64                    |     |      |
| t <sub>w</sub> (SCHL)  | Pulse duration, SCLK high or low                                   | Single device            | 32                     |     | 20                    |     | ns   |
|                        |  | Multiple device chaining | 44                     |     | 32                    |     |      |
| t <sub>d</sub> (SCCS)  | Delay time, final SCLK falling edge to $\overline{CS}$ rising edge |                          | 5                      |     | 5                     |     | ns   |
| t <sub>su</sub> (DI)   | Setup time, DIN valid before SCLK falling edge                     |                          | 5                      |     | 5                     |     | ns   |
| t <sub>h</sub> (DI)    | Hold time, DIN valid after SCLK falling edge                       |                          | 8                      |     | 8                     |     | ns   |
| t <sub>w</sub> (CSH)   | Pulse duration, $\overline{CS}$ high                               |                          | 20                     |     | 15                    |     | ns   |
| t <sub>w</sub> (RSL)   | Pulse duration, $\overline{RESET}$ low                             |                          | 800                    |     | 800                   |     | ns   |

## 7.7 Switching Characteristics: Asynchronous Interrupt Interface Mode

over operating ambient temperature range (unless otherwise noted)

|                        |  |             | 1.65 V ≤ IOVDD ≤ 2.7 V |     | 2.7 V < IOVDD ≤ 3.6 V |     | UNIT             |
|------------------------|--|-------------|------------------------|-----|-----------------------|-----|------------------|
|                        |  |             | MIN                    | MAX | MIN                   | MAX |                  |
| t <sub>p</sub> (SCDOD) | Propagation delay time, first SCLK rising edge to DOUT driven                        |             |                        | 28  |                       | 15  | ns               |
| t <sub>p</sub> (SCDO)  | Propagation delay time, SCLK rising edge to valid new DOUT                           |             |                        | 26  |                       | 15  | ns               |
| t <sub>h</sub> (LSB)   | Hold time, last SCLK falling edge to DOUT 3-state                                    | HIZDLY = 00 | 6                      | 30  | 6                     | 20  | ns               |
|                        |  | HIZDLY = 01 | 8                      | 37  | 8                     | 27  |                  |
|                        |  | HIZDLY = 10 | 10                     | 43  | 10                    | 43  |                  |
|                        |  | HIZDLY = 11 | 12                     | 47  | 12                    | 47  |                  |
| t <sub>p</sub> (DN)    | Propagation delay time, SCLK falling edge to $\overline{DONE}$ falling edge          | DNDLY = 00  | 6                      | 33  | 6                     | 21  | ns               |
|                        |  | DNDLY = 01  | 8                      | 39  | 8                     | 27  |                  |
|                        |  | DNDLY = 10  | 10                     | 44  | 10                    | 32  |                  |
|                        |  | DNDLY = 11  | 12                     | 48  | 12                    | 36  |                  |
| t <sub>p</sub> (CSDN)  | Propagation delay time, $\overline{CS}$ rising edge to $\overline{DONE}$ rising edge |             |                        | 32  |                       | 32  | ns               |
| t <sub>p</sub> (CSDR)  | Propagation delay time, $\overline{CS}$ rising edge to $\overline{DRDY}$ rising edge |             |                        | 2.0 |                       | 2.0 | t <sub>CLK</sub> |
| t <sub>d</sub> (RSSC)  | Delay time, $\overline{RESET}$ rising edge to READY response                         |             | 4.5                    |     | 4.5                   |     | ms               |

## 7.8 Timing Requirements: Synchronous Master Interface Mode

over operating ambient temperature range (unless otherwise noted)

|                        |  |                          | 1.65 V ≤ IOVDD ≤ 2.7 V |     | 2.7 V < IOVDD ≤ 3.6 V |     | UNIT               |
|------------------------|--|--------------------------|------------------------|-----|-----------------------|-----|--------------------|
|                        |  |                          | MIN                    | MAX | MIN                   | MAX |                    |
| t <sub>c</sub> (CLKIN) | External clock period                          | Single device            | 64                     |     | 40                    |     | ns                 |
|                        |  | Multiple device chaining | 88                     |     | 56                    |     |                    |
| t <sub>w</sub> (CP)    | Pulse duration, CLKIN high or low              | Single device            | 32                     |     | 20                    |     | ns                 |
|                        |  | Multiple device chaining | 44                     |     | 28                    |     |                    |
| t <sub>c</sub> (SC)    | SCLK period                                    |                          | 2                      |     | 2                     |     | t <sub>CLKIN</sub> |
| t <sub>w</sub> (SCHL)  | Pulse duration, SCLK high or low               |                          | 1                      |     | 1                     |     | t <sub>CLKIN</sub> |
| t <sub>su</sub> (DI)   | Setup time, DIN valid before SCLK falling edge |                          | 5                      |     | 5                     |     | ns                 |
| t <sub>h</sub> (DI)    | Hold time, DIN valid after SCLK falling edge   |                          | 8                      |     | 8                     |     | ns                 |
| t <sub>w</sub> (RSL)   | Pulse duration, $\overline{\text{RESET}}$ low  |                          | 800                    |     | 800                   |     | ns                 |

## 7.9 Switching Characteristics: Synchronous Master Interface Mode

over operating ambient temperature range (unless otherwise noted)

|                        |  |             | 1.65 V ≤ IOVDD ≤ 2.7 V |     | 2.7 V < IOVDD ≤ 3.6 V |     | UNIT |
|------------------------|--|-------------|------------------------|-----|-----------------------|-----|------|
|                        |  |             | MIN                    | MAX | MIN                   | MAX |      |
| t <sub>p</sub> (SCDOD) | Propagation delay time, first SCLK rising edge to DOUT driven                      |             | 28                     |     | 15                    |     | ns   |
| t <sub>p</sub> (SCDO)  | Propagation delay time, SCLK rising edge to valid new DOUT                         |             | 26                     |     | 15                    |     | ns   |
| t <sub>p</sub> (SDR)   | Propagation delay time, SCLK falling edge to $\overline{\text{DRDY}}$ falling edge |             | 31                     |     | 20                    |     | ns   |
| t <sub>h</sub> (LSB)   | Hold time, last SCLK falling edge to DOUT 3-state                                  | HIZDLY = 00 | 6                      | 30  | 6                     | 20  | ns   |
|                        |  | HIZDLY = 01 | 8                      | 37  | 8                     | 27  |      |
|                        |  | HIZDLY = 10 | 10                     | 43  | 10                    | 43  |      |
|                        |  | HIZDLY = 11 | 12                     | 47  | 12                    | 47  |      |
| t <sub>p</sub> (DN)    | Propagation delay time, SCLK falling edge to $\overline{\text{DONE}}$ falling edge | DNDLY = 00  | 6                      | 33  | 6                     | 21  | ns   |
|                        |  | DNDLY = 01  | 8                      | 39  | 8                     | 27  |      |
|                        |  | DNDLY = 10  | 10                     | 44  | 10                    | 32  |      |
|                        |  | DNDLY = 11  | 12                     | 48  | 12                    | 36  |      |
| t <sub>p</sub> (CSDN)  | Propagation delay time, CS rising edge to $\overline{\text{DONE}}$ rising edge     |             | 32                     |     | 32                    |     | ns   |
| t <sub>p</sub> (DRS)   | Delay time, last SCLK rising edge to $\overline{\text{DRDY}}$ rising edge          |             | 17                     |     | 15                    |     | ns   |
| t <sub>d</sub> (RSSC)  | Delay time, $\overline{\text{RESET}}$ rising edge to READY response                |             | 4.5                    |     | 4.5                   |     | ms   |

## 7.10 Timing Requirements: Synchronous Slave Interface Mode

over operating ambient temperature range (unless otherwise noted)

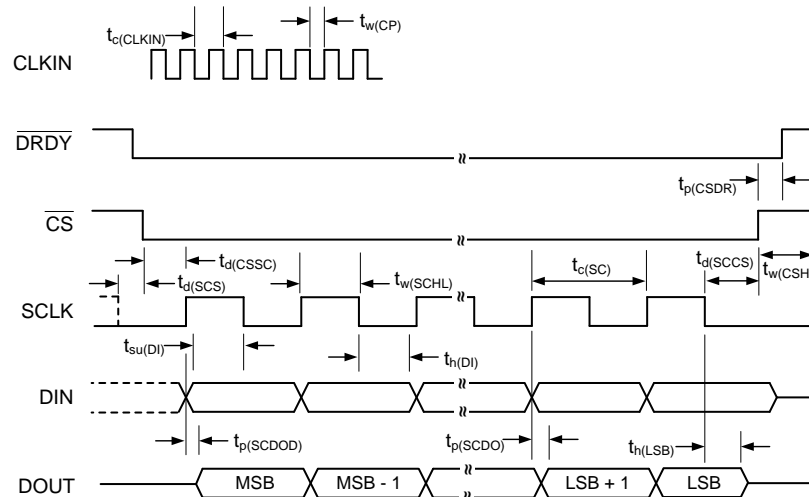
|                       |   |  | 1.65 V ≤ IOVDD ≤ 2.7 V |     | 2.7 V < IOVDD ≤ 3.6 V |     | UNIT |  |
|-----------------------|---|--|------------------------|-----|-----------------------|-----|------|--|
|                       |   |  | MIN                    | MAX | MIN                   | MAX |      |  |
| t <sub>c(CLKIN)</sub> | External clock period <sup>(1)</sup>                                    | Single device  | 64                     |     | 40                    |     | ns   |  |
|                       |   | Multiple device chaining   | 88                     |     | 56                    |     |      |  |
| t <sub>w(CP)</sub>    | Pulse duration, CLKIN high or low <sup>(1)</sup>                        | Single device  | 32                     |     | 20                    |     | ns   |  |
|                       |   | Multiple device chaining   | 44                     |     | 28                    |     |      |  |
| t <sub>d(SCS)</sub>   | Delay time, SCLK falling edge to $\overline{CS}$ falling edge           |  | 6                      |     | 4                     |     | ns   |  |
| t <sub>d(CSSC)</sub>  | Delay time, $\overline{CS}$ falling edge to first SCLK rising edge      |  | 16                     |     | 16                    |     | ns   |  |
| t <sub>c(SC)</sub>    | SCLK period   | Single device  | 64                     |     | 40                    |     | ns   |  |
|                       |   | Multiple device chaining   | 88                     |     | 64                    |     |      |  |
| t <sub>w(SCHL)</sub>  | Pulse duration, SCLK high or low  | Single device  | 32                     |     | 20                    |     | ns   |  |
|                       |   | Multiple device chaining   | 44                     |     | 32                    |     |      |  |
| t <sub>su(DI)</sub>   | Setup time, DIN valid before SCLK falling edge                          |  | 5                      |     | 5                     |     | ns   |  |
| t <sub>h(DI)</sub>    | Hold time, DIN valid after SCLK falling edge                            |  | 8                      |     | 6                     |     | ns   |  |
| t <sub>d(SCCS)</sub>  | Delay time, last SCLK falling edge to $\overline{CS}$ rising edge       |  | 5                      |     | 5                     |     | ns   |  |
| t <sub>su(sync)</sub> | Setup time, $\overline{DRDY}$ falling edge to master clock falling edge |  | 10                     |     | 10                    |     | ns   |  |
| t <sub>h(sync)</sub>  | Hold time, $\overline{DRDY}$ low after master clock falling edge        |  | 10                     |     | 10                    |     | ns   |  |
| t <sub>DATA</sub>     | Data rate period  | Set by the <a href="#">CLK1 register</a> and the <a href="#">CLK2 register</a> |                        |     |                       |     |      |  |
| t <sub>w(RSL)</sub>   | Pulse duration $\overline{RESET}$ low                                   |  | 800                    |     | 800                   |     | ns   |  |

(1) Only valid if CLKSRC = 0

## 7.11 Switching Characteristics: Synchronous Slave Interface Mode

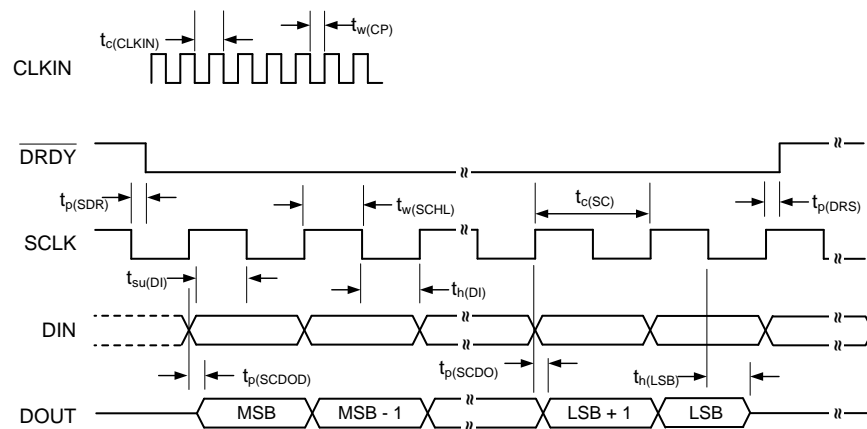
over operating ambient temperature range (unless otherwise noted)

|                       |  |             | 1.65 V ≤ IOVDD ≤ 2.7 V |     | 2.7 V < IOVDD ≤ 3.6 V |     | UNIT |
|-----------------------|--|-------------|------------------------|-----|-----------------------|-----|------|
|                       |  |             | MIN                    | MAX | MIN                   | MAX |      |
| t <sub>p(SCDOD)</sub> | Propagation delay time, first SCLK rising edge to DOUT driven                        |             | 28                     |     | 15                    |     | ns   |
| t <sub>p(SCDO)</sub>  | Propagation delay time, SCLK rising edge to valid new DOUT                           |             | 26                     |     | 15                    |     | ns   |
| t <sub>h(LSB)</sub>   | Hold time, last SCLK falling edge to DOUT 3-state                                    | HIZDLY = 00 | 6                      | 30  | 6                     | 20  | ns   |
|                       |  | HIZDLY = 01 | 8                      | 37  | 8                     | 27  |      |
|                       |  | HIZDLY = 10 | 10                     | 43  | 10                    | 43  |      |
|                       |  | HIZDLY = 11 | 12                     | 47  | 12                    | 47  |      |
| t <sub>p(DN)</sub>    | Propagation delay time, SCLK falling edge to $\overline{DONE}$ falling edge          | DNDLY = 00  | 6                      | 33  | 6                     | 21  | ns   |
|                       |  | DNDLY = 01  | 8                      | 39  | 8                     | 27  |      |
|                       |  | DNDLY = 10  | 10                     | 44  | 10                    | 32  |      |
|                       |  | DNDLY = 11  | 12                     | 48  | 12                    | 36  |      |
| t <sub>p(CSDN)</sub>  | Propagation delay time, $\overline{CS}$ rising edge to $\overline{DONE}$ rising edge |             | 32                     |     | 32                    |     | ns   |
| t <sub>d(RSSC)</sub>  | Delay time, $\overline{RESET}$ rising edge to READY response                         |             | 4.5                    |     | 4.5                   |     | ms   |



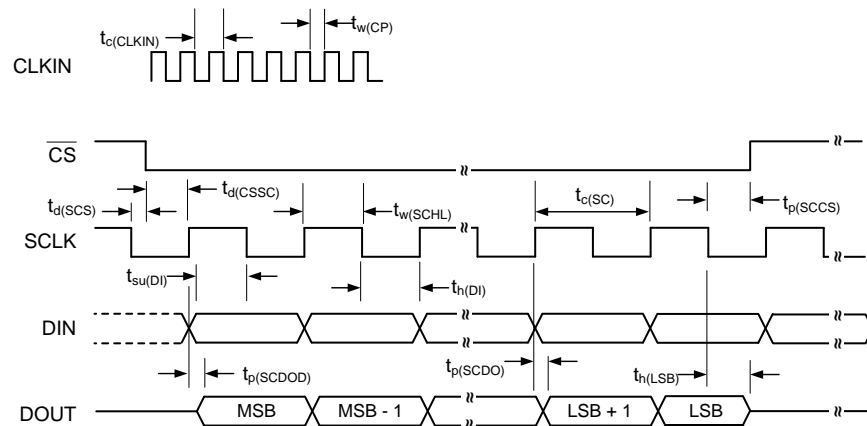
NOTE: SPI settings are CPOL = 0 and CPHA = 1.  $\overline{CS}$  transitions must take place when SCLK is low.

Figure 1. Asynchronous Interrupt Mode SPI Timing Diagram



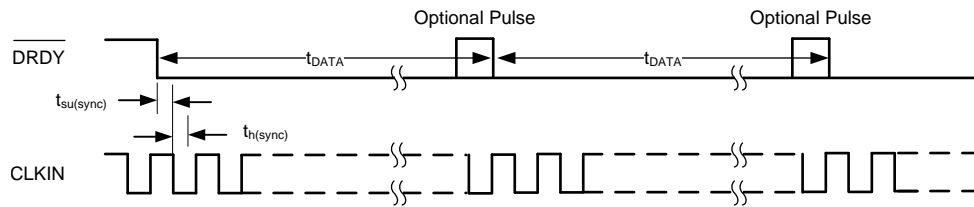
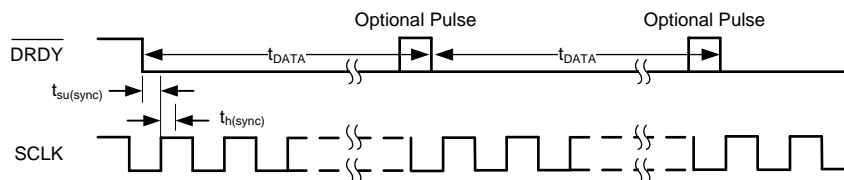
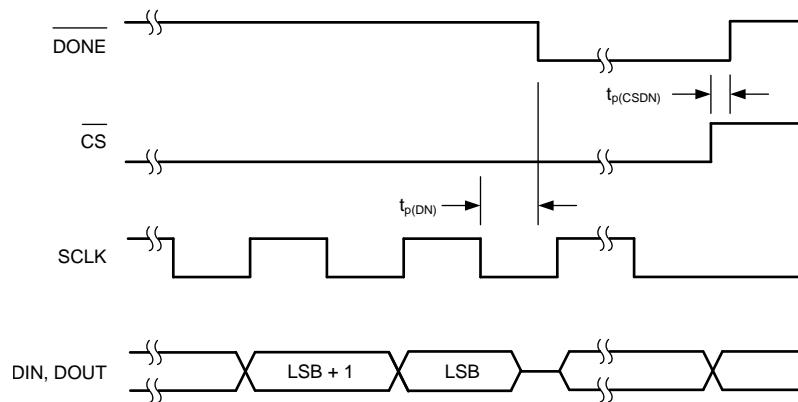
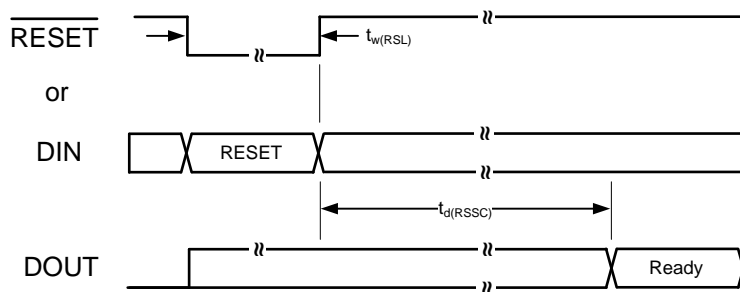
NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 2. Synchronous Master Mode SPI Timing Diagram



NOTE: SPI settings are CPOL = 0 and CPHA = 1.  $\overline{CS}$  can be tied directly to  $\overline{DRDY}$ .

Figure 3. Synchronous Slave Mode SPI Timing Diagram


**Figure 4.  $\overline{\text{DRDY}}$  Synchronization Timing for Synchronous Slave Mode (CLKSRC = 0)**

**Figure 5.  $\overline{\text{DRDY}}$  Synchronization Timing for Synchronous Slave Mode (CLKSRC = 1)**

**Figure 6.  $\overline{\text{DONE}}$  Signal Timing**

**Figure 7.  $\overline{\text{RESET}}$  Pin and Command Timing**



### 7.12 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)

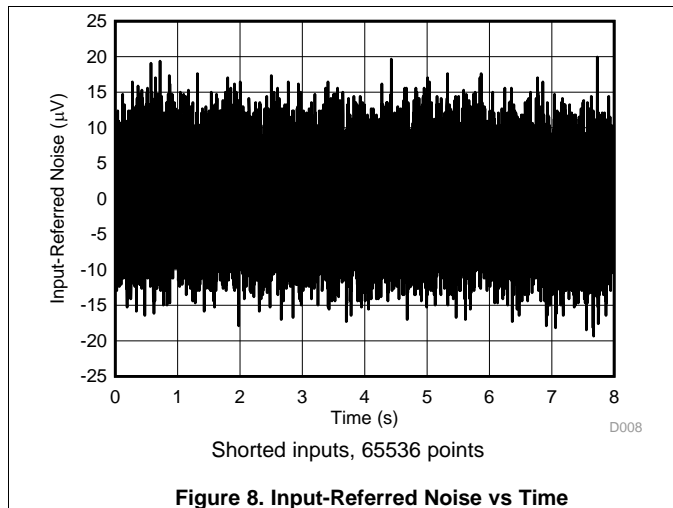


Figure 8. Input-Referred Noise vs Time

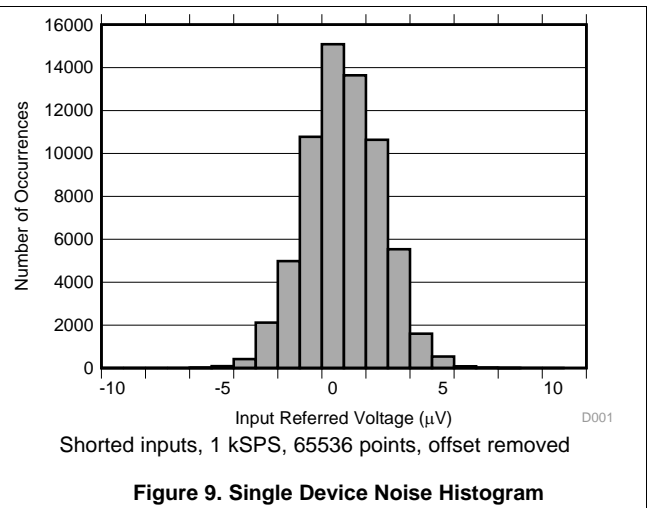


Figure 9. Single Device Noise Histogram

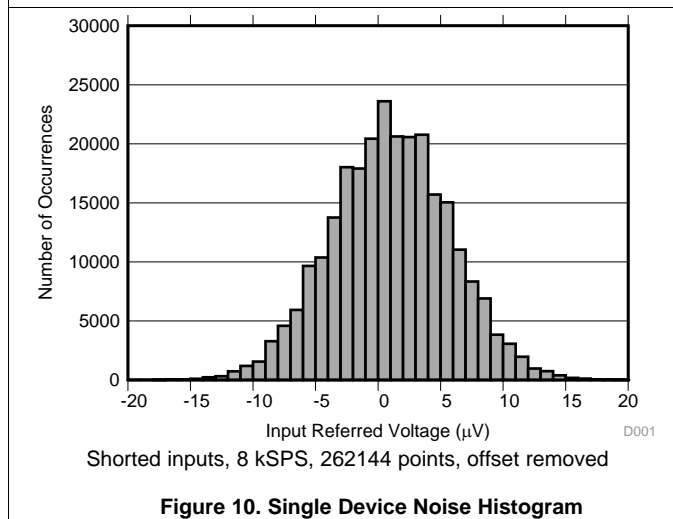


Figure 10. Single Device Noise Histogram

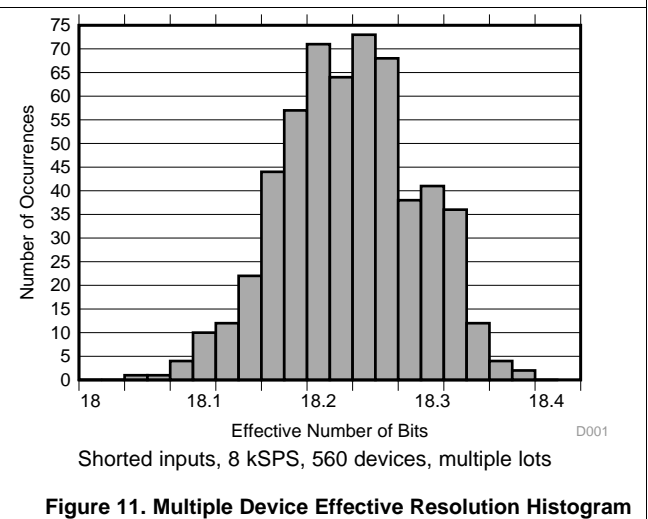


Figure 11. Multiple Device Effective Resolution Histogram

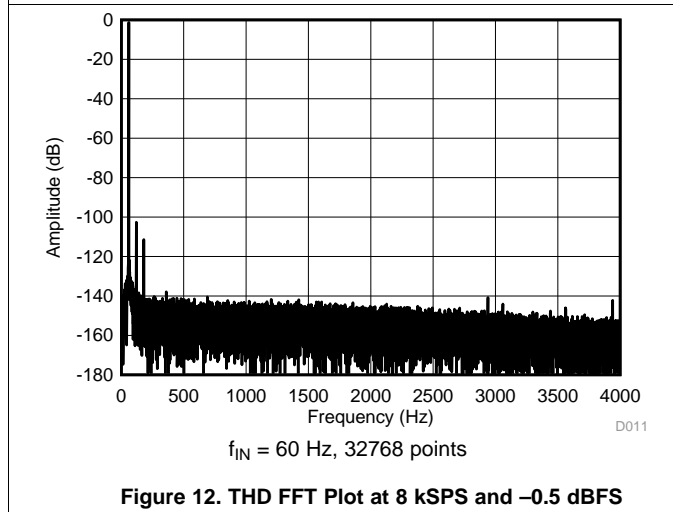


Figure 12. THD FFT Plot at 8 kSPS and  $-0.5\text{ dBFS}$

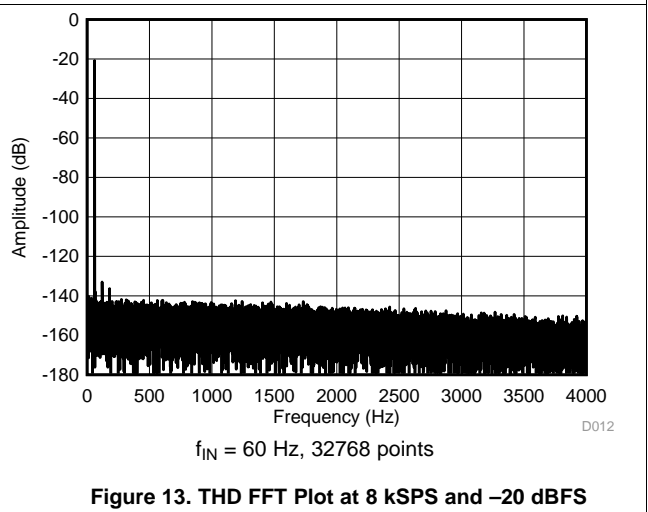


Figure 13. THD FFT Plot at 8 kSPS and  $-20\text{ dBFS}$

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)

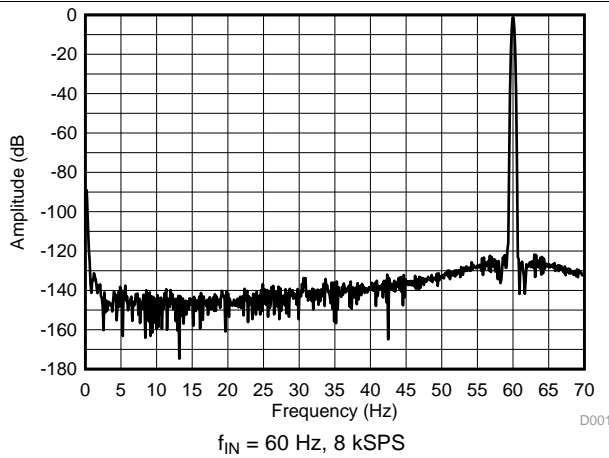


Figure 14. Low-Frequency FFT Plot

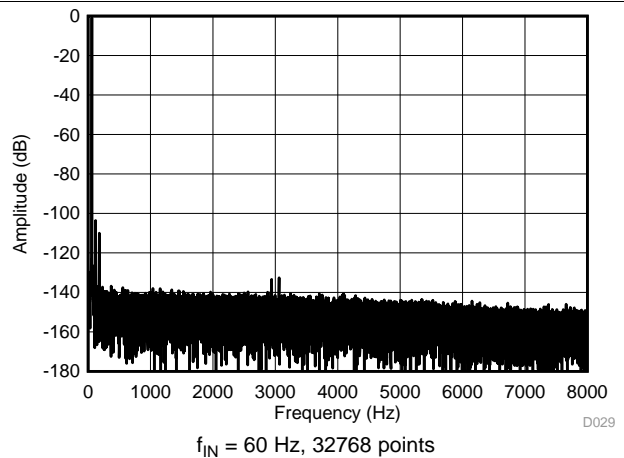


Figure 15. THD FFT Plot at 16 kSPS and -0.5 dBFS

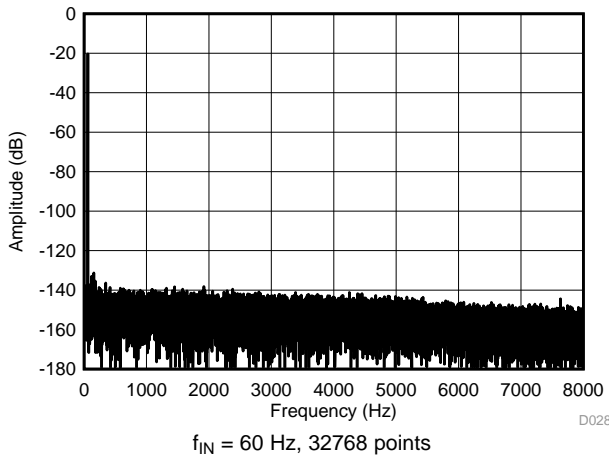


Figure 16. THD FFT Plot at 16 kSPS and -20 dBFS

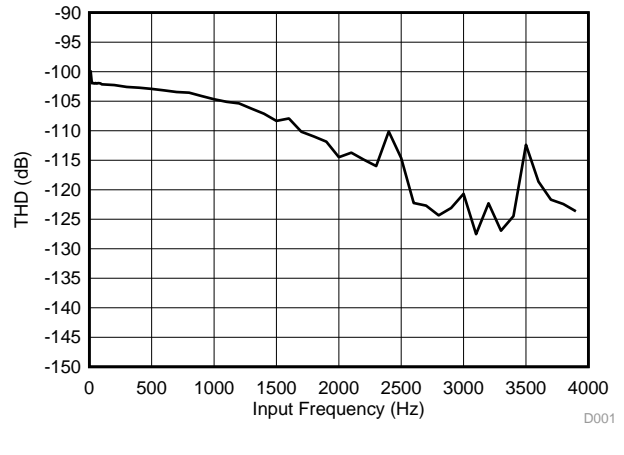


Figure 17. THD vs Input Frequency

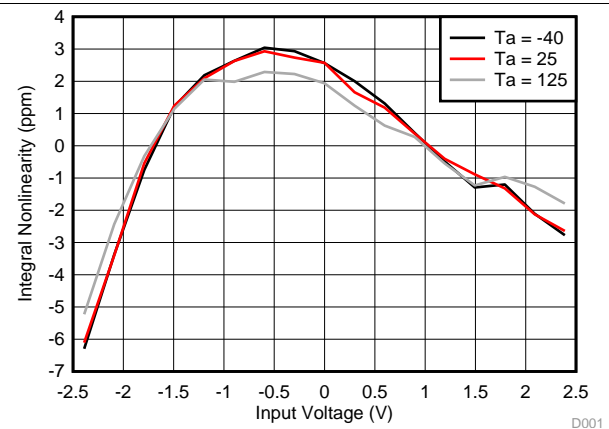


Figure 18. INL vs Temperature

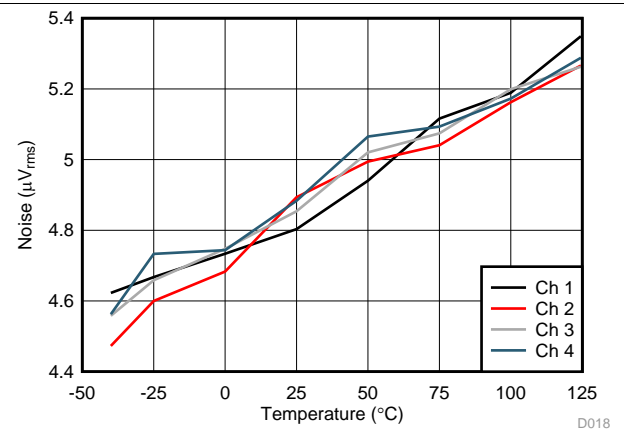
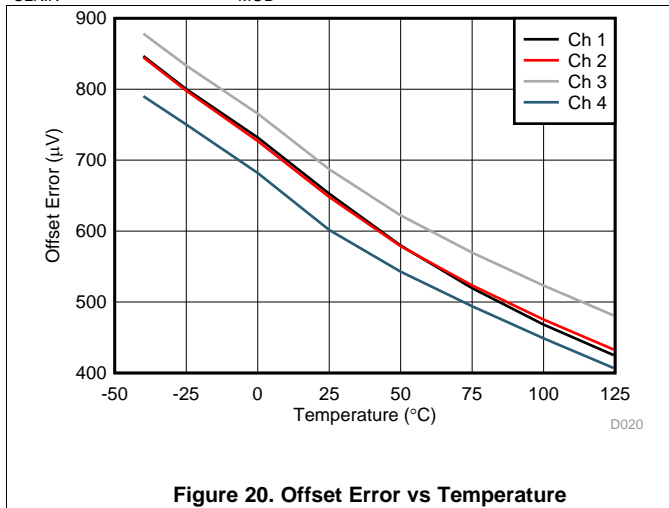


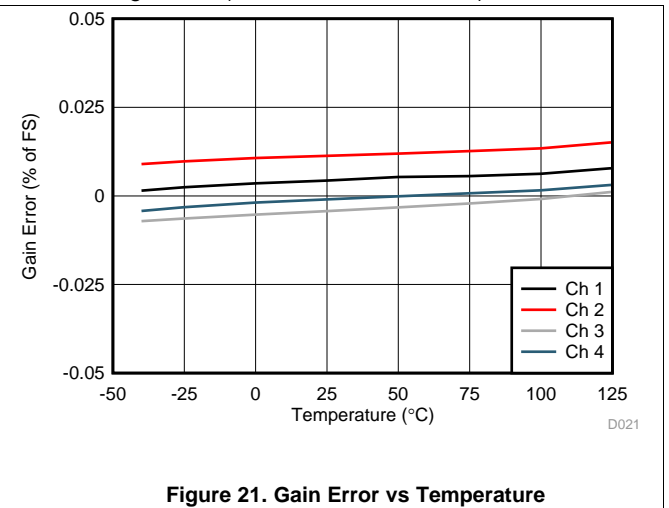
Figure 19. Noise RMS vs Temperature

**Typical Characteristics (continued)**

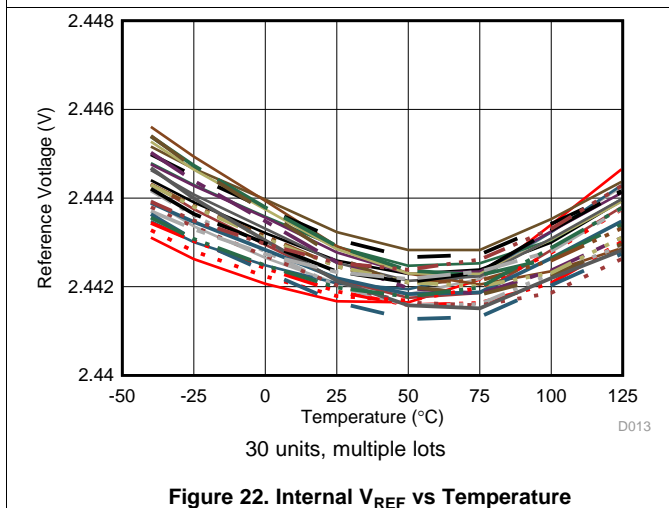
at  $T_A = 25^\circ\text{C}$ ,  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)



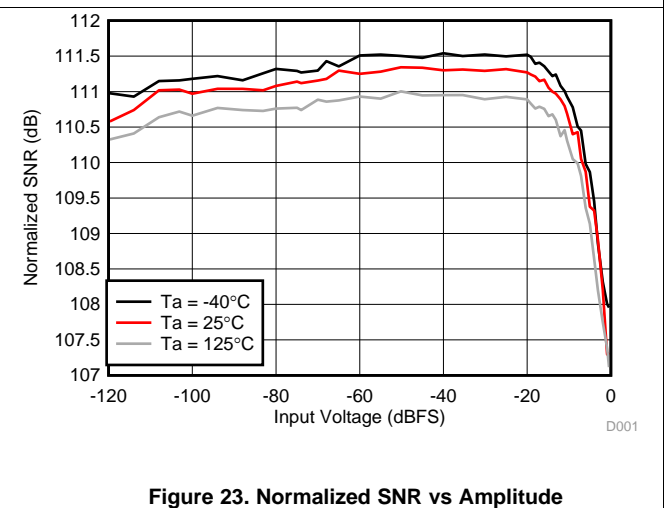
**Figure 20. Offset Error vs Temperature**



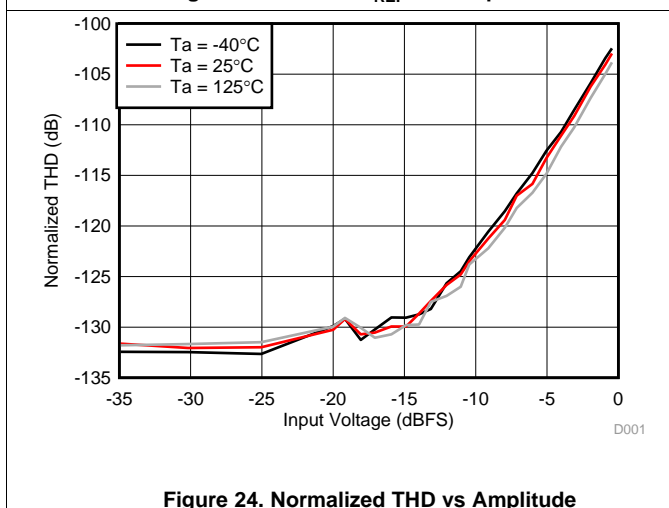
**Figure 21. Gain Error vs Temperature**



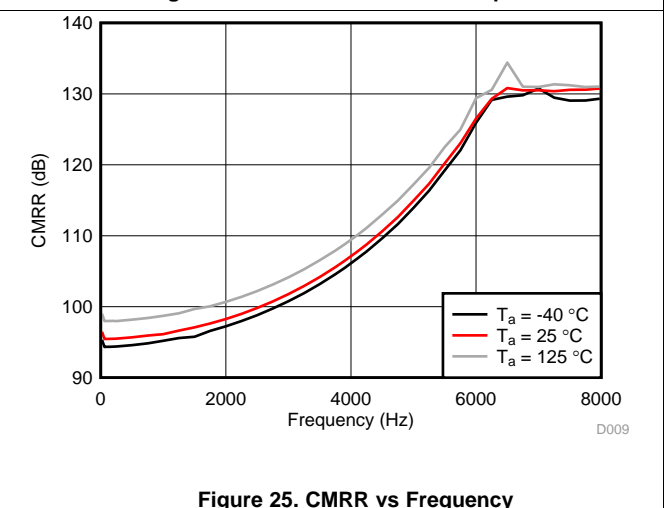
**Figure 22. Internal  $V_{\text{REF}}$  vs Temperature**



**Figure 23. Normalized SNR vs Amplitude**



**Figure 24. Normalized THD vs Amplitude**



**Figure 25. CMRR vs Frequency**

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)

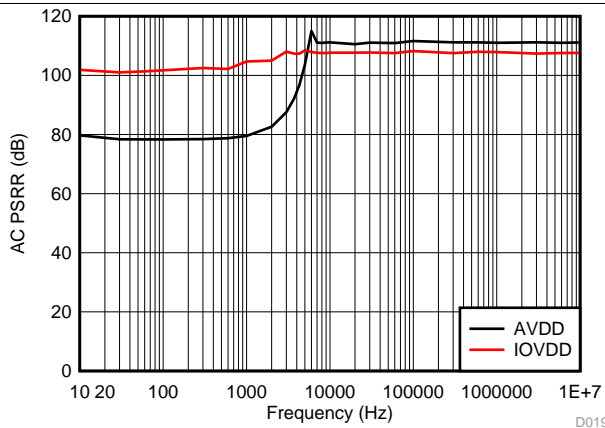


Figure 26. PSRR vs Frequency

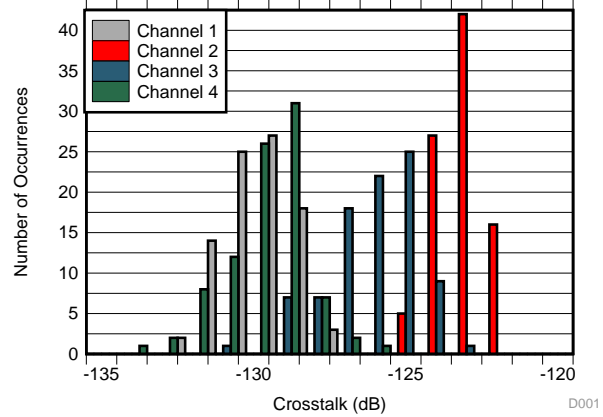


Figure 27. Crosstalk Histogram

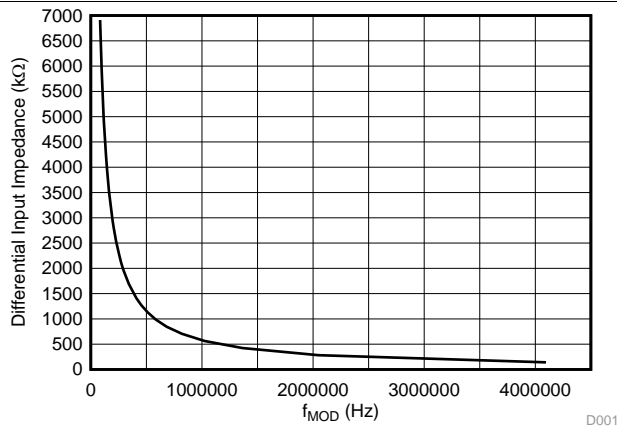


Figure 28. Differential Input Impedance vs Modulator Clock

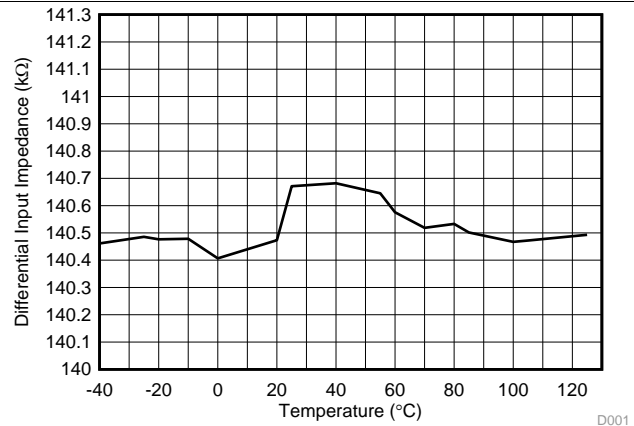


Figure 29. Differential Input Impedance vs Temperature at 4.096-MHz  $f_{\text{MOD}}$

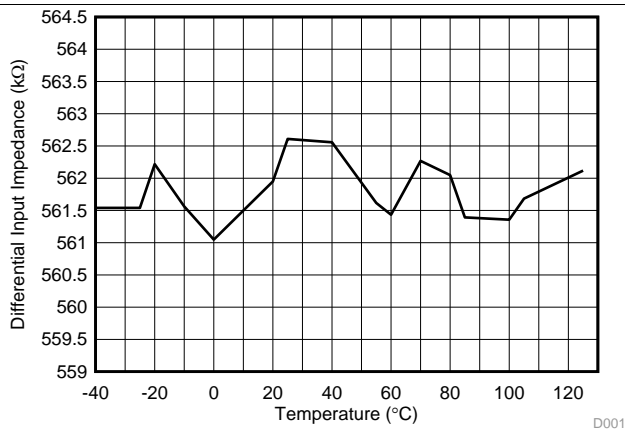
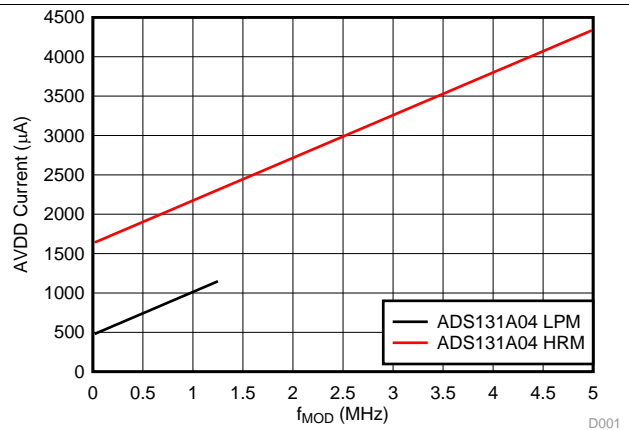


Figure 30. Differential Input Impedance vs Temperature at 1.024-MHz  $f_{\text{MOD}}$

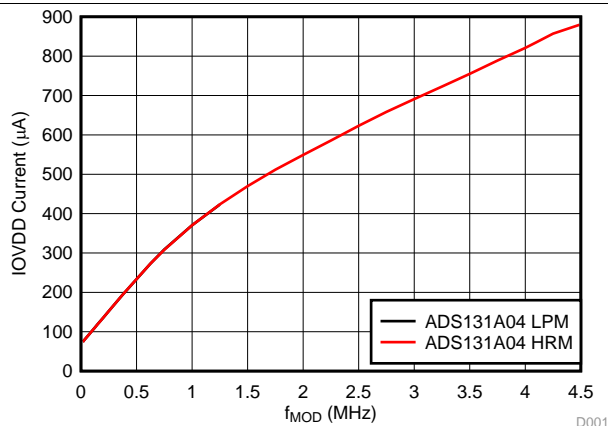


LPM = low-power mode, HRM = high-resolution mode

Figure 31. ADS131A04 AVDD Current vs  $f_{\text{MOD}}$

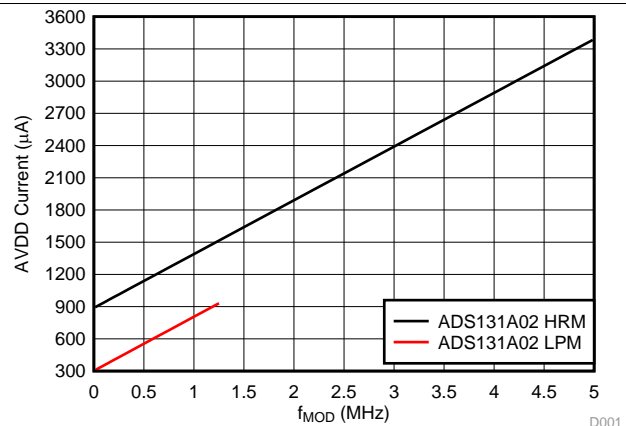
**Typical Characteristics (continued)**

at  $T_A = 25^\circ\text{C}$ ,  $\text{IOVDD} = 3.3\text{ V}$ ,  $\text{AVDD} = 2.5\text{ V}$ ,  $\text{AVSS} = -2.5\text{ V}$ ,  $\text{VNCPEN}$  (register 0Bh, bit 7) = 0, internal  $V_{\text{REF}} = 2.442\text{ V}$ ,  $f_{\text{CLKIN}} = 16.384\text{ MHz}$ ,  $f_{\text{MOD}} = 4.096\text{ MHz}$ , data rate = 8 kSPS, HR mode, and gain = 1 (unless otherwise noted)



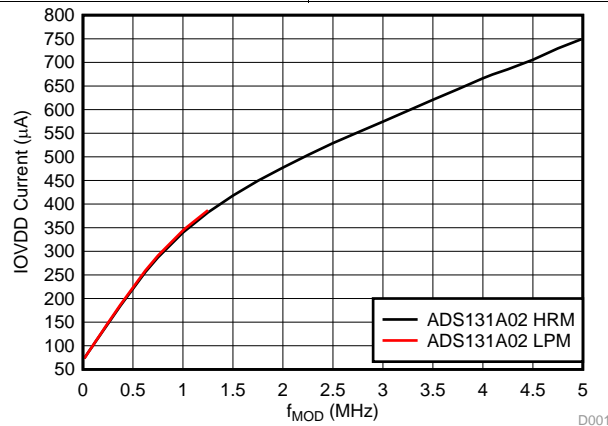
LPM = low-power mode, HRM = high-resolution mode

**Figure 32. ADS131A04 IOVDD Current vs  $f_{\text{MOD}}$**



LPM = low-power mode, HRM = high-resolution mode

**Figure 33. ADS131A02 AVDD Current vs  $f_{\text{MOD}}$**



LPM = low-power mode, HRM = high-resolution mode

**Figure 34. ADS131A02 IOVDD Current vs  $f_{\text{MOD}}$**

## 8 Parameter Measurement Information

### 8.1 Noise Measurements

Adjust the data rate and gain to optimize the ADS131A02 and ADS131A04 noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. [Table 1](#) and [Table 2](#) summarize the ADS131A0x noise performance with a 2.442-V reference and a 3.3-V analog power supply. [Table 3](#) and [Table 4](#) summarize the ADS131A02 and ADS131A04 noise performance with a 4.0-V reference and a 5-V analog power supply (or using  $\pm 2.5$ -V bipolar analog power supplies). The data are representative of typical noise performance at  $T_A = 25^\circ\text{C}$  when  $f_{\text{MOD}} = 4.096$  MHz. The data shown are typical results with the analog inputs shorted together and taking an average of multiple readings across all channels. A minimum 1 second of consecutive readings are used to calculate the RMS noise for each reading. The data are also representative of the ADS131A0x noise performance when using a low-noise external reference, such as the [REF5025](#) or [REF5040](#). The effective resolution data and dynamic range data in [Table 1](#), [Table 2](#), [Table 3](#), and [Table 4](#) are calculated using [Equation 1](#) and [Equation 2](#). The  $\mu\text{V}_{\text{RMS}}$  noise numbers in the tables are input-referred.

$$\text{Effective Resolution} = \log_2 \left( \frac{2 \times V_{\text{REF}}}{\text{Gain} \times V_{\text{RMS}}} \right) \quad (1)$$

$$\text{Dynamic Range} = 20 \times \log \left( \frac{V_{\text{REF}}}{\sqrt{2} \times \text{Gain} \times V_{\text{RMS}}} \right) \quad (2)$$

**Noise Measurements (continued)**
**Table 1. Dynamic Range, Effective Resolution, and Noise in  $\mu\text{V}_{\text{rms}}$  at 3.3-V Analog Supply, and 2.442-V Reference for Gain = 1, 2, and 4**

| OSR SETTING | $f_{\text{DATA AT 4.096-MHz}}$<br>$f_{\text{MOD}}$ (kHz) | GAIN               |                             |                            |                    |                             |                            |                    |                             |                            |
|-------------|--|--------------------|-----------------------------|----------------------------|--------------------|-----------------------------|----------------------------|--------------------|-----------------------------|----------------------------|
|             |  | x1                 |                             |                            | x2                 |                             |                            | x4                 |                             |                            |
|             |  | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu\text{V}_{\text{rms}}$ | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu\text{V}_{\text{rms}}$ | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu\text{V}_{\text{rms}}$ |
| 4096        | 1.000  | 119.49             | 21.35                       | 1.82                       | 113.49             | 20.35                       | 1.82                       | 108.08             | 19.46                       | 1.70                       |
| 2048        | 2.000  | 116.47             | 20.85                       | 2.58                       | 110.97             | 19.94                       | 2.44                       | 105.22             | 18.98                       | 2.36                       |
| 1024        | 4.000  | 113.85             | 20.41                       | 3.49                       | 107.91             | 19.43                       | 3.47                       | 101.77             | 18.41                       | 3.52                       |
| 800         | 5.120  | 112.93             | 20.26                       | 3.88                       | 106.72             | 19.23                       | 3.98                       | 101.05             | 18.29                       | 3.82                       |
| 768         | 5.333  | 112.90             | 20.25                       | 3.90                       | 106.69             | 19.22                       | 3.99                       | 100.76             | 18.24                       | 3.95                       |
| 512         | 8.000  | 110.73             | 19.89                       | 5.01                       | 104.83             | 18.91                       | 4.95                       | 98.75              | 17.91                       | 4.97                       |
| 400         | 10.240   | 109.74             | 19.73                       | 5.61                       | 103.69             | 18.72                       | 5.64                       | 97.76              | 17.74                       | 5.58                       |
| 384         | 10.667   | 109.53             | 19.70                       | 5.75                       | 103.65             | 18.72                       | 5.66                       | 97.58              | 17.71                       | 5.69                       |
| 256         | 16.000   | 107.74             | 19.40                       | 7.07                       | 101.67             | 18.39                       | 7.11                       | 95.72              | 17.40                       | 7.06                       |
| 200         | 20.480   | 106.48             | 19.19                       | 8.17                       | 100.55             | 18.20                       | 8.09                       | 94.54              | 17.21                       | 8.08                       |
| 192         | 21.333   | 106.28             | 19.16                       | 8.36                       | 100.17             | 18.14                       | 8.45                       | 94.11              | 17.13                       | 8.49                       |
| 128         | 32.000   | 104.05             | 18.78                       | 10.81                      | 97.98              | 17.78                       | 10.88                      | 92.00              | 16.78                       | 10.82                      |
| 96          | 42.667   | 101.90             | 18.43                       | 13.85                      | 95.95              | 17.44                       | 13.74                      | 89.90              | 16.43                       | 13.79                      |
| 64          | 64.000   | 97.63              | 17.72                       | 22.64                      | 91.61              | 16.72                       | 22.64                      | 85.52              | 15.71                       | 22.83                      |
| 48          | 85.333   | 92.58              | 16.88                       | 40.50                      | 86.62              | 15.89                       | 40.22                      | 80.59              | 14.89                       | 40.26                      |
| 32          | 128.000  | 85.12              | 15.62                       | 96.82                      | 78.96              | 14.62                       | 97.12                      | 73.02              | 13.61                       | 97.51                      |

**Table 2. Dynamic Range, Effective Resolution, and Noise in  $\mu\text{V}_{\text{rms}}$  at 3.3-V Analog Supply, and 2.442-V Reference for Gain = 8 and 16**

| OSR SETTING | $f_{\text{DATA AT 4.096-MHz}}$<br>$f_{\text{MOD}}$ (kHz) | GAIN               |                             |                            |                    |                             |                            |
|-------------|--|--------------------|-----------------------------|----------------------------|--------------------|-----------------------------|----------------------------|
|             |  | x8                 |                             |                            | x16                |                             |                            |
|             |  | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu\text{V}_{\text{rms}}$ | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu\text{V}_{\text{rms}}$ |
| 4096        | 1.000  | 101.72             | 18.40                       | 1.77                       | 95.45              | 17.36                       | 1.82                       |
| 2048        | 2.000  | 98.88              | 17.93                       | 2.45                       | 93.07              | 16.96                       | 2.39                       |
| 1024        | 4.000  | 95.97              | 17.44                       | 3.43                       | 89.82              | 16.42                       | 3.48                       |
| 800         | 5.120  | 95.03              | 17.29                       | 3.82                       | 88.66              | 16.23                       | 3.98                       |
| 768         | 5.333  | 94.63              | 17.22                       | 4.00                       | 88.41              | 16.19                       | 4.09                       |
| 512         | 8.000  | 92.75              | 16.91                       | 4.96                       | 87.00              | 15.95                       | 4.81                       |
| 400         | 10.240   | 91.84              | 16.76                       | 5.51                       | 85.62              | 15.72                       | 5.64                       |
| 384         | 10.667   | 91.52              | 16.70                       | 5.72                       | 85.50              | 15.70                       | 5.72                       |
| 256         | 16.000   | 89.57              | 16.38                       | 7.16                       | 83.58              | 15.38                       | 7.14                       |
| 200         | 20.480   | 88.44              | 16.19                       | 8.16                       | 82.45              | 15.20                       | 8.12                       |
| 192         | 21.333   | 88.26              | 16.16                       | 8.32                       | 82.12              | 15.14                       | 8.44                       |
| 128         | 32.000   | 86.02              | 15.79                       | 10.77                      | 79.80              | 14.76                       | 11.02                      |
| 96          | 42.667   | 83.91              | 15.44                       | 13.74                      | 77.72              | 14.41                       | 14.00                      |
| 64          | 64.000   | 79.52              | 14.71                       | 22.78                      | 73.45              | 13.70                       | 22.92                      |
| 48          | 85.333   | 74.60              | 13.89                       | 40.14                      | 68.47              | 12.87                       | 40.66                      |
| 32          | 128.000  | 66.93              | 12.62                       | 97.05                      | 60.97              | 11.61                       | 97.61                      |

**Table 3. Dynamic Range, Effective Resolution, and Noise in  $\mu V_{rms}$  at  $\pm 2.5$ -V Analog Supply, and 4.0-V Reference for Gain = 1, 2, and 4**

| OSR SETTING | $f_{DATA}$ AT 4.096-MHz<br>$f_{MOD}$ (kHz) | GAIN               |                             |               |                    |                             |               |                    |                             |               |
|-------------|--|--------------------|-----------------------------|---------------|--------------------|-----------------------------|---------------|--------------------|-----------------------------|---------------|
|             |  | x1                 |                             |               | x2                 |                             |               | x4                 |                             |               |
|             |  | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu V_{rms}$ | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu V_{rms}$ | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu V_{rms}$ |
| 4096        | 1.000                                      | 124.55             | 22.19                       | 1.66          | 118.69             | 21.22                       | 1.64          | 112.32             | 20.16                       | 1.71          |
| 2048        | 2.000                                      | 121.47             | 21.68                       | 2.38          | 114.98             | 20.60                       | 2.51          | 109.58             | 19.70                       | 2.34          |
| 1024        | 4.000                                      | 118.44             | 21.18                       | 3.37          | 112.48             | 20.18                       | 3.36          | 106.31             | 19.16                       | 3.41          |
| 800         | 5.120                                      | 117.58             | 21.03                       | 3.72          | 111.46             | 20.02                       | 3.77          | 105.29             | 18.99                       | 3.84          |
| 768         | 5.333                                      | 116.75             | 20.89                       | 4.10          | 110.88             | 19.92                       | 4.03          | 105.06             | 18.95                       | 3.94          |
| 512         | 8.000                                      | 115.16             | 20.63                       | 4.93          | 109.23             | 19.65                       | 4.88          | 103.10             | 18.63                       | 4.94          |
| 400         | 10.240                                     | 114.15             | 20.46                       | 5.53          | 108.33             | 19.50                       | 5.41          | 102.28             | 18.49                       | 5.43          |
| 384         | 10.667                                     | 113.88             | 20.42                       | 5.71          | 107.83             | 19.41                       | 5.73          | 101.70             | 18.39                       | 5.80          |
| 256         | 16.000                                     | 112.09             | 20.12                       | 7.02          | 105.76             | 19.07                       | 7.27          | 99.83              | 18.08                       | 7.19          |
| 200         | 20.480                                     | 110.71             | 19.89                       | 8.22          | 104.65             | 18.88                       | 8.27          | 98.37              | 17.84                       | 8.51          |
| 192         | 21.333                                     | 110.13             | 19.79                       | 8.79          | 104.10             | 18.79                       | 8.80          | 97.99              | 17.78                       | 8.90          |
| 128         | 32.000                                     | 106.93             | 19.26                       | 12.72         | 100.76             | 18.24                       | 12.94         | 94.59              | 17.21                       | 13.15         |
| 96          | 42.667                                     | 104.17             | 18.80                       | 17.47         | 98.18              | 17.81                       | 17.41         | 92.00              | 16.78                       | 17.74         |
| 64          | 64.000                                     | 98.84              | 17.92                       | 32.27         | 92.74              | 16.91                       | 32.58         | 86.50              | 15.87                       | 33.40         |
| 48          | 85.333                                     | 93.30              | 17.00                       | 61.06         | 87.45              | 16.03                       | 59.91         | 81.31              | 15.01                       | 60.74         |
| 32          | 128.000                                    | 85.10              | 15.64                       | 156.92        | 78.87              | 14.60                       | 160.84        | 73.35              | 13.67                       | 153.69        |

**Table 4. Dynamic Range, Effective Resolution, and Noise in  $\mu V_{rms}$  at  $\pm 2.5$ -V Analog Supply, and 4.0-V Reference for Gain = 8 and 16**

| OSR SETTING | $f_{DATA}$ AT 4.096-MHz<br>$f_{MOD}$ (kHz) | GAIN               |                             |               |                    |                             |               |
|-------------|--|--------------------|-----------------------------|---------------|--------------------|-----------------------------|---------------|
|             |  | x8                 |                             |               | x16                |                             |               |
|             |  | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu V_{rms}$ | DYNAMIC RANGE (dB) | EFFECTIVE RESOLUTION (Bits) | $\mu V_{rms}$ |
| 4096        | 1.000                                      | 106.35             | 19.17                       | 1.70          | 100.66             | 18.22                       | 1.63          |
| 2048        | 2.000                                      | 103.40             | 18.68                       | 2.38          | 97.37              | 17.68                       | 2.39          |
| 1024        | 4.000                                      | 100.46             | 18.19                       | 3.35          | 94.59              | 17.21                       | 3.29          |
| 800         | 5.120                                      | 99.53              | 18.04                       | 3.72          | 93.28              | 17.00                       | 3.83          |
| 768         | 5.333                                      | 99.19              | 17.98                       | 3.87          | 93.09              | 16.97                       | 3.91          |
| 512         | 8.000                                      | 97.31              | 17.67                       | 4.81          | 91.08              | 16.63                       | 4.93          |
| 400         | 10.240                                     | 96.23              | 17.49                       | 5.45          | 90.16              | 16.48                       | 5.48          |
| 384         | 10.667                                     | 95.84              | 17.42                       | 5.70          | 89.85              | 16.43                       | 5.68          |
| 256         | 16.000                                     | 93.87              | 17.09                       | 7.15          | 87.73              | 16.07                       | 7.25          |
| 200         | 20.480                                     | 92.70              | 16.90                       | 8.18          | 86.43              | 15.86                       | 8.41          |
| 192         | 21.333                                     | 92.10              | 16.80                       | 8.77          | 85.68              | 15.73                       | 9.17          |
| 128         | 32.000                                     | 88.58              | 16.22                       | 13.14         | 82.42              | 15.19                       | 13.36         |
| 96          | 42.667                                     | 86.27              | 15.83                       | 17.15         | 80.00              | 14.79                       | 17.64         |
| 64          | 64.000                                     | 80.60              | 14.89                       | 32.92         | 74.48              | 13.87                       | 33.31         |
| 48          | 85.333                                     | 75.29              | 14.01                       | 60.68         | 69.10              | 12.98                       | 61.90         |
| 32          | 128.000                                    | 67.06              | 12.64                       | 156.51        | 61.17              | 11.64                       | 156.32        |



## 9 Detailed Description

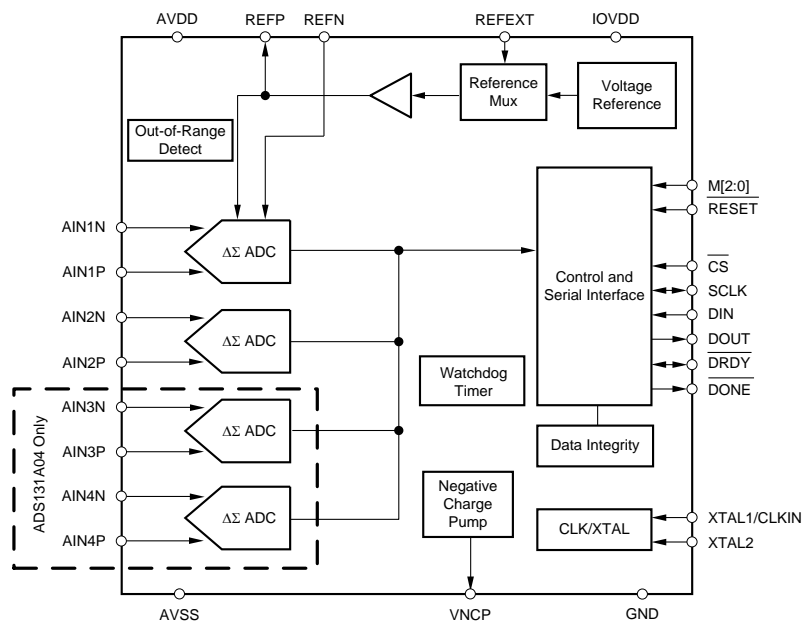
### 9.1 Overview

The ADS131A02 and ADS131A04 are low-power, two- and four-channel, simultaneous-sampling, 24-bit, delta-sigma ( $\Delta\Sigma$ ), analog-to-digital converters (ADCs) with an integrated low-drift internal reference voltage. Data rate flexibility, wide dynamic range, and interface options make these devices good choices when designing for smart-grid and other industrial power monitor, control, and protection applications. The ADC interface data integrity features provide for a very low rate of transmission errors. Throughout this document, the ADS131A02 and ADS131A04 are referred to as the ADS131A0x.

The ADS131A0x has very flexible power-supply options. A 5-V single-supply (or  $\pm 2.5$ -V bipolar-supply) operation is available to support up to a 4.5-V external reference to maximize the dynamic range of the converter. Alternatively, a negative charge pump can be enabled to accept absolute input signals down to  $-1.5$  V below ground when powered from a single 3.3-V supply. Five gain options are available to help maximize the ADC code range and 16 selectable oversampling ratio (OSR) options are selectable to optimize the converter for a specific data rate. The low-drift internal reference can be programmed to either 2.442 V or 4 V. Input signal out-of-range detection can be accomplished by using the integrated comparators, with programmable trigger-point settings. A detailed diagram of the ADS131A0x is shown in the [Functional Block Diagram](#) section.

The device offers multiple serial peripheral interface (SPI) communication options to provide flexibility for interfacing to microprocessors or field-programmable gate arrays (FPGAs). Synchronous real-time and asynchronous interrupt communication modes are available using the SPI-compatible interface. Multiple devices can share a common SPI port and are synchronized by using the  $\overline{\text{DRDY}}$  signal. Device communication is specified through configuration of the M0 interface mode pin and chaining of the  $\overline{\text{DONE}}$  signal. Optional cyclic redundancy check (CRC) and hamming code correction on the interface enhance communication integrity.

### 9.2 Functional Block Diagram



## 9.3 Feature Description

This section contains details of the ADS131A0x internal feature elements. The ADC clocking is discussed first, followed by the analog blocks and the digital filter.

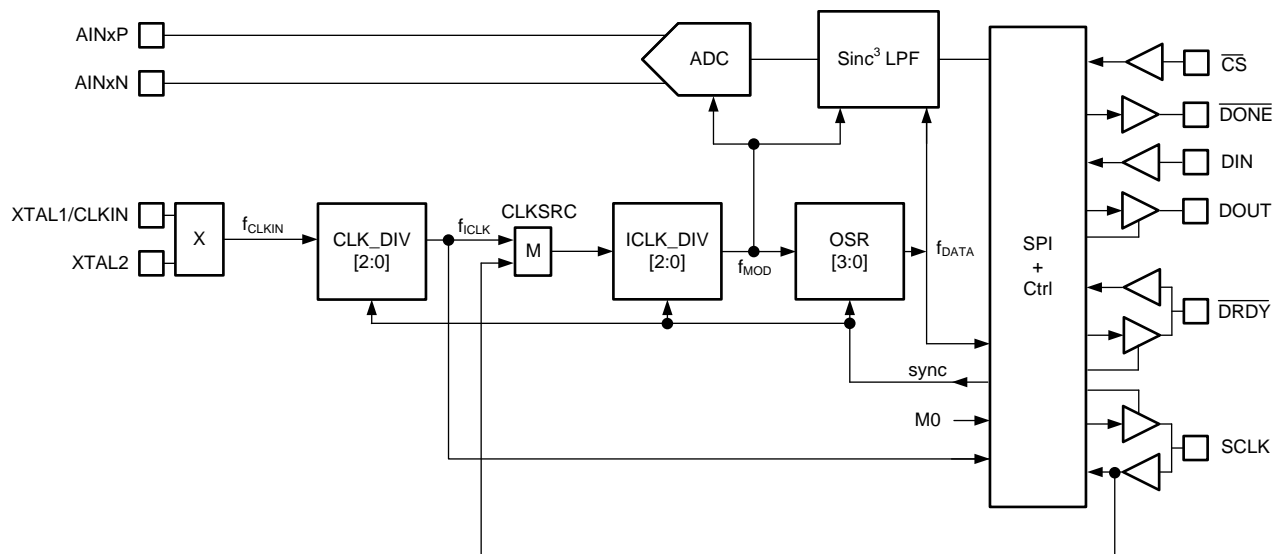
### 9.3.1 Clock

Multiple clocks are created from one external master clock source in the ADS131A0x to create device configuration flexibility. The ADC operates from the internal system clock, ICLK, which is provided in one of three ways.

- An external master clock, CLKIN, can be applied directly to the XTAL1/CLKIN pin to be divided down to generate ICLK using the CLK\_DIV[2:0] bits in the [CLK1 register](#). In this case, leave the XTAL2 pin floating.
- A crystal oscillator can be applied between XTAL1/CLKIN and XTAL2, generating a master clock to be divided down using the CLK\_DIV[2:0] bits in the CLK1 register to generate ICLK.
- A free-running SCLK can be internally routed to be set as ICLK. This mode is only available in synchronous slave interface mode. Tie the CLKIN/XTAL1 pin to GND. Leave the XTAL2 pin unconnected.

The system ICLK is passed through a second 3-bit clock divider (ICLK\_DIV[2:0] in the [CLK2 register](#)) to create the modulator clock, MODCLK. MODCLK is used for timing of the delta-sigma ( $\Delta\Sigma$ ) modulator sampling and digital filter.

The interface operation mode determines the options for sourcing ICLK. When in asynchronous interrupt or synchronous master mode, generate ICLK by applying a direct external master clock signal to the XTAL1/CLKIN pin or by using a crystal oscillator across the XTAL1/CLKIN and XTAL2 pins. If directly applying a master clock to the XTAL1/CLKIN pin, leave XTAL2 floating. In synchronous slave mode, a free-running SCLK line can be connected directly into the ICLK\_DIV block in place of the divided XTAL or CLKIN source. Use the CLKSRC bit in the CLK1 register to select between the XTAL1/CLKIN or SCLK input as the master clock source for the ADC. The CLKSRC bit must be set prior to powering up the ADC channels. Using SCLK as ICLK is useful in galvanic isolated applications to limit the digital I/O lines crossing the isolation barrier. [Figure 35](#) shows the clock dividers and clocking names.



**Figure 35. ADC Clock Generation**

## Feature Description (continued)

### 9.3.1.1 XTAL1/CLKIN and XTAL2

XTAL1/CLKIN is the external clock input to the ADC and can be supplied from a clock source or by using a crystal (along with the XTAL2 pin). Figure 36 shows the configuration for the two clock input options.

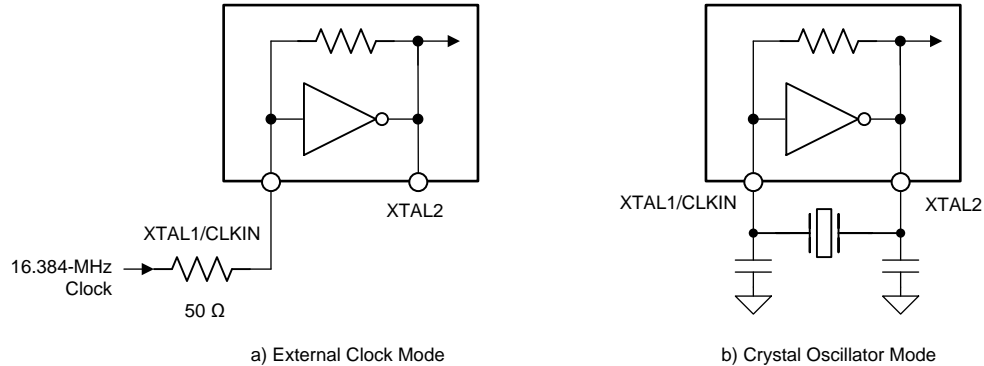


Figure 36. Clock Mode Configurations

Input the clock directly to the XTAL1/CLKIN pin and leave the XTAL2 pin floating when using a direct clock source.

Connect the crystal and load capacitors as shown in Figure 36b to the XTAL1/CLKIN and XTAL2 pins. Place the crystal and crystal load capacitors close to the ADC pins using short, direct traces. Connect the load capacitors to the digital ground. Do not connect any other external circuit to the crystal oscillator. Table 5 lists recommended crystals for use with the ADS131A0x. The crystal oscillator start-up time is typically 5 ms, but can be longer depending on the crystal characteristics.

Table 5. Recommended Crystals

| MANUFACTURER | FREQUENCY  | OPERATING TEMPERATURE RANGE | PART NUMBER           |
|--------------|------------|-----------------------------|-----------------------|
| Abracon      | 16.384 MHz | –40°C to +125°C             | ABLS-16.384MHZ-L4Q-T  |
| Abracon      | 16.384 MHz | –40°C to +85°C              | ABM3C-16.384MHZ-D4Y-T |
| ECS          | 16.384 MHz | –40°C to +85°C              | ECS-163-18-5PXEN-TR   |

### 9.3.1.2 ICLK

ICLK is the internal system clock to the ADC. ICLK is derived from CLKIN set through the CLK\_DIV[2:0] bits in the CLK1 register or is set as SCLK when operating in synchronous slave mode. ICLK is used as the SCLK output when operating in synchronous master mode in addition to being used for the internal ADC clock timing. Use the CLKSRC bit to set the source for ICLK.

### 9.3.1.3 MODCLK

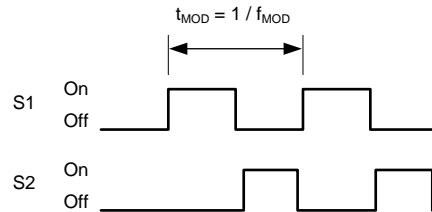
MODCLK is the modulator clock used for the ADC sampling. MODCLK is derived from ICLK set through the ICLK\_DIV[2:0] bits in the CLK2 register. Verify that the  $f_{MOD}$  minimum and maximum limits are met in the Electrical Characteristics table by adjusting the CLK\_DIV[2:0] and ICLK\_DIV[2:0] clock dividers.

### 9.3.1.4 Data Rate

The data rate is the rate at which conversion results are generated by the ADC. In a delta-sigma ADC, the oversampling ratio (OSR) is the ratio between the modulator frequency and the output data rate. The OSR[3:0] bits in the CLK2 register set the OSR on the ADS131A0x. The output data rate is the frequency of MODCLK ( $f_{MOD}$ ) divided by the OSR.

### 9.3.2 Analog Input

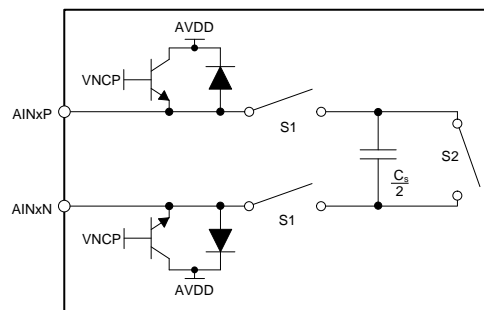
The ADS131A0x analog inputs are directly connected to the switched-capacitor sampling network of the  $\Delta\Sigma$  modulator without a multiplexer or integrated buffer. The device inputs are measured differentially ( $V_{IN} = V_{AINxP} - V_{AINxN}$ ) and can span from  $-V_{REF} / \text{Gain}$  to  $V_{REF} / \text{Gain}$ . [Figure 38](#) shows a conceptual diagram of the modulator circuit charging and discharging the sampling capacitor through switches, although the actual implementation is slightly different. The timing for switches S1 and S2, as shown in [Figure 37](#), are 180 degrees out-of-phase of one another.



**Figure 37. S1 and S2 Switch Timing**

Electrostatic discharge (ESD) circuitry protects the inputs. [Figure 38](#) shows a simplified representation of the ESD circuit. Protection for input voltages exceeding AVDD can be modeled as a simple diode.

The negative charge pump voltage, VNCP, controls the voltage at which the low-side protection devices begin conducting. Tie VNCP to AVSS if the charge pump is not used to ensure the clamping voltage is properly set. The charge pump cannot provide a large amount of current. The mechanism shown in [Figure 38](#) ensures current provided by the charge pump is limited in the case of an overvoltage event.



**Figure 38. Equivalent Analog Input Circuitry**

To prevent the ESD diodes from being enabled, the absolute voltage on any input must stay within the range provided by [Equation 3](#) when the internal charge pump is disabled and within the range in [Equation 4](#) when the internal charge pump is enabled:

$$AVSS - 0.3 \text{ V} < V_{AINxP} \text{ or } V_{AINxN} < AVDD + 0.3 \text{ V} \quad (3)$$

$$AVSS - 1.65 \text{ V} < V_{AINxP} \text{ or } V_{AINxN} < AVDD + 0.3 \text{ V} \quad (4)$$

If the voltages on the input pins have any potential to violate these conditions, external clamp diodes or series resistors may be required to limit the input currents to safe values (see the [Absolute Maximum Ratings](#) table).

The charging of the input capacitors draws a transient current from the sensor driving the ADS131A0x inputs. The average value of this current can be used to calculate an effective impedance of  $Z_{IN}$ , where  $Z_{IN} = V_{IN} / I_{AVERAGE}$ . This effective input impedance is a function of the modulator sampling frequency and [Equation 5](#) can be used to calculate an estimate value. When using  $f_{MOD} = 4.096 \text{ MHz}$ , the input impedance is approximately 130 k $\Omega$ .

$$Z_{in} = \frac{2}{f_{MOD} \times C_S}$$

where

- $f_{MOD}$  = modulator clock and
- $C_S = 3.5 \text{ pF}$

(5)

There are two general methods of driving the ADS131A0x analog inputs, as shown in Figure 39: pseudo-differential or fully-differential.

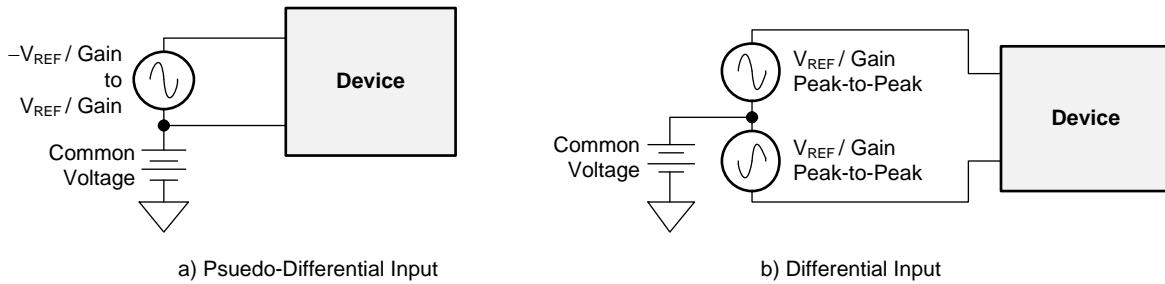
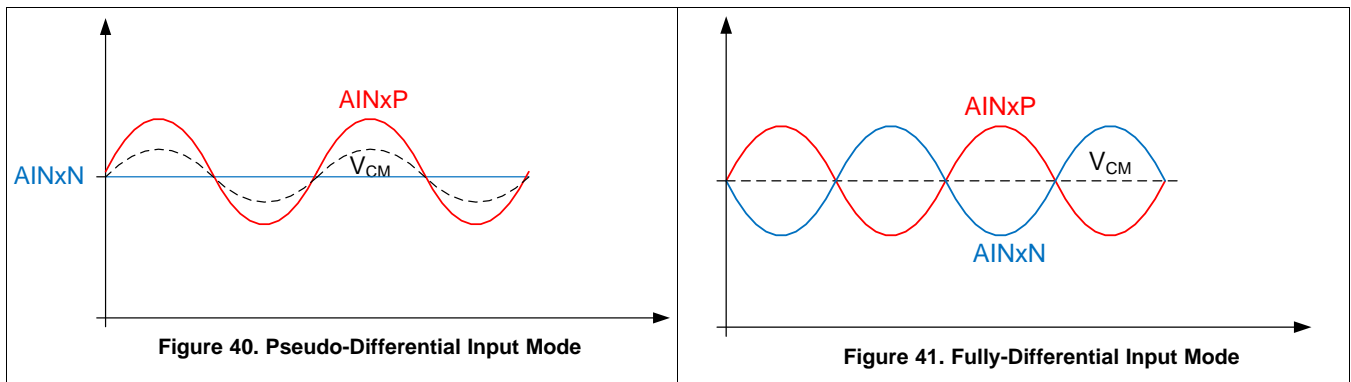


Figure 39. Pseudo-Differential and Fully-Differential Inputs

To apply a pseudo-differential signal to the fully-differential inputs, apply a dc voltage to AINxN, preferably to the analog mid-supply  $[(AVDD + AVSS) / 2]$  or  $[(AVDD + VNCP) / 2]$  when the negative charge pump is enabled. The AINxP pins can swing between  $-V_{REF} / \text{Gain}$  to  $V_{REF} / \text{Gain}$  (as shown in Figure 40) around the common voltage. The common-mode voltage,  $V_{CM}$ , changes with  $V_{AINxP}$ .

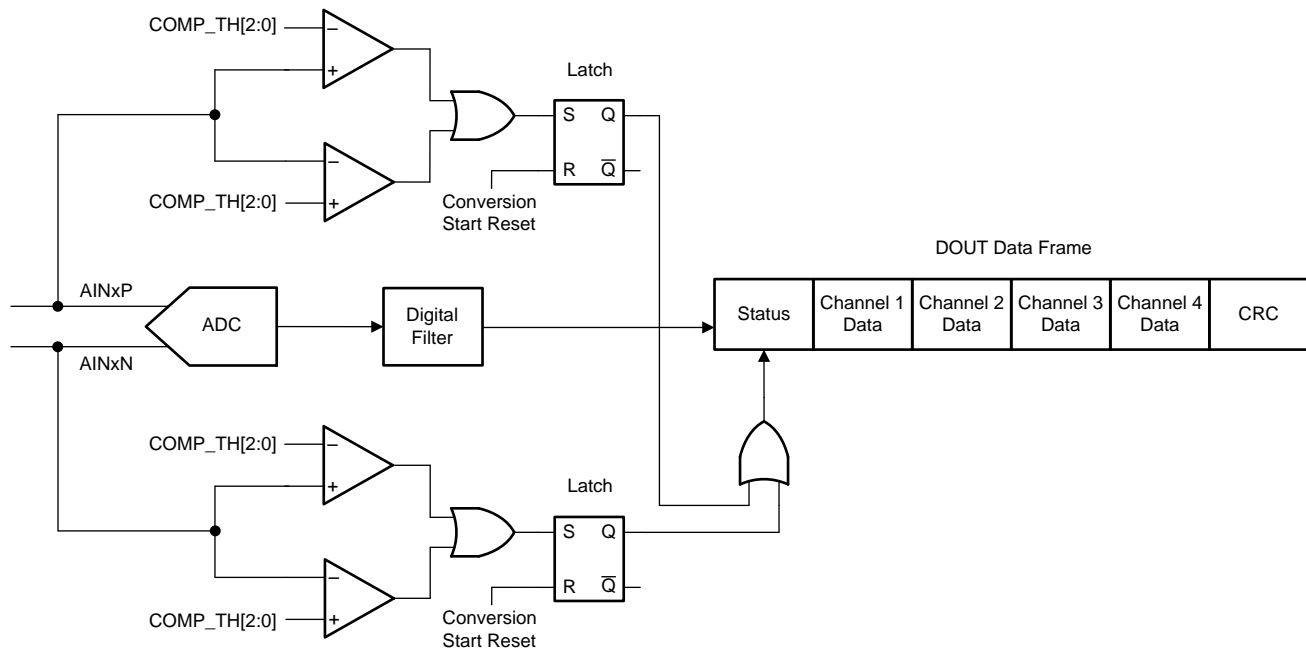
Configure the signals at AINxP and AINxN to be 180° out-of-phase centered around a common-mode voltage to use a fully-differential input method. Both the AINxP and AINxN inputs swing from  $V_{CM} + \frac{1}{2} V_{REF} / \text{Gain}$  to  $V_{CM} - \frac{1}{2} V_{REF} / \text{Gain}$ , as shown in Figure 41. The differential voltage at the maximum and minimum points is equal to  $V_{REF} / \text{Gain}$  to  $-V_{REF} / \text{Gain}$ , respectively. The  $V_{CM}$  voltage remains fixed when AINxP and AINxN swing. Use the ADS131A0x in a differential configuration to maximize the dynamic range of the data converter. For optimal performance, the  $V_{CM}$  is recommended to be set at the midpoint of the analog supplies.

Tie any unused analog input channels directly to AVSS.



### 9.3.3 Input Overrange and Underrange Detection

Each ADS131A0x channel has two integrated comparators to detect overrange and underrange conditions on the input signals. Use the COMP\_TH[2:0] bits in the [A\\_SYS\\_CFG register](#) to set a high and low threshold level using a 3-bit digital-to-analog converter (DAC). This threshold voltage is compared to the voltage on the input pins. The voltage monitor triggers an alarm by setting the F\_ADCIN bit of the [STAT\\_1 register](#) when the individual voltage on AINxP or AINxN exceeds the threshold set by the COMP\_TH[2:0] bits. When the F\_ADCIN bit of the STAT\_1 register is set, indicating an out-of-range event, read the [STAT\\_P register](#) or [STAT\\_N register](#) to determine exactly which input pin exceeded the set threshold. [Figure 42](#) shows an input overrange and underrange detection block diagram.



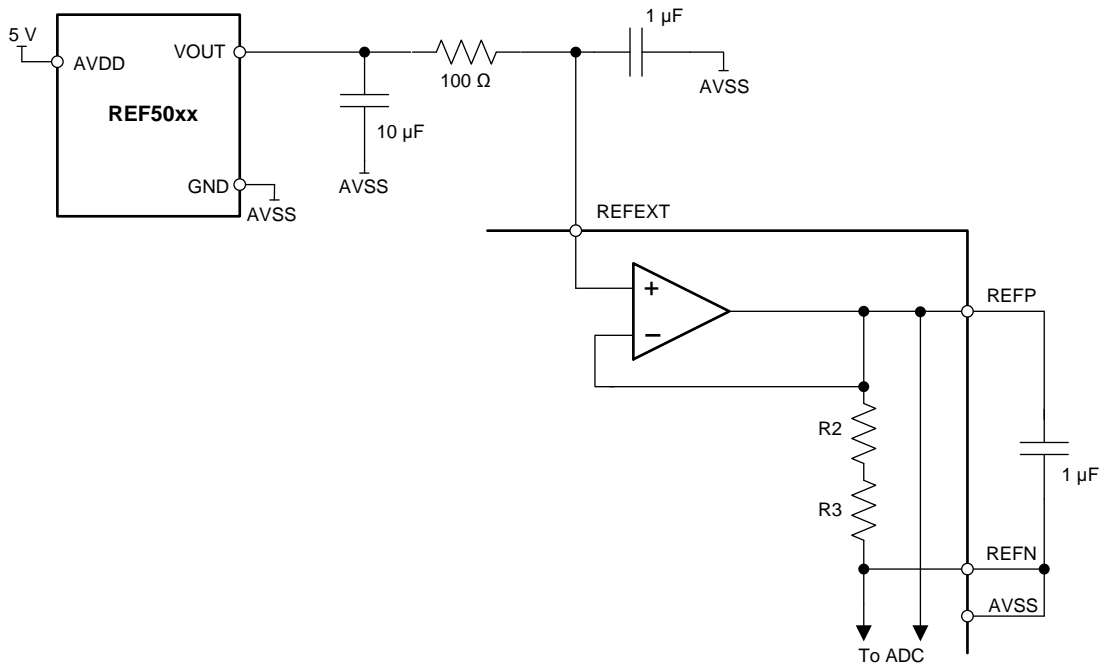
**Figure 42. ADC Out-of-Range Detection Monitor**

### 9.3.4 Reference

The ADS131A0x offers an integrated low-drift, 2.442-V or 4.0-V reference option. For applications that require a different reference voltage, the device offers a reference input option for use with an external reference voltage.

The reference source is selected by the INT\_REFEN bit in the [A\\_SYS\\_CFG register](#). By default, the external reference is selected (INT\_REFEN = 0). The internal voltage reference requires 0.2 ms to settle to 1% and 250 ms to fully settle to 0.01% when switching from an external reference source to the internal reference (using the recommended bypass capacitor values). The external reference input is internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference. Connect the reference voltage to the REFEXT pin when using an external reference.

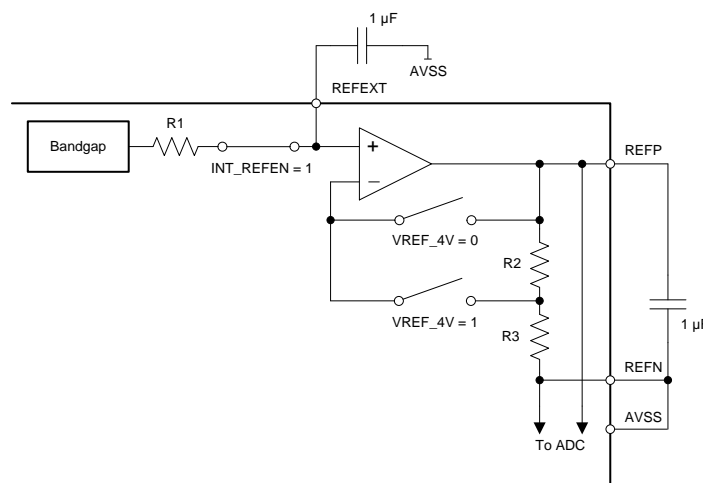
External band-limiting capacitors determine the amount of reference noise contribution. For high-end systems, choose capacitor values such that the bandwidth is limited to less than 10 Hz so that the reference noise does not dominate the system noise. In systems with strict ADC power-on requirements, using a large capacitor on the reference increases the time for the voltage to meet the desired value, thus increasing system power-on time. [Figure 43](#) illustrates a typical external reference drive circuitry with recommended filtering options.



NOTE: R2 = 62.3 kΩ, R3 = 97.5 kΩ.

**Figure 43. External Reference Driver**

Set the INTREF\_EN bit to 1 in the [A\\_SYS\\_CFG](#) register to use the internal reference. When the internal reference is selected, use the VREF\_4V bit to select between a 2.442-V or 4.0-V reference. By default, the device is set to use the 2.442-V reference. The VREF\_4V bit has no function when set to use the external reference. When enabling the negative charge pump with a 3.0-V to 3.45-V analog supply, the internal reference must be set to 2.442 V. [Figure 44](#) shows a simplified block diagram of the internal ADS131A0x reference. The reference voltage is generated with respect to AVSS requiring a direct connection between REFNP and AVSS.



NOTE: R1 = 20 kΩ, R2 = 62.3 kΩ, R3 = 97.5 kΩ.

**Figure 44. Internal Reference**

### 9.3.5 $\Delta\Sigma$ Modulator

The ADS131A0x is a multichannel, simultaneous sampling  $\Delta\Sigma$  ADC where each channel has an individual modulator and digital filter. The modulator samples the input signal at the rate of  $f_{\text{MOD}}$  derived as a function of the ADC operating clock,  $f_{\text{CLK}}$ . As in the case of any  $\Delta\Sigma$  modulator, the ADS131A0x noise is shaped until  $f_{\text{MOD}} / 2$ . The modulator converts the analog input voltage into a pulse-code modulated (PCM) data stream. The on-chip digital decimation filters take this bitstream and provide attenuation to the now shaped, higher frequency noise. This  $\Delta\Sigma$  sample and conversion process drastically reduces the complexity of the analog antialiasing filters typically required with nyquist ADCs.

### 9.3.6 Digital Decimation Filter

The digital filter receives the modulator output and decimates the data stream to create the final conversion result. The digital filter on each channel consists of a third-order sinc filter. The oversampling ratio (OSR) determines the number of samples taken to create the output data word, and is set by the modulator rate divided by the data rate ( $f_{\text{MOD}} / f_{\text{DATA}}$ ). The OSR of the sinc filters is adjusted by the OSR[3:0] bits in the [CLK2 register](#). The OSR setting is a global setting that affects all channels and, therefore, all channels operate at the same data rate in the device. By adjusting the OSR, tradeoffs can be made between noise and data rate to optimize the signal chain: filter more for lower noise (thus creating lower data rates), filter less for higher data rates.

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of  $f_{\text{MOD}}$ . [Equation 6](#) shows the scaled sinc<sup>3</sup> filter Z-domain transfer function. As shown in [Table 6](#), the integer  $N$  is the set OSR and the integer  $K$  is a scaling factor for OSR values that are not an integer power of 2.

$$|H(z)| = K \times \left| \frac{(1 - Z^{-N})}{N \times (1 - Z^{-1})} \right|^3 \quad (6)$$

[Equation 7](#) shows the sinc filter frequency domain transfer function. As shown in [Table 6](#), the integer  $N$  is the set OSR and the integer  $K$  is a scaling factor for OSR values that are not an integer power of 2.

$$|H(f)| = K \times \left| \frac{\sin \left[ \frac{N\pi f}{f_{\text{MOD}}} \right]}{N \times \sin \left[ \frac{\pi f}{f_{\text{MOD}}} \right]} \right|^3$$

where:

(7)

N = oversampling ratio

**Table 6. K Scaling Factor**

| OSR (N)                                 | K SCALING VALUE |
|---|-----------------|
| 800, 400, 200                           | 0.9983778       |
| 4096, 2048, 1024, 512, 256, 128, 64, 32 | 1.0             |
| 768, 384, 192, 96, 48                   | 1.00195313      |

The sinc<sup>3</sup> filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. [Figure 45](#) and [Figure 46](#) illustrate the digital filter frequency response out to a normalized input frequency ( $f_{\text{IN}} / f_{\text{DATA}}$ ) of 5 and 0.5, respectively. [Figure 47](#), [Figure 48](#), and [Figure 49](#) illustrate the frequency response for OSR = 32, OSR = 512, and OSR = 4096 up to  $f_{\text{MOD}}$ , respectively.



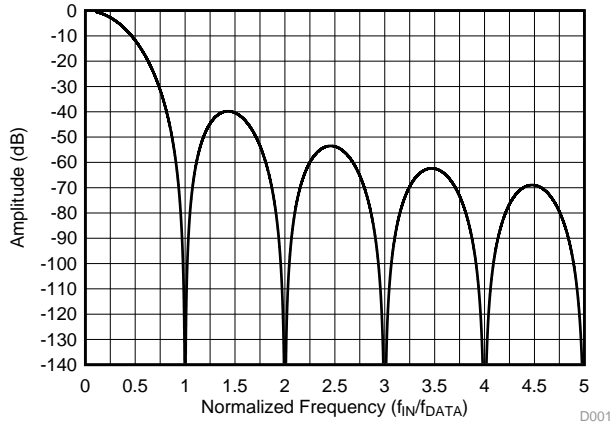


Figure 45. Sinc<sup>3</sup> Filter Frequency Response

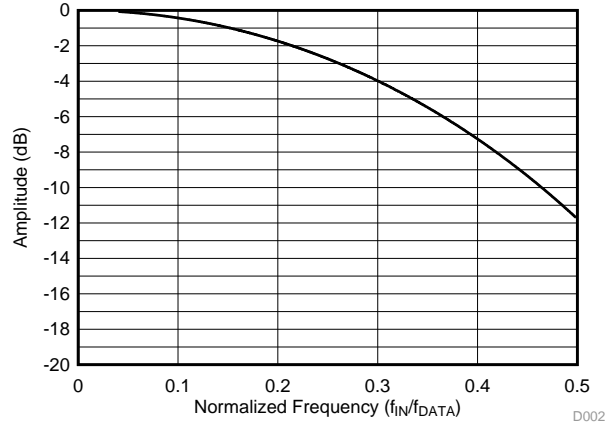


Figure 46. Sinc<sup>3</sup> Filter Roll-Off

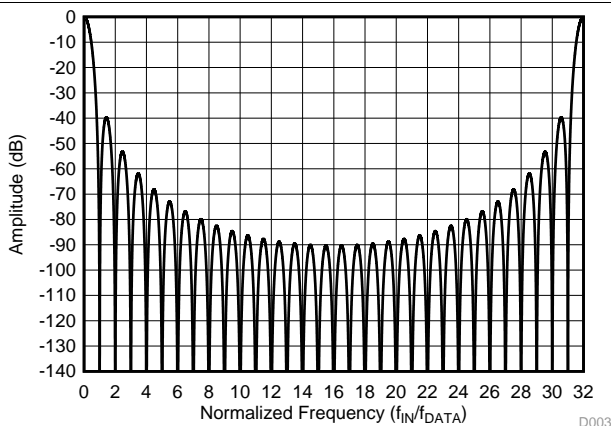


Figure 47. Sinc<sup>3</sup> Filter Frequency Response (OSR 32)

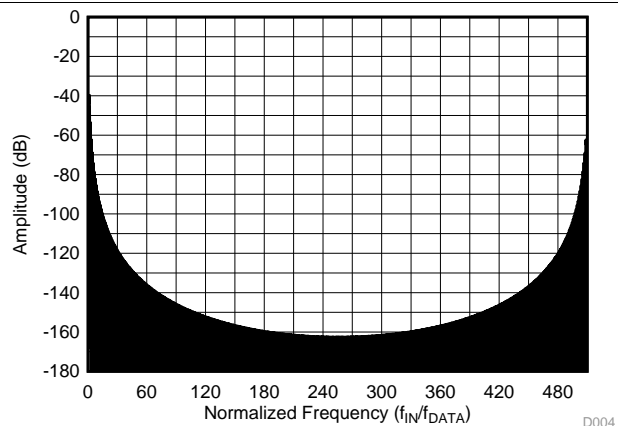


Figure 48. Sinc<sup>3</sup> Filter Frequency Response (OSR 512)

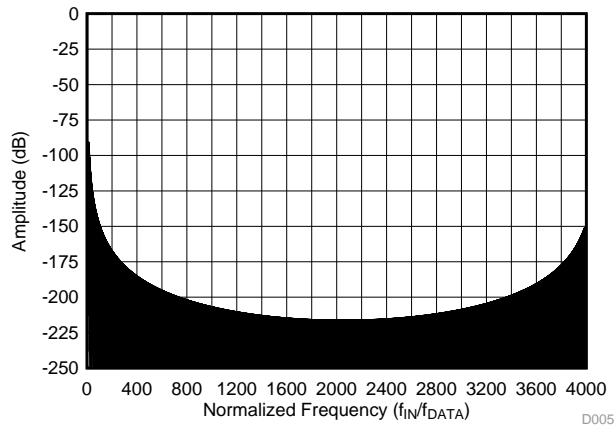
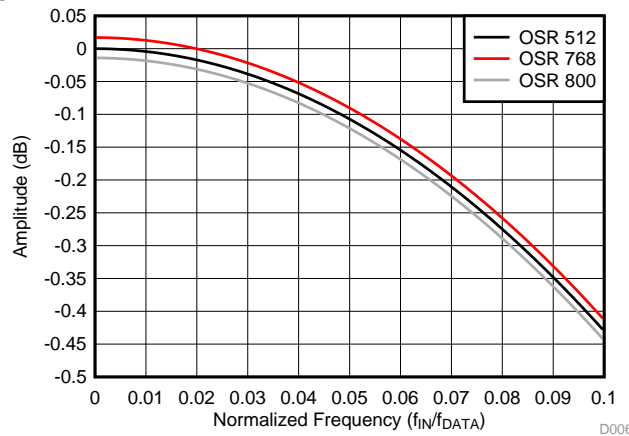


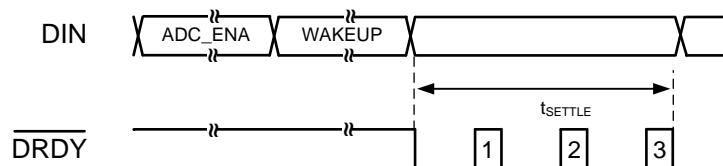
Figure 49. Sinc<sup>3</sup> Filter Frequency Response (OSR 4096)

The K scaling factor for OSR values that are not an integer power of two adds a non-integer gain factor to the  $\text{sinc}^3$  frequency response across all frequencies. The host must account for the K scaling factor to obtain the ADC gain error given in the [Electrical Characteristics](#) table. [Figure 50](#) overlays the digital filter frequency response for the three K scaling options in [Table 6](#). Graph scaling is set to a narrow limit to show the small gain variation between OSR values.



**Figure 50. Non-Binary OSR  $\text{Sinc}^3$  Filter Frequency Response**

The ADS131A0x immediately begins outputting conversion data when powered up and brought out of standby mode using the WAKEUP command. The  $\text{sinc}^3$  digital filter requires three conversion cycles to provide a settled conversion result, assuming the analog input has settled to its final value ( $t_{\text{SETTLE}}$ ). The output data are not gated when the digital filter settles, meaning that the first two conversion results show unsettled data from the filter path before settled data are available on the third conversion cycle. The first two unsettled conversion cycles, though unsettled, can be used for diagnostic purposes to ensure the ADC is coming out of standby as expected. [Figure 51](#) shows the new data ready behavior and time needed for the digital filter coming out of standby.



**Figure 51.  $\text{Sinc}^3$  Filter Settling**

The digital filter uses a multiple stage linear-phase digital filter. Linear-phase filters exhibit constant delay time across all input frequencies (also known as *constant group delay*). This behavior results in zero-phase error when measuring multi-tone signals. For more information about group delay in delta-sigma ADCs, see the [Accounting for delay from multiple sources in delta-sigma ADCs](#) white paper.

### 9.3.7 Watchdog Timer

The ADS131A0x offers an integrated watchdog timer to protect the device from entering any unresponsive state. The watchdog timer is a 16-bit counter running on an internal 50-kHz clock. The timer resets with each data frame when the  $\overline{\text{CS}}$  signal transitions from high to low. If a timer reset does not take place and the watchdog timer expires after 500 ms, the device assumes that an unresponsive state has occurred and issues a watchdog timer reset. Following the reset, the device enters the power-up state (see the [Power-Up](#) section), sets the F\_WDT bit in the STAT\_1 register, and indicates that a watchdog timer reset has taken place. Enable the watchdog timer by setting the WDT\_EN bit in the [D\\_SYS\\_CFG](#) register.

## 9.4 Device Functional Modes

### 9.4.1 Low-Power and High-Resolution Mode

The ADS131A0x offers two modes of operation: high-resolution and low-power mode. High-resolution mode enables a faster modulator clock, up to  $f_{\text{MOD}} = 4.25$  MHz, to maximize performance at higher data rates. Low-power mode scales the analog and digital currents and restricts the maximum  $f_{\text{MOD}}$  to 1.05 MHz. Select the operating mode using the HRM bit in the [A\\_SYS\\_CFG](#) register.

## Device Functional Modes (continued)

### 9.4.2 Power-Up

After all supplies are established and the  $\overline{\text{RESET}}$  pin goes high, an internal power-on-reset (POR) is performed. As part of the POR process, all registers are initialized to the default states, the state of the Mx pins are latched, the interface is placed in a locked state, and the device enters standby mode. POR can take up to 4.5 ms to complete. When the host communicates with the ADS131A0x, the SPI interface outputs a READY status word indicating that the power-on cycle is completed and the device is ready to accept commands. The [STAT\\_S register](#) indicates if the ADC powered up properly or if any fault occurred during the initialization of the device. Send an UNLOCK command to enable the interface and begin communicating with the device. See [Table 14](#) for more information on the READY status word and the [UNLOCK from POR or RESET](#) or [RESET: Reset to POR Values](#) sections for more information on bringing the device out of POR.

### 9.4.3 Standby and Wake-Up Mode

After being unlocked from POR or after reset, the device enters a low-power standby mode with all ADC channels powered down. After the registers are properly configured, enable all the ADC channels together by writing to the [ADC\\_ENA register](#) and issue a WAKEUP command to start conversions. To enter standby mode again, send the STANDBY command and disable all ADC channels by writing to the ADC\_ENA register. The ADS131A0x requires using the WAKEUP and STANDBY commands together with writing to the ADC\_ENA register to disable or enable ADC channels to start and stop conversions.

### 9.4.4 Conversion Mode

The device runs in continuous conversion mode. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion. Data are available at the next data-ready indicator, although data may not be fully settled through the digital filter (see the [Digital Decimation Filter](#) section for more information on settled data).

### 9.4.5 Reset (RESET)

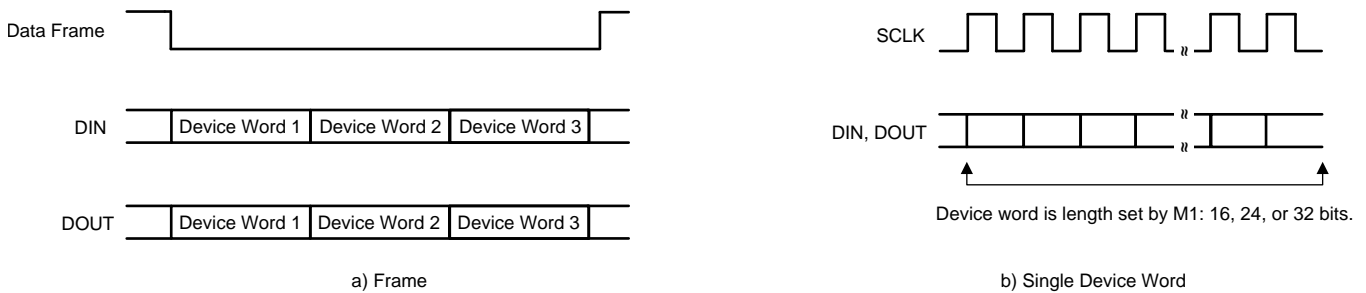
There are two methods to reset the ADS131A0x: pull the  $\overline{\text{RESET}}$  pin low for at least  $t_{w(\text{RSL})}$  or send the RESET command. The  $\overline{\text{RESET}}$  pin must be tied high if the RESET command is used. The RESET command takes effect at the completion of the command. As part of the reset process, all registers are initialized to the default states, the status of M0, M1, and M2 pins are latched, the interface is placed in a locked state, and the device enters standby mode. Reset can take up to 4.5 ms to complete. The device outputs a READY status word indicating that the reset is completed and the device is ready to accept commands. Send an UNLOCK command to enable the interface and begin communicating with the device. See [Table 13](#) for more information on the READY status word, the UNLOCK from POR command, and the RESET command. [Figure 7](#) illustrates the critical timing relationship of taking the ADS131A0x into reset and bringing the device out of reset.

There are two methods to reset the ADS131A0x: pull the  $\overline{\text{RESET}}$  pin low, or send the RESET command. When using the  $\overline{\text{RESET}}$  pin, driving the pin low forces the device into reset. Follow the minimum pulse duration timing specifications before taking the  $\overline{\text{RESET}}$  pin back high. The RESET command takes effect at the completion of the command (see the [RESET: Reset to POR Values](#) section for more information). After the device is reset, 4.5 ms are required to complete initialization of the configuration registers to the default states and for the device to be ready for normal operation.. [Figure 7](#) illustrates the critical timing relationship of taking the ADS131A0x into reset and bringing the device out of reset. Tie the  $\overline{\text{RESET}}$  pin high if the RESET command is used to reset the device.

## 9.5 Programming

### 9.5.1 Interface Protocol

The ADS131A0x is designed with an interface protocol that expands the capability of outputting more ADC system monitors without disrupting data flow. This protocol communicates through standard serial peripheral interface (SPI) methods, using allocated device words within a single data transmission frame to pass information. A single data frame starts when the interface is enabled, typically done by pulling the  $\overline{CS}$  line low. The duration of a data frame is made up of several device words with programmable bit lengths. A visual representation showing how a data frame is made up of multiple device words is shown in [Figure 52](#).



**Figure 52. Data Frame and Device Word**

#### 9.5.1.1 Device Word Length

The interface is full duplex, allowing the device to be read to and written from within the same data frame. The length of the individual device words is programmable through the state of the M1 pin. This pin must be set to one of three states at power-up. The pin state is latched at power-up and changing the pin state after power-up has no effect. [Table 7](#) lists the modes associated with the M1 pin state. The M1 pin must be tied high to IOVDD through a  $< 1\text{-k}\Omega$  resistor, low to GND through a  $< 1\text{-k}\Omega$  resistor, or left floating.

**Table 7. M1 Pin Setting**

| M1 STATE | DEVICE WORD LENGTH (Bits) |
|----------|---------------------------|
| IOVDD    | 32                        |
| GND      | 24                        |
| Float    | 16                        |

#### 9.5.1.2 Fixed versus Dynamic-Frame Mode

The device has two data frame size options to set the number of device words per frame: fixed and dynamic-frame mode, controlled by the FIXED bit in the [D\\_SYS\\_CFG register](#). By default, the ADS131A0x powers up in dynamic-frame mode.

In fixed-frame mode, there are always six device words for each data frame for the ADS131A0x. The first device word is reserved for the status word, the next four device words are reserved for the conversion data for each of the four channels, and the last word is reserved for the cyclic redundancy check (CRC) data word.

In dynamic-frame mode, the number of device words per data frame is dependent on if the ADCs are enabled and if CRC data integrity is enabled. When the ADCs are powered down in standby mode, the number of device words per data frame is either one or two depending if CRC data integrity is enabled. In normal operation with the ADC channels powered up, the number of device words per data frame depends on if CRC is enabled. When CRC data integrity is disabled in dynamic-frame mode, the sixth device word for the ADS131A0x is removed from the data frame. If CRC data integrity remains enabled, the device word count remains at six.

Figure 53 shows the fixed-frame and dynamic-frame modes for the ADS131A04 in standby mode with CRC data integrity enabled and disabled. Figure 54 shows the fixed-frame and dynamic-frame modes for the ADS131A04 with ADC channels and CRC data integrity enabled and disabled.

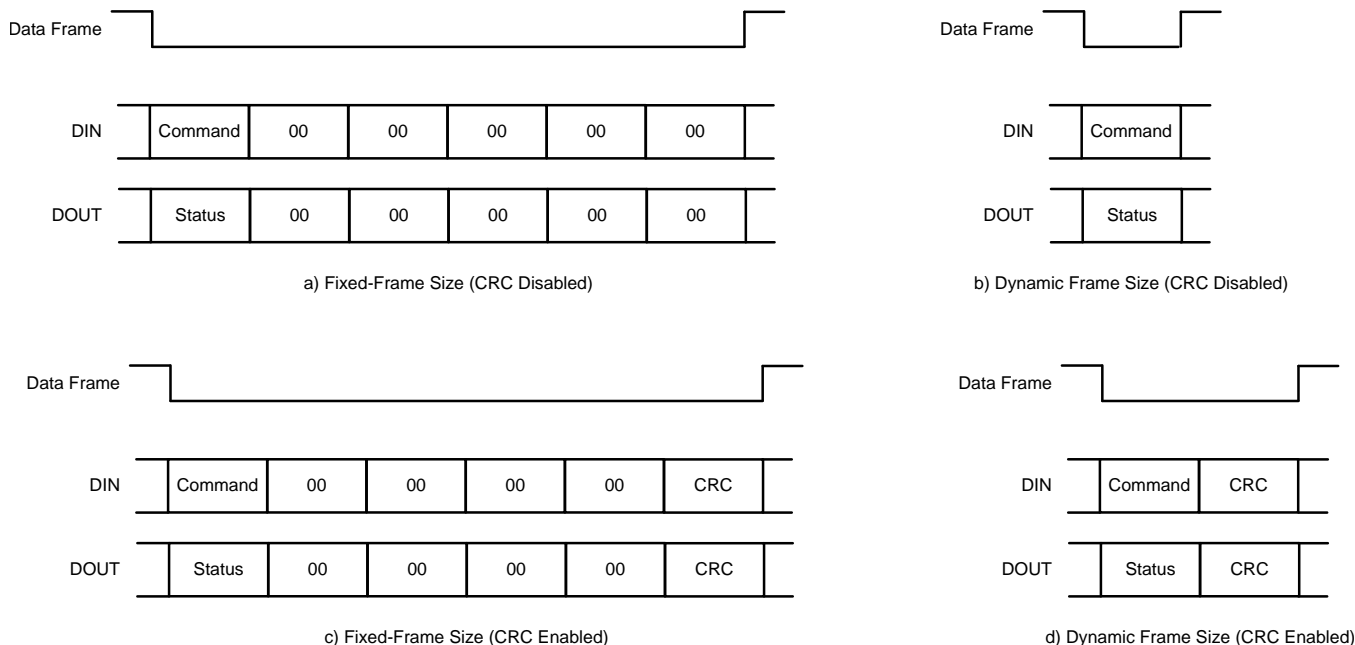
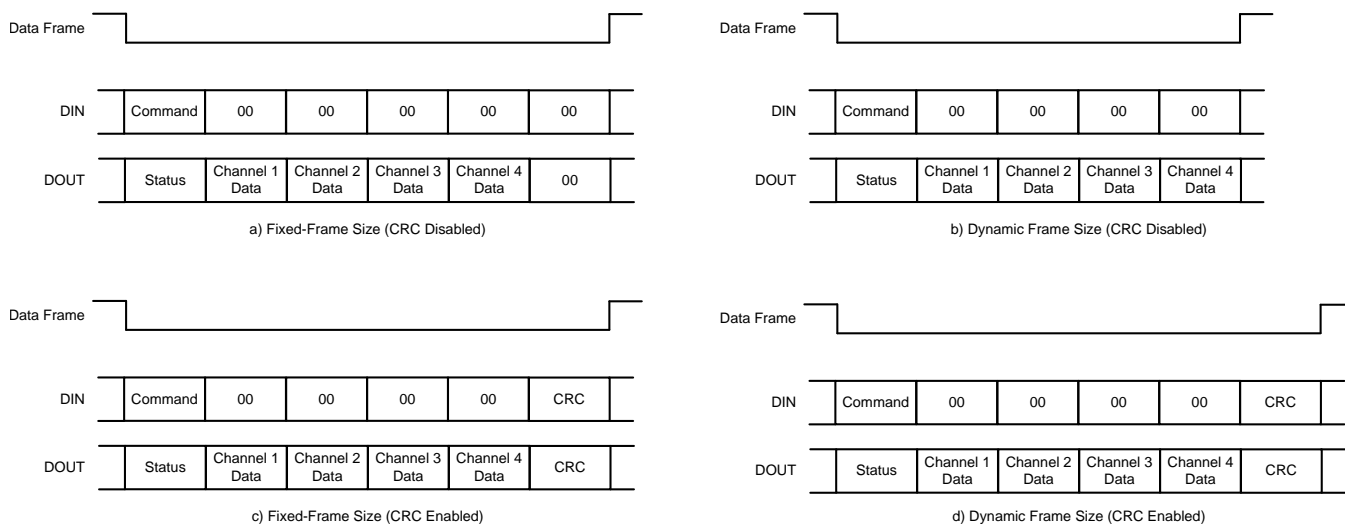


Figure 53. Fixed versus Dynamic-Frame Modes in Standby Mode



NOTE: CMND = Command.

Figure 54. Fixed versus Dynamic-Frame Modes With ADCs Enabled

### 9.5.1.3 Command Word

The command word is the first device word on every DIN data frame. This frame is reserved for sending user commands to write or read from registers (see the *SPI Command Definitions* section). The commands are stand-alone, 16-bit words that appear in the 16 most significant bits (MSBs) of the first device word of the DIN data frame. Write zeroes to the remaining unused least significant bits (LSBs) when operating in either 24-bit or 32-bit word size modes.

### 9.5.1.4 Status Word

The status word is the first device word in every DOUT data frame. The status word either provides a status update of the ADC internal system monitors or functions as a status response to an input command; see the [SPI Command Definitions](#) section. The contents of the status word are always 16 bits in length with the remaining LSBs set to zeroes depending on the device word length; see [Table 7](#).

### 9.5.1.5 Data Words

The data words follow the status word. The device shifts individual channel data in separate data words. The ADS131A0x converter is 24-bit resolution regardless of the device word length; see [Table 7](#). The output data are truncated to 16 bits when using the 16-bit device word length setting (or when enabling hamming code with a 24-bit device word length setting). The output data are extended to 32 bits with eight zeroes (00000000) added to the least significant bits when using the 32-bit device word length setting (when hamming code is disabled).

Use the device word length (see [Table 7](#)) to set the output resolution of the ADS131A0x. When placing the hardware M1 pin in a floating state, the interface operates in 16-bit device word length mode by removing the eight least significant bits. The 16 bits of data per channel are sent in binary twos complement format, MSB first. The size of one code (LSB) is calculated using [Equation 8](#):

$$1 \text{ LSB} = (2 \times V_{\text{REF}} / \text{Gain}) / 2^{16} = \text{FS} / 2^{15} \quad (8)$$

A positive full-scale input [ $V_{\text{IN}} \geq (\text{FS} - 1 \text{ LSB}) = (V_{\text{REF}} / \text{Gain} - 1 \text{ LSB})$ ] produces an output code of 7FFFh and a negative full-scale input ( $V_{\text{IN}} \leq -\text{FS} = -V_{\text{REF}} / \text{Gain}$ ) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

[Table 8](#) summarizes the ideal output codes for different input signals.

**Table 8. 16-Bit Ideal Output Code versus Input Signal**

| INPUT SIGNAL, $V_{\text{IN}}$<br>$V_{\text{AINxP}} - V_{\text{AINxN}}$ | IDEAL OUTPUT CODE <sup>(1)</sup> |
|--|----------------------------------|
| $\geq \text{FS} (2^{15} - 1) / 2^{15}$                                 | 7FFFh                            |
| $\text{FS} / 2^{15}$   | 0001h                            |
| 0  | 0000h                            |
| $-\text{FS} / 2^{15}$  | FFFFh                            |
| $\leq -\text{FS}$  | 8000h                            |

(1) Excludes the effects of noise, INL, offset, and gain errors.

Pull the M1 pin to IOVDD (through a < 1-kΩ resistor) or GND (through a < 1-kΩ resistor) to set the device either to a 24-bit or 32-bit device word length. In either setting, the ADS131A0x outputs 24 bits of data per channel in binary twos complement format, MSB first. The size of one code (LSB) is calculated using [Equation 9](#):

$$1 \text{ LSB} = (2 \times V_{\text{REF}} / \text{Gain}) / 2^{24} = \text{FS} / 2^{23} \quad (9)$$

A positive full-scale input [ $V_{\text{IN}} \geq (\text{FS} - 1 \text{ LSB}) = (V_{\text{REF}} / \text{Gain} - 1 \text{ LSB})$ ] produces an output code of 7FFFFFFh and a negative full-scale input ( $V_{\text{IN}} \leq -\text{FS} = -V_{\text{REF}} / \text{Gain}$ ) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

[Table 9](#) summarizes the ideal output codes for different input signals.

**Table 9. 24-Bit Ideal Output Code versus Input Signal**

| INPUT SIGNAL, $V_{\text{IN}}$<br>$V_{\text{AINxP}} - V_{\text{AINxN}}$ | IDEAL OUTPUT CODE <sup>(1)</sup> |
|--|----------------------------------|
| $\geq \text{FS} (2^{23} - 1) / 2^{23}$                                 | 7FFFFFFh                         |
| $\text{FS} / 2^{23}$   | 000001h                          |
| 0  | 000000h                          |
| $-\text{FS} / 2^{23}$  | FFFFFFh                          |
| $\leq -\text{FS}$  | 800000h                          |

(1) Excludes the effects of noise, INL, offset, and gain errors.

### 9.5.1.6 Cyclic Redundancy Check (CRC)

The CRC word is the last device word in the DIN and DOUT data frame. The CRC device word is optional and is enabled by the CRC\_EN control bit in the **D\_SYS\_CFG register**. When enabled, a 16-bit CRC data check word is present in the 16 most significant bits of the last device word in the data frame on both DIN and DOUT. Use the CRC to provide detection of single and multiple bit errors during data transmission.

The ADS131A0x implements a standard CRC16-CCITT algorithm using a polynomial of 11021h and an initial remainder of FFFFh.

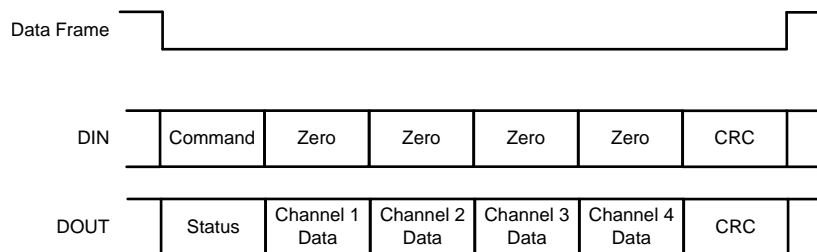
The CRC on all DIN commands is verified by the device prior to command execution except for the WREGS command; see the **WREGS: Write Multiple Registers** section. The WREGS command does not check the CRC prior to writing registers but does indicate if an error occurred. If the CRC on DIN is incorrect, F\_CHECK in the **STAT\_1 register** is set to 1 and the input command does not execute (for all commands except WREGS). Fill the unused device words on DIN with zeroes, placing the CRC word in the last device word.

The number of input CRC errors is counted and stored in the **error count** register. The register counts errors up to 255 before rolling over to 0. The counter is cleared by reading the ERROR\_CNT register.

The CRC is calculated using specific device words in the data frame determined by the CRC\_MODE and FIXED bits in the D\_SYS\_CFG register. For DIN, when the FIXED bit is 0, all device words are calculated into the CRC. When the FIXED bit is 1 and the CRC\_MODE bit is 1, all device words are used for calculating the CRC on DIN. When the FIXED bit is 1 and the CRC\_MODE bit is 0, only the command word and device words are used for the CRC calculation on DIN.

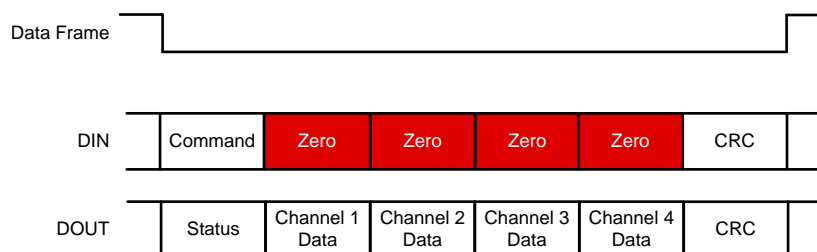
For DOUT, when the FIXED bit is 0, all device words in the data frame are included in the CRC calculation. When the FIXED bit is 1 and CRC\_MODE is 1, all device words in the data frame are included in the DOUT CRC calculation. When the FIXED bit is 1 and CRC\_MODE is 0, only the command, status word, and active device words are included in the DOUT CRC calculation. When hamming codes are enabled, the hamming byte of each word is omitted in the CRC calculation.

Figure 55 and Figure 56 show which device words are included in the CRC calculation on DIN and DOUT under various CRC settings. In the following examples, the device words that are not checked are highlighted in red.



NOTE: CRC\_MODE = 1.

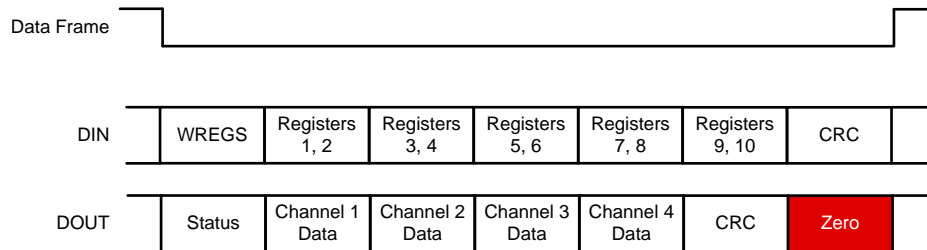
Figure 55. CRC with CRC\_MODE = 1



NOTE: CRC\_MODE = 0.

Figure 56. CRC with CRC\_MODE = 0

The WREGS command causes the data frame to extend until the last register is written (see the [WREGS: Write Multiple Registers](#) section for more details), thus requiring the CRC to be placed on DIN after the data frame extension. The ADS131A0x places the CRC word on DOUT at the end of all ADC data. When sending the WREGS command, the device words following the CRC on DOUT are padded with zeroes and are not included in the CRC calculation; see [Figure 57](#). The device words that are not checked are highlighted in red.



**Figure 57. CRC Using the WREGS Command**

#### 9.5.1.6.1 Computing the CRC

The CRC byte is the 16-bit remainder of the bitwise exclusive-OR (XOR) operation of the data bytes by a CRC polynomial. The CRC is based on the CRC-CCITT polynomial  $X_{16} + X_{12} + X_5 + 1$ .

The binary coefficients of the polynomial are: 10001000 00010001. Calculate the CRC by dividing the data bytes (with the XOR operation, thus excluding the CRC) with the polynomial and compare the calculated CRC values to the provided CRC value. If the values do not match, then a data transmission error has occurred. In the event of a data transmission error, read or write the data again.

The following list shows a general procedure to compute the CRC value. Assume the shift register is 16 bits wide:

1. Set the polynomial value to 1021h
2. Set the shift register to FFFFh
3. For each byte in the data stream:
  - Shift the next data byte left by eight bits and XOR the result with the shift register, placing the result into the shift register
  - Do the following eight times:
    1. If the most significant bit of the shift register is set, shift the register left by one bit and XOR the result with the polynomial, placing the result into the shift register
    2. If the most significant bit of the shift register is not set, shift the register left by one bit
4. The result in the shift register is the CRC check value

#### NOTE

The CRC algorithm used here employs an assumed set X16 bit. This bit is divided out by left-shifting it 16 times out of the register prior to XORing with the polynomial register. This process makes the CRC calculable with a 16-bit word size.

#### 9.5.1.7 Hamming Code Error Correction

Hamming code is an optional data integrity feature used to correct for single-bit errors and detect multiple-bit errors in each device word. Enable hamming code with M2 pin settings (see [Table 10](#) for details). Tie the M2 pin to IOVDD through a < 1-kΩ resistor to enable hamming code, or tie the M2 pin to GND through a < 1-kΩ resistor to disable hamming code.

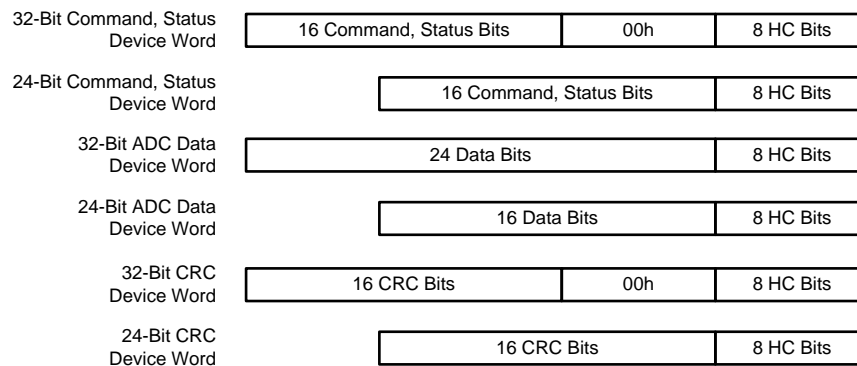


Hamming code is only supported in 24-bit and 32-bit device word sizes. The ADS131A0x outputs 24 bits of conversion data and an 8-bit hamming code per channel when operating in 32-bit word size. The ADS131A0x outputs 16 bits of conversion data and an 8-bit hamming code per channel when operating in 24-bit word size. [Table 10](#) lists the configuration options of the M1 and M2 hardware pins and the associated device word size. The status and command words are always 16 bits in length, reserving the eight least significant bits for hamming code.

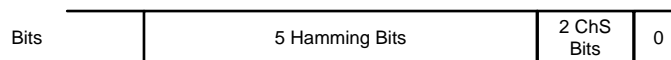
**Table 10. M2 Pin Setting Options**

| M2 STATE | M1 STATE | DEVICE WORD SIZE | CONVERSION DATA   | HAMMING DATA  |
|----------|----------|------------------|-------------------|---------------|
| IOVDD    | IOVDD    | 32 bits          | 24 bits           | On: 8 bits    |
|          | GND      | 24 bits          | 16 bits           | On: 8 bits    |
|          | Float    | Not available    | Not available     | Not available |
| GND      | IOVDD    | 32 bits          | 24 bit + 8 zeroes | Off           |
|          | GND      | 24 bits          | 24 bit            | Off           |
|          | Float    | 16 bits          | 16 bit            | Off           |
| Float    | N/A      | Not available    | Not available     | Not available |

When enabled, the hamming code byte is an additional 8-bits appended to the end of each device word on both the input and output, as shown in [Figure 58](#). This additional eight bits are a combination of five hamming code (Hamming) bits, two checksum (ChS) bits, and one zero bit, as shown in [Figure 59](#).



**Figure 58. Hamming Code on Each Device Word**



**Figure 59. Hamming Code Bit Allocation**

CRC can be used with the hamming code error correction enabled. When the hamming code error correction is enabled with CRC, the 8-bit hamming data per device word is not protected by the CRC and is ignored in the calculation. For example, if the 32-bit word size is used with hamming code enabled, the CRC check only uses the most significant 24 bits of each device word and ignores the last eight bits used for the hamming code. The CRC considers each device word as being 24 bits.

Table 11 shows the hamming bit coverage for 24-bit data. The encoded data bit 00 corresponds to the LSB of the data and bit 23 is the MSB of the data. The hamming code bits are interleaved within the data bits. H0 is the least significant bit of the hamming code and H4 is the most significant bit.

Table 11. ADS131A0x Hamming Codes

| HAMMING OR DATA     | D  | D  | D  | D  | D  | D  | D  | D  | D  | D  | D  | D  | D  | H  | D  | D  | D  | D  | D  | D  | H  | D  | D  | D  | H  | D  | H  | H  |    |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Encoded data bits   | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 10 | 11 | 12 | 04 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 03 | 20 | 21 | 22 | 02 | 23 | 01 | 00 |
| Parity bit coverage | H0 | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    | x  |    |
|                     | H1 |    |    | x  | x  |    |    | x  | x  |    |    | x  | x  |    |    | x  | x  |    |    | x  | x  |    |    | x  | x  |    |    | x  | x  |
|                     | H2 | x  | x  |    |    |    |    | x  | x  | x  | x  |    |    |    |    | x  | x  | x  | x  |    |    |    |    | x  | x  | x  | x  |    |    |
|                     | H3 | x  | x  | x  | x  | x  | x  |    |    |    |    |    |    |    |    | x  | x  | x  | x  | x  | x  | x  |    |    |    |    |    |    |    |
|                     | H4 | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  | x  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

9.5.2 SPI Interface

The device SPI-compatible serial interface is used to read conversion data, read and write the device configuration registers, and control device operation. Only CPOL = 0 and CPHA = 1 are supported. The interface consists of five control lines (CS, SCLK, DIN, DOUT, and DRDY) but can be used with only four signals as well. Three interface configurations are selectable in the ADS131A0x by M0 pin settings, as shown in Table 12: asynchronous interrupt mode, synchronous master mode, and synchronous slave mode.

The M0 pin settings (listed in Table 12) are latched on power-up to set the interface. The same communication lines are used for all three interface modes: SCLK, DIN, DOUT, and DRDY, with CS as an option in 5-wire mode. An optional sixth signal (DONE) is available for use when chaining multiple devices, as discussed in the ADC Frame Complete (DONE) section. Tie the M0 pin high to IOVDD through a < 1-kΩ resistor, low to GND through a < 1-kΩ resistor, or leave the M0 pin floating.

Table 12. M0 Pin Settings

| M0 STATE | INTERFACE MODE              |
|----------|-----------------------------|
| IOVDD    | Asynchronous interrupt mode |
| GND      | Synchronous master mode     |
| Float    | Synchronous slave mode      |

9.5.2.1 Asynchronous Interrupt Mode

The SPI uses five interface signals: CS, SCLK, DIN, DOUT, and DRDY in asynchronous interrupt mode. Use the four interface lines, CS, SCLK, DIN, and DOUT to read conversion data, read and write registers, and send commands to the ADS131A0x. Use the DRDY output as a status signal to indicate when new conversion data are ready. Figure 60 shows typical device connections for the ADS131A0x to a host microprocessor or digital signal processor (DSP) in asynchronous interrupt mode.

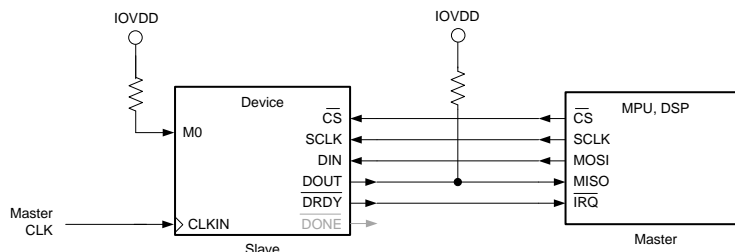


Figure 60. Asynchronous Interrupt Mode Device Connections

### 9.5.2.1.1 Chip Select ( $\overline{CS}$ )

Chip select ( $\overline{CS}$ ) is an active-low input that selects the device for SPI communication and controls the beginning and end of a data frame in asynchronous interrupt mode.  $\overline{CS}$  must remain low for the entire duration of the serial communication to complete a command or data readback. When  $\overline{CS}$  is taken high, the serial interface (including the data frame) is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state.  $\overline{DRDY}$  transitions low when data conversion is complete, regardless of whether  $\overline{CS}$  is high or low.

### 9.5.2.1.2 Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data into and out of the device on DIN and DOUT, respectively. SCLKs can be sent continuously or in byte increments to the ADC. Even though the input has hysteresis, keeping the SCLK signal as clean as possible is recommended to prevent glitches from accidentally shifting data. When the serial interface is idle, hold SCLK low.

### 9.5.2.1.3 Data Input (DIN)

Use the data input (DIN) pin and SCLK to communicate with the ADS131A0x (user commands and register data). The device latches data on DIN on the SCLK falling edge. The command or register write takes effect following completion of the data frame.

### 9.5.2.1.4 Data Output (DOUT)

Use the data output (DOUT) pin with SCLK to read conversion and register data from the ADS131A0x. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when  $\overline{CS}$  is high or after the least significant bit is shifted from the output shift register (see the  $t_{h(LSB)}$  specification in the [Switching Characteristics: Asynchronous Interrupt Interface Mode](#) table).

### 9.5.2.1.5 Data Ready ( $\overline{DRDY}$ )

$\overline{DRDY}$  indicates when a new conversion result is ready for retrieval. When  $\overline{DRDY}$  transitions from high to low, new conversion data are ready. The  $\overline{DRDY}$  signal remains low for the duration of the data frame and returns high either when  $\overline{CS}$  returns high (signaling the completion of the frame), or prior to new data being available. The high-to-low  $\overline{DRDY}$  transition occurs at the set data rate regardless of the  $\overline{CS}$  state. If data are not completely shifted out when new data are ready, the  $\overline{DRDY}$  signal toggles high for a duration of  $0.5 \times t_{MOD}$  and back low. The device sets the F\_DRDY bit in the STAT\_1 register indicating that the DOUT output shift register is not updated with the new conversion result. [Figure 61](#) shows an example of new data being ready before previous data are shifted out, causing the new conversion result to be lost. The  $\overline{DRDY}$  pin is always actively driven, even when  $\overline{CS}$  is high.

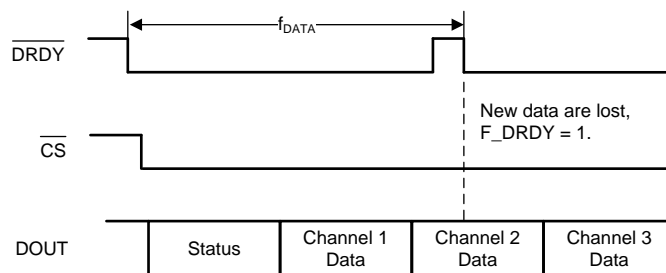


Figure 61. Asynchronous Interrupt Mode Conversion Update During a Read Operation

### 9.5.2.1.6 Asynchronous Interrupt Mode Data Retrieval

Figure 62 shows the relationship between  $\overline{\text{DRDY}}$ ,  $\overline{\text{CS}}$ , SCLK, DIN, and DOUT during data retrieval. The high-to-low  $\overline{\text{DRDY}}$  transition indicates that new data are available. Transition  $\overline{\text{CS}}$  from high to low to begin a data frame. At the end of the data frame,  $\overline{\text{CS}}$  returns high and brings  $\overline{\text{DRDY}}$  high.

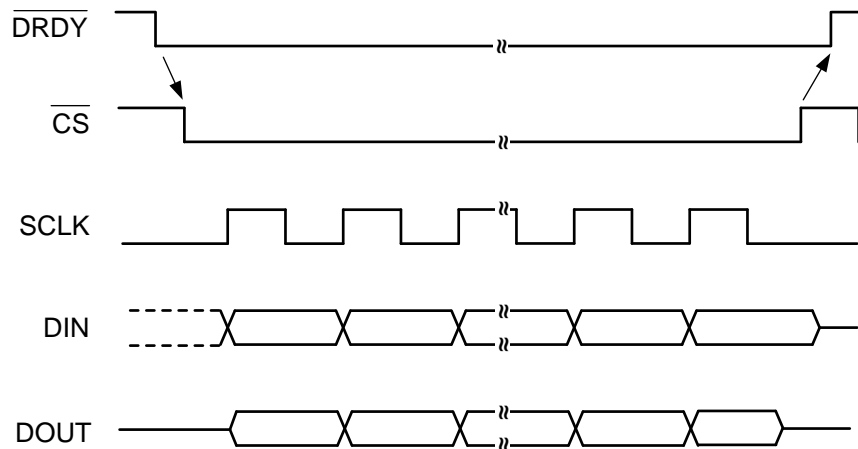


Figure 62.  $\overline{\text{DRDY}}$  Behavior with Data Retrieval in Asynchronous Interrupt Mode

### 9.5.2.2 Synchronous Master Mode

The SPI uses four interface signals: SCLK, DIN, DOUT, and  $\overline{\text{DRDY}}$  in synchronous master mode. Connect the  $\overline{\text{CS}}$  signal to the  $\overline{\text{DONE}}$  signal when using a single device in synchronous master mode. The SCLK,  $\overline{\text{DRDY}}$ , and DOUT signals are outputs from the device. Provide DIN from the microprocessor (MPU) or DSP using the SCLK edge timing of the ADS131A0x. Figure 63 shows typical device connections for the ADS131A0x in synchronous master mode to a host microprocessor or DSP.

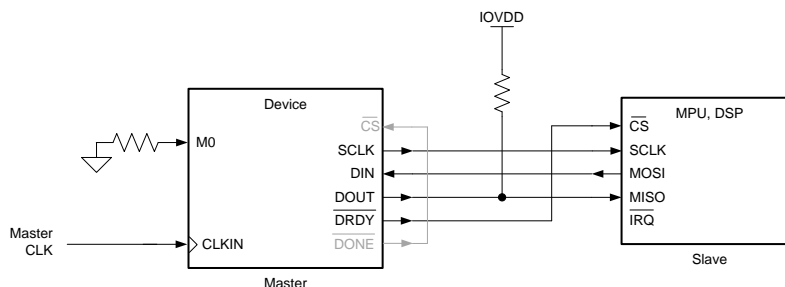


Figure 63. Synchronous Master Mode Device Connections

#### 9.5.2.2.1 Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. Use SCLK to shift in commands and shift out data from the device, similar to the description provided in the [Asynchronous Interrupt Mode](#) section. The SCLK output equals the ICLK derived from the input clock, CLKIN, using the clock divider control in the [CLK1 register](#). SCLKs continuously output at the ICLK rate with the beginning of a data frame set by a  $\overline{\text{DRDY}}$  falling edge.

#### 9.5.2.2.2 Data Input (DIN)

Use the data input (DIN) pin and SCLK to communicate with the ADS131A0x (user commands and register data). The device latches data on DIN on the SCLK falling edge. The command or register write takes effect following completion of the data frame.

### 9.5.2.2.3 Data Output (DOUT)

Use the data output pin (DOUT) with SCLK to read conversion and register data from the ADS131A0x. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high impedance state when  $\overline{CS}$  is high or after the least significant bit is shifted from the output shift register (see the  $t_{h(LSB)}$  specification in the [Switching Characteristics: Asynchronous Interrupt Interface Mode](#) table).

### 9.5.2.2.4 Data Ready ( $\overline{DRDY}$ )

The  $\overline{DRDY}$  signal is an output that functions as a new data ready indicator and as the control for the start and stop of a data frame. A high-to-low transition of  $\overline{DRDY}$  from the ADC indicates that the output shift register is updated with new data and begins a new data frame. Subsequent SCLKs shift out the first device word on DOUT.

### 9.5.2.2.5 Chip Select ( $\overline{CS}$ )

For single device operation in synchronous master mode, tie the  $\overline{CS}$  line to the  $\overline{DONE}$  output signal.

### 9.5.2.2.6 Synchronous Master Mode Data Retrieval

Figure 64 shows the relationship between  $\overline{DRDY}$ , DOUT, DIN, and SCLK during data retrieval in synchronous master mode. The high-to-low  $\overline{DRDY}$  transition from the ADS131A0x starts a data frame and indicates that new data are available. DIN and DOUT transition on the SCLK rising edge. After the LSB is shifted out  $\overline{DRDY}$  returns high, completing the data frame. The ICLK speed must be fast enough to shift out the required bits before new data are available because ICLK determines the SCLK output rate, as described in the [Serial Clock \(SCLK\)](#) section. Tie the CS signal to the DONE signal in single device synchronous master mode.

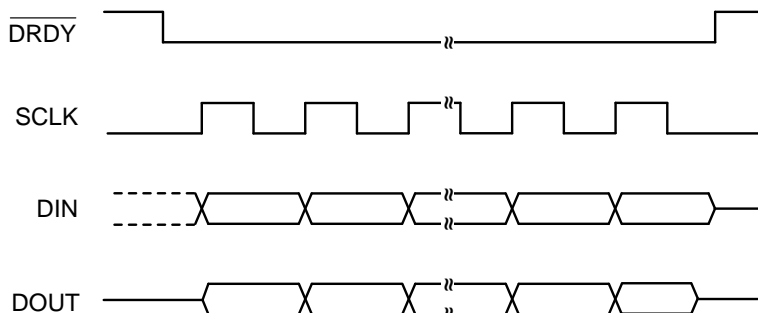


Figure 64. Data Retrieval in Synchronous Master Mode

### 9.5.2.3 Synchronous Slave Mode

The SPI uses five interface signals:  $\overline{CS}$ , SCLK, DIN, DOUT, and  $\overline{DRDY}$  in synchronous slave mode. The  $\overline{CS}$ , SCLK, DIN, and  $\overline{DRDY}$  signals are inputs to the device and the DOUT signal is an output.  $\overline{DRDY}$  can be tied directly to  $\overline{CS}$  (for a total of four interface lines) or can be used independently as a fourth input signal for synchronization to an external event; see the [Data Ready \( \$\overline{DRDY}\$ \)](#) section for more information on using the  $\overline{DRDY}$  line for synchronization. Figure 65 shows typical device connections for the ADS131A0x in synchronous slave mode to a host microprocessor or DSP.

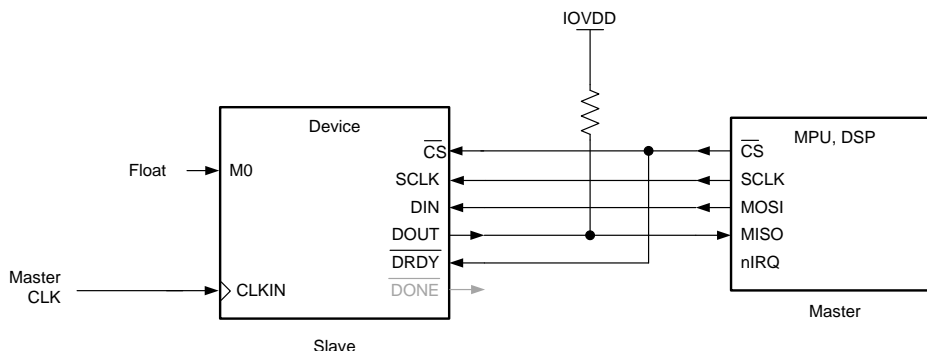


Figure 65. Synchronous Slave Mode Device Connections

### 9.5.2.3.1 Chip Select ( $\overline{CS}$ )

Chip select ( $\overline{CS}$ ) is an active-low input that selects the device for SPI communication and controls the beginning and end of a data frame in synchronous slave mode.  $\overline{CS}$  must remain low for the entire duration of the serial communication to complete a command or data readback. When  $\overline{CS}$  is taken high, the serial interface (including the data frame) is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. Tie  $\overline{CS}$  directly to the  $\overline{DRDY}$  input signal to minimize communication lines as long as the synchronization timing in [Figure 5](#) is met. Otherwise, the  $\overline{CS}$  line can be used independent of  $\overline{DRDY}$ .

### 9.5.2.3.2 Serial Clock (SCLK)

SCLK is the SPI serial clock. Use SCLK to shift in commands on DIN and shift out data from the device on DOUT, similar to the description in the [Asynchronous Interrupt Mode](#) section.

If the SCLK source is free-running, the SCLK input signal can be set as the ADC ICLK, removing the need of a separate CLKIN. The CLKSRC bit in the [CLK1 register](#) controls the source for the ADC ICLK. The modulator clock is derived from the ICLK using the ICLK\_DIV[2:0] bits in the [CLK2 register](#); see [Figure 35](#) for a diagram of how SCLK is routed into the device when serving as the ICLK. Setting SCLK as the internal ICLK requires that clocks are sent continuously without any delay or stop periods. Care must be taken to prevent glitches on SCLK at all times.

### 9.5.2.3.3 Data Input (DIN)

Use the data input pin (DIN) along with SCLK to communicate with the ADS131A0x (user commands and register data). The device latches data on DIN on the SCLK falling edge. The command or register write takes effect following the completion of the data frame.

### 9.5.2.3.4 Data Output (DOUT)

Use the data output pin (DOUT) with SCLK to read conversion and register data from the ADS131A0x. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high impedance state when  $\overline{CS}$  is high or after the least significant bit is shifted from the output shift register (see the  $t_{h(LSB)}$  specification in the [Switching Characteristics: Asynchronous Interrupt Interface Mode](#) table).

### 9.5.2.3.5 Data Ready ( $\overline{DRDY}$ )

In synchronous slave mode,  $\overline{DRDY}$  is an input signal that must be pulsed at the device set data rate. The  $\overline{DRDY}$  input signal is compared to an internally-generated data update signal to verify that these two signals are synchronized. A high-to-low  $\overline{DRDY}$  transition is expected at the programmed data rate or at multiples thereof. In the event of an unexpected  $\overline{DRDY}$  input pulse, the F\_RESYNC bit flags in the [STAT\\_1 register](#) and the ADC digital filter resets. Use the  $\overline{DRDY}$  input signal as a synchronization method to align new data ready with an external event or with a second ADS131A0x device. See the [Timing Requirements: Synchronous Slave Interface Mode](#) table for the timing requirements of the  $\overline{DRDY}$  input in synchronous slave mode.

### 9.5.2.3.6 Synchronous Slave Mode Data Retrieval

Figure 66 shows the relationship between  $\overline{\text{DRDY}}$ ,  $\overline{\text{CS}}$ , SCLK, DIN, and DOUT during data retrieval in synchronous slave mode. In synchronous slave mode, the high-to-low  $\overline{\text{DRDY}}$  transition sent from the processor must be synchronized with the data rate programmed, or multiples thereof, to avoid a digital filter reset. The data frame begins with a high-to-low  $\overline{\text{CS}}$  transition with or after  $\overline{\text{DRDY}}$  transitions low. The DIN and DOUT signals transition on the SCLK rising edge.  $\overline{\text{DRDY}}$  can return high at any point but must maintain a high-to-low transition at the set data rate to avoid a resynchronization event. To minimize interface lines, the  $\overline{\text{CS}}$  signal can be tied directly to the  $\overline{\text{DRDY}}$  signal; the timing specifications in the *Timing Requirements: Synchronous Slave Interface Mode* table are still maintained.

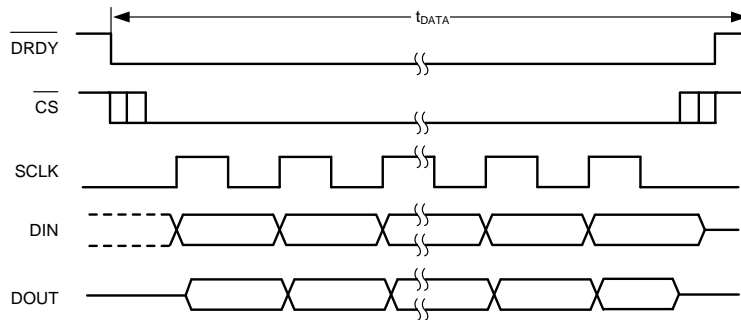


Figure 66. Data Retrieval in Synchronous Slave Mode

### 9.5.2.4 ADC Frame Complete ( $\overline{\text{DONE}}$ )

The  $\overline{\text{DONE}}$  output signal is an optional interface line that enables chaining multiple devices together to increase channel count. Connect the  $\overline{\text{DONE}}$  signal to the  $\overline{\text{CS}}$  of the next chained data converter in the system to control the start and stop of the subsequent converter interface. The  $\overline{\text{DONE}}$  signal transitions from high to low following the LSB being shifted out. The delay time from the SCLK falling edge shifting out the LSB to the high-to-low  $\overline{\text{DONE}}$  transition is configured using the DNDLY[1:0] bits in the D\_SYS\_CFG register. See Figure 6 for details of the signals and timings of the  $\overline{\text{DONE}}$  signal.

For single device operation, configure  $\overline{\text{DONE}}$  in the following ways:

- In asynchronous slave mode, either float the  $\overline{\text{DONE}}$  output signal or pull the  $\overline{\text{DONE}}$  output signal to IOVDD through a 100-k $\Omega$  pullup resistor.
- In synchronous master mode, tie the  $\overline{\text{DONE}}$  output signal to the  $\overline{\text{CS}}$  input line.
- In synchronous slave mode, either float the  $\overline{\text{DONE}}$  output signal or pull the  $\overline{\text{DONE}}$  output signal to IOVDD through a 100-k $\Omega$  pullup resistor.

See the *Multiple Device Configuration* section for more information on using the  $\overline{\text{DONE}}$  signal for multiple device chaining.

### 9.5.3 SPI Command Definitions

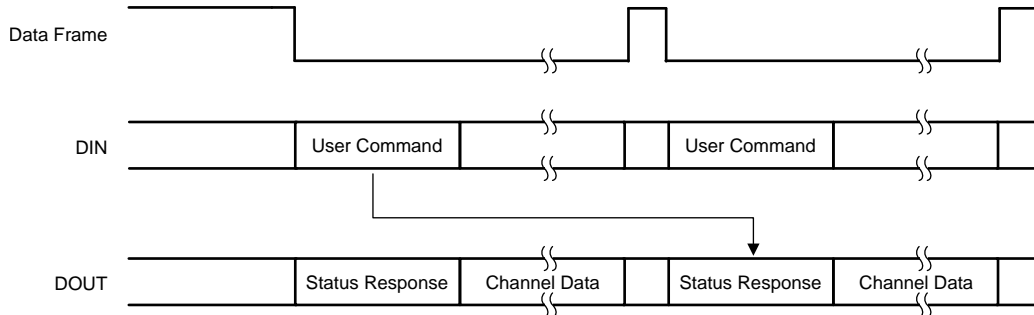
The ADS131A0x device operation is controlled and configured through ten commands. Table 13 summarizes the available commands. The commands are stand-alone, 16-bit words and reside in the first device word of the data frame. Write zeroes to the remaining LSBs when operating in either 24-bit or 32-bit word sizes because each command is 16-bits in length. The commands are decoded following the completion of a data frame and take effect immediately. Each recognized command is acknowledged with a status output in the first device word of the next data frame.

**Table 13. Command Definitions**

| COMMAND                                 | DESCRIPTION  | DEVICE WORD            | ADDITIONAL DEVICE WORD          | COMMAND STATUS RESPONSE      |
|---|--|------------------------|---------------------------------|------------------------------|
| <b>SYSTEM COMMANDS</b>                  |  |                        |                                 |                              |
| NULL                                    | Null command   | 0000h                  |                                 | STATUS                       |
| RESET                                   | Software reset   | 0011h                  |                                 | READY                        |
| STANDBY                                 | Enter low-power standby mode   | 0022h                  |                                 | ACK = 0022h                  |
| WAKEUP                                  | Wake-up from standby mode  | 0033h                  |                                 | ACK = 0033h                  |
| LOCK                                    | Places the interface in a locked state and ignores all commands except NULL, RREGS, and UNLOCK   | 0555h                  |                                 | ACK = 0555h                  |
| UNLOCK                                  | Brings the device out of an unconfigured POR state or a locked state   | 0655h                  |                                 | ACK = 0655h                  |
| <b>REGISTER WRITE AND READ COMMANDS</b> |  |                        |                                 |                              |
| RREG                                    | Read a single register   | (001a aaaa nnnn nnnn)b |                                 | REG                          |
| RREGS                                   | Read ( <i>nnnn nnnn</i> + 1) registers starting at address <i>a aaaa</i>   | (001a aaaa nnnn nnnn)b |                                 | RREGS                        |
| WREG                                    | Write a single register at address <i>a aaaa</i> with data <i>dddd dddd</i>  | (010a aaaa dddd dddd)b |                                 | REG (updated register)       |
| WREGS                                   | Write ( <i>nnnn nnnn</i> + 1) registers beginning at address <i>a aaaa</i> . Additional device words are required to send data ( <i>dddd dddd</i> ) to register address ( <i>a</i> ) and data ( <i>eeee eeee</i> ) to register address ( <i>a+1</i> ). Each device word contains data for two registers. The data frame size is extended by ( <i>n / 2</i> ) device words to allow for command completion. | (011a aaaa nnnn nnnn)b | ( <i>dddd dddd eeee eeee</i> )b | ACK = (010a_aaaa_nnnn_nnnn)b |



A command status response is 16 bits in length, located in the MSBs of the first device word in the DOUT data frame. The response indicates that the command in the previous data frame is executed. When operating in 24-bit or 32-bit word size modes, the remaining LSBs of the command status response device word read back as zero unless hamming code is used. An example showing the acknowledgment to a user input command is shown in [Figure 67](#).



**Figure 67. User Command Status Response**

Some user commands require multiple data words over multiple device frames. This section describes the commands and details which commands require multiple data words.

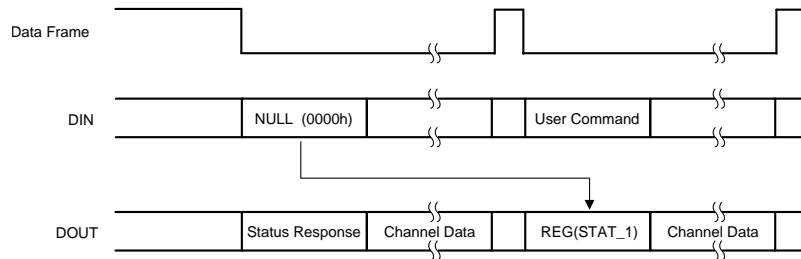
The command status responses to the user commands are listed in [Table 14](#). Every data frame begins with one of the listed command status responses on DOUT.

**Table 14. Command Status Responses**

| RESPONSE               | DESCRIPTION  | DEVICE WORD                                  | ADDITIONAL DEVICE WORD                               |
|------------------------|--|--|--|
| <b>SYSTEM RESPONSE</b> |  |  |  |
| READY                  | Fixed-status word stating that the device is in a power-up ready state or standby mode and is ready for use. The least significant byte of the device word indicates the address 0 hardware device ID code ( <i>da</i> ). In the READY state, the device transmits only one word, allowing a 1-word command to be received. An UNLOCK command must be issued before the device responds to other commands. | (FFdd)h                                      | —  |
| ACK                    | Acknowledgment response. The device has received and executed the command and repeats the received command ( <i>cccc</i> ) as the command status response. (A NULL input does not result in an ACK response).  | (cccc)h                                      | —  |
| STATUS/REG             | Status byte update. Register address <i>aaaa</i> contains data <i>dddd</i> . This command status response is the response to a recognized RREGS or WREG command. An automatic status update of register address (02h) is sent when the NULL command is sent.   | (001a <i>aaaa</i> <i>dddd</i> <i>dddd</i> )b | —  |
| RREGS                  | Response for read ( <i>nnnn</i> <i>nnnn</i> + 1) registers starting at address <i>aaaa</i> . Data for two registers are output per device word. If the resulting address extends beyond the usable register space, zeroes are returned for remaining non-existent registers. During an RREGS response, any new input commands are ignored until the RREGS status response completes.                       | (011a <i>aaaa</i> <i>nnnn</i> <i>nnnn</i> )b | ( <i>dddd</i> <i>dddd</i> <i>eeee</i> <i>eeee</i> )b |

### 9.5.3.1 NULL: Null Command

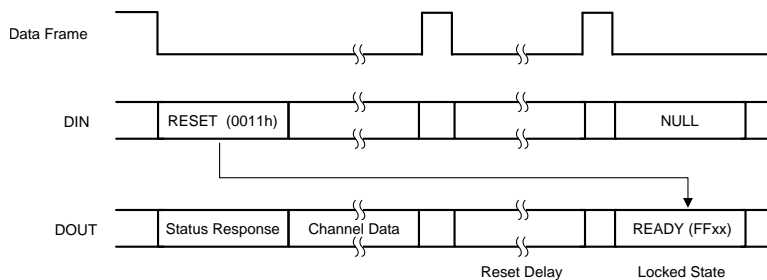
The NULL command has no effect on ADC registers or data. Rather than producing an ACK response on DOUT, the command issues a register readback of the [STAT\\_1 register](#) to monitor for general fault updates. An example of the response to a NULL command is shown in [Figure 68](#).



**Figure 68. NULL Command Status Response**

### 9.5.3.2 RESET: Reset to POR Values

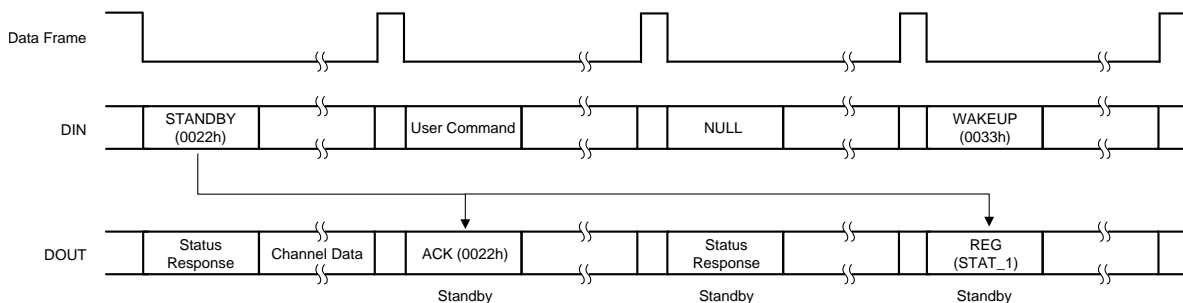
The RESET command places the ADC into a power-on reset (POR) state, resetting all user registers to the default states. The reset begins following the completion of the frame. When reset completes, the ADC enters a reset locked state and outputs the READY status response on DOUT as the command status response. An example of the response to a RESET command is shown in [Figure 69](#).



**Figure 69. RESET Command Status Response**

### 9.5.3.3 STANDBY: Enter Standby Mode

The STANDBY command places the ADC in a low-power standby mode, halting conversions. The digital interface remains powered, allowing all registers to retain the previous states. When in standby mode, writing and reading from registers is possible and any programmable bits that activate circuitry take effect in the device after the WAKEUP command is issued. The command status response following a STANDBY command is 0022h. In standby mode, the command status response is dependent on the user command that is sent. All ADC channels must be disabled (by writing to the [ADCx registers](#)) prior to entering standby mode to reduce current consumption. An example for the response to the STANDBY command and behavior when in standby mode is shown in [Figure 70](#).



**Figure 70. STANDBY Command Status Response**

### 9.5.3.4 WAKEUP: Exit STANDBY Mode

The WAKEUP command brings the ADC out of standby mode. The ADC channels must be enabled (by writing to the [ADCx registers](#)) before bringing the device out of standby mode. Allow enough time for all circuits in standby mode to power-up (see the [Electrical Characteristics](#) table for details). The command status response following a WAKEUP command is 0033h. An example showing the response to exiting standby mode using the WAKEUP command is shown in [Figure 71](#).

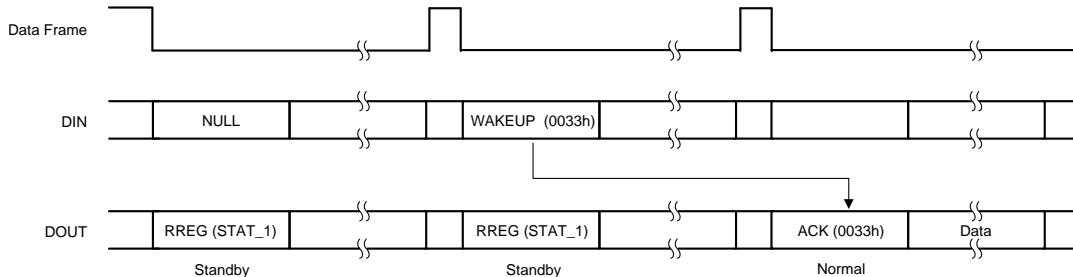


Figure 71. WAKEUP Command Status Response

### 9.5.3.5 LOCK: Lock ADC Registers

The LOCK command places the converter interface in a locked state where the interface becomes unresponsive to most input commands. The UNLOCK, NULL, RREG, and RREGS commands are the only commands that are recognized when reading back data. Following the LOCK command, the first DOUT status response reads 0555h followed by the command status response of a NULL command (by reading the [STAT\\_1](#) register). An example showing the response to sending a LOCK command and entering a register locked state is shown in [Figure 72](#).

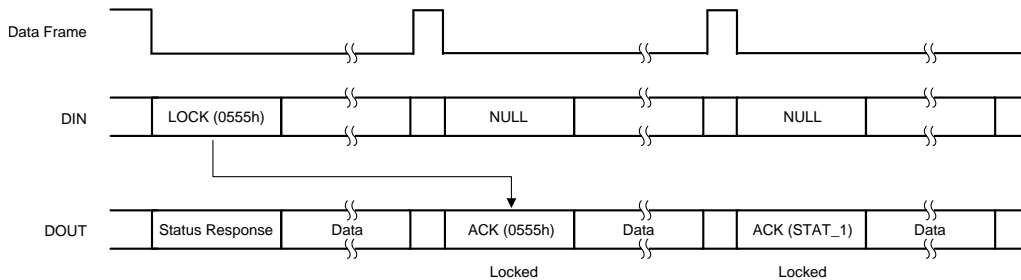


Figure 72. LOCK Command Status Response

### 9.5.3.6 UNLOCK: Unlock ADC Registers

The UNLOCK command brings the converter out of the locked state, allowing all registers to be accessed in the next data frame. The command status response associated with the UNLOCK command is 0655h. An example of bringing the interface out of the locked state using the UNLOCK command is shown in [Figure 73](#).

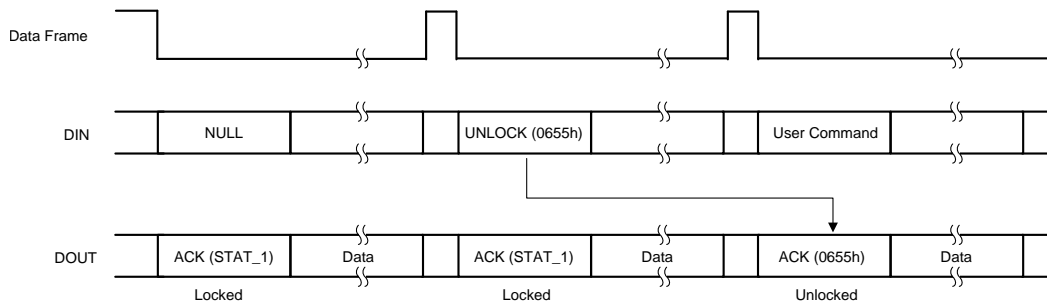
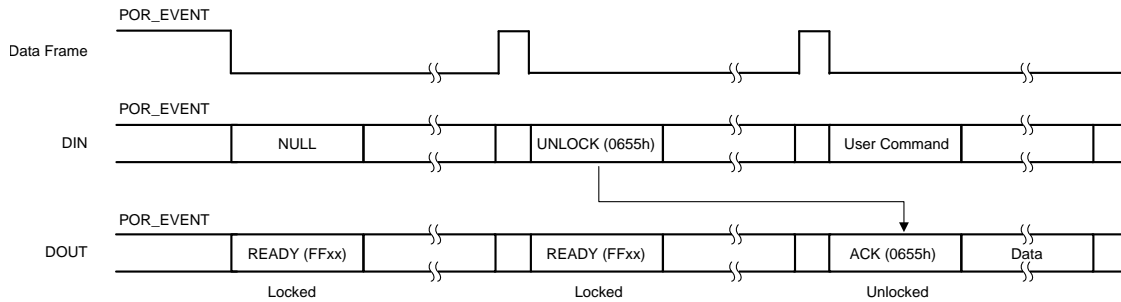


Figure 73. UNLOCK Command Status Response

**9.5.3.6.1 UNLOCK from POR or RESET**

When powering up the device or coming out of a power-on reset (POR) state, the ADC does not accept any commands. During this time, the jost can poll the ADC until the command status response reads back FFDDh (DD denotes the channel count defined by the NU\_CH[3:0] bits in the ID\_MSB register), indicating that the ADC power-on reset cycle is complete and that the ADC is ready to accept commands. Use the UNLOCK command to enable the SPI interface and begin communication with the device. The command status response associated with the UNLOCK command is 0655h. Figure 74 shows an example of unlocking the device after POR using the UNLOCK command.



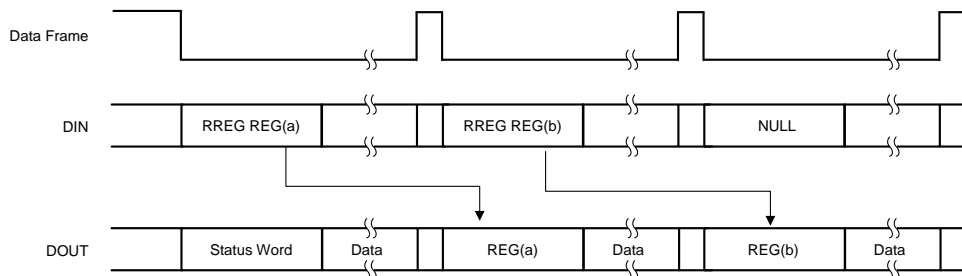
**Figure 74. UNLOCK from a POR Command Status Response**

**9.5.3.7 RREG: Read a Single Register**

The RREG command reads register data from the ADC. RREG is a 16-bit command containing the command, the register address, and the number of registers to be to read. The command details are shown below:

- First byte: 001a aaaa, where a aaaa is the register address
- Second byte: 00h

The ADC executes the command upon completion of the data frame and the register data transmission begins on the first device word of the following data frame. The response contains an 8-bit acknowledgement byte with the register address and an 8-bit data byte with the register content. Figure 75 shows an example command response to a single register read.



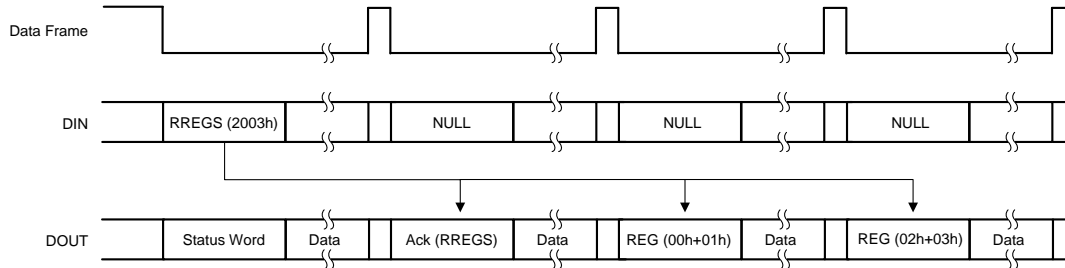
**Figure 75. RREGS Command Status Response (Single Register Read)**

**9.5.3.8 RREGS: Read Multiple Registers**

For a multiple register read back, the command status response exceeds the 16-bit reserved device word space, causing an overflow to additional command status words. The first command status response is an acknowledgment of multiple registers to be read back and the additional command status responses shift out register data. The command status response details are shown below:

- First command status response: 001a aaaa nnnn nnnn, where a aaaa is the starting register address and nnnn nnnn is the number of registers to read minus one (n-1).
- Additional command status responses: dddd dddd eeee eeee, where dddd dddd is the register data from the first register read back and eeee eeee is the register data from the second read back register.

The number of additional command status responses across multiple frames is dependent on the number of registers to be read back. During a RREGS command status response, any new input commands are ignored until the command completes by shifting out all necessary command status responses. If the resulting address extends beyond the usable register space, zeroes are returned for any remaining non-existent registers. An example of the command response to reading four registers using a RREGS command is shown in [Figure 76](#).



**Figure 76. RREGS Command Status Response (Multiple Register Read)**

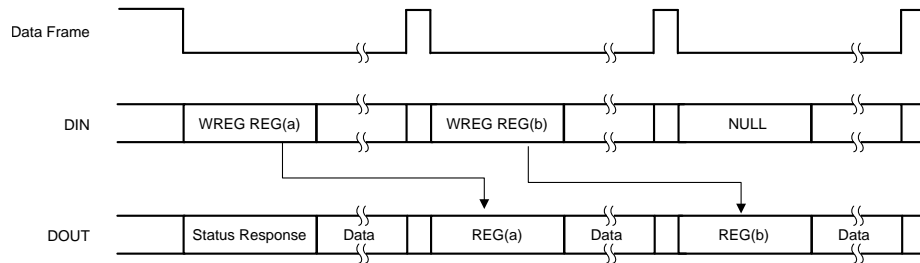
### 9.5.3.9 WREG: Write Single Register

The WREG command writes data to a single register. The single register write command is a two-byte command containing the address and the data to write to the address. The command details are shown below:

First byte: 010a aaaa, where a aaaa is the register address.

Second byte: dddd dddd, where dddd dddd is the data to write to the address.

The resulting command status response is a register read back from the updated register. An example of a single register write and response is shown in [Figure 77](#).



**Figure 77. WREG Command Status Response (Single Register Write)**

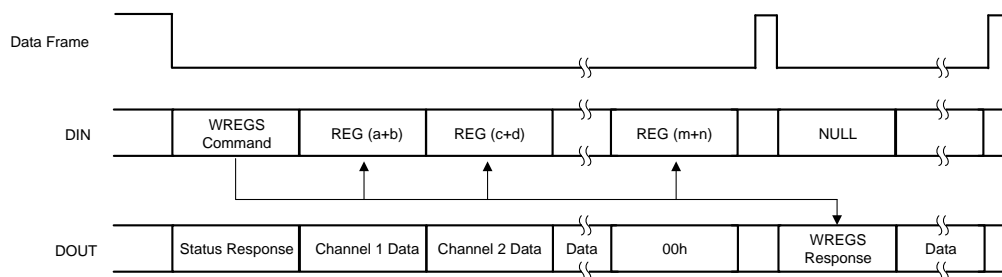
### 9.5.3.10 WREGS: Write Multiple Registers

The WREGS command writes data to multiple registers. The command steps through each register incrementally, thus allowing the user to incrementally write to each register. This process extends the data frame by (n) device words to complete the command. If the resulting address extends beyond the usable register space, any following data for non-existent registers are ignored. The 16 bits contained in the first device word contain the command, the starting register address, and the number of registers to write, followed by additional device words for the register data. The command details are shown below:

First user command device word:  $011a\ aaaa\ nnnn\ nnnn$ , where  $aaaa$  is the starting register address and  $nnnn\ nnnn$  is the number of registers to write minus one (n-1).

Additional user command device words:  $dddd\ dddd\ eeee\ eeee$ , where  $dddd\ dddd$  is the data to write to the first register and  $eeee\ eeee$  is the register data for the second register.

The user command device word uses the 16 MSBs regardless of word length (that is, only the 16 MSBs are used in 16-bit, 24-bit, or 32-bit word lengths). When additional command device words are required, only a maximum of two 8-bit registers can be written per command and any additional LSBs beyond 16 bits are ignored. The command status response for the WREGS command is  $010a\ aaaa\ nnnn\ nnnn$ , where  $aaaa$  is the starting register address and  $nnnn\ nnnn$  is the number of registers written minus one. An example of a multiple register write and the command status response is shown in [Figure 78](#).



**Figure 78. WREGS Command Status Response (Multiple Register Write)**

## 9.6 Register Maps

**Table 15. Register Map**

| ADDRESS<br>(Hex)                    | REGISTER NAME       | DEFAULT<br>SETTING | REGISTER BITS |          |            |         |              |              |            |         |
|-------------------------------------|---------------------|--------------------|---------------|----------|------------|---------|--------------|--------------|------------|---------|
|                                     |                     |                    | 7             | 6        | 5          | 4       | 3            | 2            | 1          | 0       |
| <b>Read Only ID Registers</b>       |                     |                    |               |          |            |         |              |              |            |         |
| 00h                                 | ID_MSB              | xxh                | NU_CH[7:0]    |          |            |         |              |              |            |         |
| 01h                                 | ID_LSB              | xxh                | REV_ID[7:0]   |          |            |         |              |              |            |         |
| <b>Status Registers</b>             |                     |                    |               |          |            |         |              |              |            |         |
| 02h                                 | STAT_1              | 00h                | 0             | F_OPC    | F_SPI      | F_ADCIN | F_WDT        | F_RESYNC     | F_DRDY     | F_CHECK |
| 03h                                 | STAT_P              | 00h                | 0             | 0        | 0          | 0       | F_IN4P       | F_IN3P       | F_IN2P     | F_IN1P  |
| 04h                                 | STAT_N              | 00h                | 0             | 0        | 0          | 0       | F_IN4N       | F_IN3N       | F_IN2N     | F_IN1N  |
| 05h                                 | STAT_S              | 00h                | 0             | 0        | 0          | 0       | 0            | F_STARTUP    | F_CS       | F_FRAME |
| 06h                                 | ERROR_CNT           | 00h                | ER[7:0]       |          |            |         |              |              |            |         |
| 07h                                 | STAT_M2             | xxh                | 0             | 0        | M2PIN[1:0] |         | M1PIN[1:0]   |              | M0PIN[1:0] |         |
| 08h                                 | Reserved            | 00h                | 0             | 0        | 0          | 0       | 0            | 0            | 0          | 0       |
| 09h                                 | Reserved            | 00h                | 0             | 0        | 0          | 0       | 0            | 0            | 0          | 0       |
| <b>User Configuration Registers</b> |                     |                    |               |          |            |         |              |              |            |         |
| 0Ah                                 | Reserved            | 00h                | 0             | 0        | 0          | 0       | 0            | 0            | 0          | 0       |
| 0Bh                                 | A_SYS_CFG           | 60h                | VNCPEN        | HRM      | 1          | VREF_4V | INT_REFEN    | COMP_TH[2:0] |            |         |
| 0Ch                                 | D_SYS_CFG           | 3Ch                | WDT_EN        | CRC_MODE | DNDLY[1:0] |         | HIZDLY[1:0]  |              | FIXED      | CRC_EN  |
| 0Dh                                 | CLK1                | 08h                | CLKSRC        | 0        | 0          | 0       | CLK_DIV[2:0] |              |            | 0       |
| 0Eh                                 | CLK2                | 86h                | ICLK_DIV[2:0] |          |            | 0       | OSR[3:0]     |              |            |         |
| 0Fh                                 | ADC_ENA             | 00h                | 0             | 0        | 0          | 0       | ENA[3:0]     |              |            |         |
| 10h                                 | Reserved            | 00h                | 0             | 0        | 0          | 0       | 0            | 0            | 0          | 0       |
| 11h                                 | ADC1                | 00h                | 0             | 0        | 0          | 0       | GAIN1_[2:0]  |              |            |         |
| 12h                                 | ADC2                | 00h                | 0             | 0        | 0          | 0       | GAIN2_[2:0]  |              |            |         |
| 13h                                 | ADC3 <sup>(1)</sup> | 00h                | 0             | 0        | 0          | 0       | GAIN3_[2:0]  |              |            |         |
| 14h                                 | ADC4 <sup>(1)</sup> | 00h                | 0             | 0        | 0          | 0       | GAIN4_[2:0]  |              |            |         |

(1) This register is for the ADS131A04 only. This register is reserved for the ADS131A02.

## 9.6.1 User Register Description

### 9.6.1.1 ID\_MSB: ID Control Register MSB (address = 00h) [reset = xxh]

This register is programmed during device manufacture to indicate device characteristics.

**Figure 79. ID\_MSB Register**

|            |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NU_CH[7:0] |   |   |   |   |   |   |   |
| R-xxh      |   |   |   |   |   |   |   |

LEGEND: R = Read only; -n = value after reset

**Table 16. ID\_MSB Register Field Descriptions**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 7:0 | NU_CH[7:0] | R    | xxh   | <b>Channel count identification bits.</b><br>These bits indicate the device channel count.<br>02h : 2-channel device<br>04h : 4-channel device |

### 9.6.1.2 ID\_LSB: ID Control Register LSB (address = 01h) [reset = xxh]

This register is reserved for future use.

**Figure 80. ID\_LSB Register**

|             |   |   |   |   |   |   |   |
|-------------|---|---|---|---|---|---|---|
| 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REV_ID[7:0] |   |   |   |   |   |   |   |
| R-xxh       |   |   |   |   |   |   |   |

LEGEND: R = Read only; -n = value after reset

**Table 17. ID\_LSB Register Field Descriptions**

| Bit | Field       | Type | Reset | Description  |
|-----|-------------|------|-------|--|
| 7:0 | REV_ID[7:0] | R    | xxh   | <b>Reserved.</b><br>These bits indicate the revision of the device and are subject to change without notice. |



### 9.6.1.3 STAT\_1: Status 1 Register (address = 02h) [reset = 00h]

This register contains general fault updates. This register is automatically transferred on the command status response when the NULL command is sent.

**Figure 81. STAT\_1 Register**

| 7    | 6     | 5     | 4       | 3     | 2        | 1      | 0       |
|------|-------|-------|---------|-------|----------|--------|---------|
| 0    | F_OPC | F_SPI | F_ADCIN | F_WDT | F_RESYNC | F_DRDY | F_CHECK |
| R-0h | R-0h  | R-0h  | R-0h    | R-0h  | R-0h     | R-0h   | R-0h    |

LEGEND: R = Read only; -n = value after reset

**Table 18. STAT\_1 Register Field Descriptions**

| Bit | Field    | Type | Reset | Description  |
|-----|----------|------|-------|--|
| 7   | Reserved | R    | 0h    | <b>Reserved.</b><br>Always read 0.   |
| 6   | F_OPC    | R    | 0h    | <b>Command fault.</b><br>This bit indicates that a received command is not recognized as valid and the command is ignored. This bit auto-clears on a STAT_1 data transfer, unless the condition remains.<br>When in a locked state, this bit is set if any command other than LOCK, UNLOCK, NULL, or RREGS is written to the device.<br>0 : No fault has occurred<br>1 : Possible invalid command is ignored   |
| 5   | F_SPI    | R    | 0h    | <b>SPI fault.</b><br>This bit indicates that one of the status bits in the STAT_S register is set. Read the STAT_S register to clear the bit.<br>0 : No fault has occurred<br>1 : A bit in the STAT_S register is set high   |
| 4   | F_ADCIN  | R    | 0h    | <b>ADC input fault.</b><br>This bit indicates that one of the ADC input fault detection bits in the STAT_P or STAT_N register is set. Read the STAT_P and STAT_N registers to clear the bit.<br>0 : No fault has occurred<br>1 : A bit in the STAT_P or STAT_N register is set high  |
| 3   | F_WDT    | R    | 0h    | <b>Watchdog timer timeout.</b><br>This bit indicates if the watchdog timer times out before a new data frame transfer occurs.<br>0 : No fault has occurred<br>1 : Timer has run out (resets following register read back)  |
| 2   | F_RESYNC | R    | 0h    | <b>Resynchronization fault.</b><br>This bit is set whenever the signal path is momentarily reset resulting from a $\overline{\text{DRDY}}$ synchronization event. This fault is only possible in synchronous slave mode.<br>0 : Devices are in sync<br>1 : Signal path is momentarily reset to maintain synchronization  |
| 1   | F_DRDY   | R    | 0h    | <b>Data ready fault.</b><br>This bit is set if data shifted out from the previous result are not complete by the time new ADC data are ready. The ADC DRDY line pulses, indicating that new data are available and overwrite the current data. This bit auto-clears on a STAT_1 transfer, unless the condition remains.<br>0 : Data read back complete before new data update<br>1 : New data update during DOUT data transmission   |
| 0   | F_CHECK  | R    | 0h    | <b>DIN check fault.</b><br>This bit is set if either of the following conditions are detected: <ul style="list-style-type: none"> <li>• Uncorrectable hamming error correction state is determined for any DIN word transfer when hamming code is enabled.</li> <li>• CRC check word on DIN fails. The input command that triggered this error is ignored.</li> </ul> This bit auto-clears on a STAT_S transfer, unless the condition remains.<br>0 : No error in DIN transmission<br>1 : DIN transmission error |

**9.6.1.4 STAT\_P: Positive Input Fault Detect Status Register (address = 03h) [reset = 00h]**

This register stores the status of whether the positive input on each channel exceeds the threshold set by the COMP\_TH[2:0] bits; see the [Input Overrange and Underrange Detection](#) section for details.

**Figure 82. STAT\_P Register**

| 7    | 6    | 5    | 4    | 3      | 2      | 1      | 0      |
|------|------|------|------|--------|--------|--------|--------|
| 0    | 0    | 0    | 0    | F_IN4P | F_IN3P | F_IN2P | F_IN1P |
| R-0h | R-0h | R-0h | R-0h | R-0h   | R-0h   | R-0h   | R-0h   |

LEGEND: R = Read only; -n = value after reset

**Table 19. STAT\_P Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description  |
|-----|-----------------------|------|-------|--|
| 7:4 | Reserved              | R    | 0h    | <b>Reserved.</b><br>Always read 0h.  |
| 3   | F_IN4P <sup>(1)</sup> | R    | 0h    | <b>AIN4P threshold detect.</b><br>0 : The channel 4 positive input pin does not exceed the set threshold<br>1 : The channel 4 positive input pin exceeds the set threshold |
| 2   | F_IN3P <sup>(1)</sup> | R    | 0h    | <b>AIN3P threshold detect.</b><br>0 : The channel 3 positive input pin does not exceed the set threshold<br>1 : The channel 3 positive input pin exceeds the set threshold |
| 1   | F_IN2P                | R    | 0h    | <b>AIN2P threshold detect.</b><br>0 : The channel 2 positive input pin does not exceed the set threshold<br>1 : The channel 2 positive input pin exceeds the set threshold |
| 0   | F_IN1P                | R    | 0h    | <b>AIN1P threshold detect.</b><br>0 : The channel 1 positive input pin does not exceed the set threshold<br>1 : The channel 1 positive input pin exceeds the set threshold |

(1) This bit is not available in the ADS131A02 and always read 0.

**9.6.1.5 STAT\_N: Negative Input Fault Detect Status Register (address = 04h) [reset = 00h]**

This register stores the status of whether the negative input on each channel exceeds the threshold set by the COMP\_TH[2:0] bits; see the [Input Overrange and Underrange Detection](#) section for details.

**Figure 83. STAT\_N Register**

| 7    | 6    | 5    | 4    | 3      | 2      | 1      | 0      |
|------|------|------|------|--------|--------|--------|--------|
| 0    | 0    | 0    | 0    | F_IN4N | F_IN3N | F_IN2N | F_IN1N |
| R-0h | R-0h | R-0h | R-0h | R-0h   | R-0h   | R-0h   | R-0h   |

LEGEND: R = Read only; -n = value after reset

**Table 20. STAT\_N Register Field Descriptions**

| Bit | Field                 | Type | Reset | Description  |
|-----|-----------------------|------|-------|--|
| 7:4 | Reserved              | R    | 0h    | <b>Reserved.</b><br>Always read 0h.  |
| 3   | F_IN4N <sup>(1)</sup> | R    | 0h    | <b>AIN4N threshold detect.</b><br>0 : The channel 4 negative input pin does not exceed the set threshold<br>1 : The channel 4 negative input pin exceeds the set threshold |
| 2   | F_IN3N <sup>(1)</sup> | R    | 0h    | <b>AIN3N threshold detect.</b><br>0 : The channel 3 negative input pin does not exceed the set threshold<br>1 : The channel 3 negative input pin exceeds the set threshold |
| 1   | F_IN2N                | R    | 0h    | <b>AIN2N threshold detect.</b><br>0 : The channel 2 negative input pin does not exceed the set threshold<br>1 : The channel 2 negative input pin exceeds the set threshold |
| 0   | F_IN1N                | R    | 0h    | <b>AIN1N threshold detect.</b><br>0 : The channel 1 negative input pin does not exceed the set threshold<br>1 : The channel 1 negative input pin exceeds the set threshold |

(1) This bit is not available in the ADS131A02 and always read 0.

**9.6.1.6 STAT\_S: SPI Status Register (address = 05h) [reset = 00h]**

This register indicates the detection of SPI fault conditions.

**Figure 84. STAT\_S Register**

| 7    | 6    | 5    | 4    | 3    | 2         | 1    | 0       |
|------|------|------|------|------|-----------|------|---------|
| 0    | 0    | 0    | 0    | 0    | F_STARTUP | F_CS | F_FRAME |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h      | R-0h | R-0h    |

LEGEND: R = Read only; -n = value after reset

**Table 21. STAT\_S Register Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7:3 | Reserved  | R    | 00h   | <b>Reserved.</b><br>Always read 00h.   |
| 2   | F_STARTUP | R    | 0h    | <b>ADC startup fault.</b><br>This bit indicates if an error is detected during power-up. This bit clears only when power is recycled.<br>0 : No fault has occurred<br>1 : A fault has occurred   |
| 1   | F_CS      | R    | 0h    | <b>Chip-select fault.</b><br>This bit is set if $\overline{CS}$ transitions when the SCLK pin is high. This bit auto-clears on a STAT_S transfer, unless the condition remains.<br>0 : $\overline{CS}$ is asserted or deasserted when SCLK is low<br>1 : $\overline{CS}$ is asserted or deasserted when SCLK is high |
| 0   | F_FRAME   | R    | 0h    | <b>Frame fault.</b><br>This bit is set if the device detects that not enough SCLK cycles are sent in a data frame for the existing mode of operation. This bit auto-clears on a STAT_S transfer, unless the condition remains.<br>0 : Enough SCLKs are sent per frame<br>1 : Not enough SCLKs are sent per frame     |

**9.6.1.7 ERROR\_CNT: Error Count Register (address = 06h) [reset = 00h]**

This register counts the hamming and CRC errors. This register is cleared when read.

**Figure 85. ERROR\_CNT Register**

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|------|------|------|------|------|------|------|
| ER7  | ER6  | ER5  | ER4  | ER3  | ER2  | ER1  | ER0  |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read only; -n = value after reset

**Table 22. ERROR\_CNT Register Field Descriptions**

| Bit | Field   | Type | Reset | Description   |
|-----|---------|------|-------|---|
| 7:0 | ER[7:0] | R    | 00h   | <b>Error tracking count.</b><br>These bits count the number of hamming and CRC errors on the input. The counter saturates if the number of errors exceeds 255, FFh. This register is cleared when read. |

**9.6.1.8 STAT\_M2: Hardware Mode Pin Status Register (address = 07h) [reset = xxh]**

This register indicates detection of the captured states of the hardware mode pins.

**Figure 86. STAT\_M2 Register**

| 7    | 6    | 5                   | 4 | 3                   | 2 | 1                   | 0 |
|------|------|---------------------|---|---------------------|---|---------------------|---|
| 0    | 0    | M2PIN[1:0]          |   | M1PIN[1:0]          |   | M0PIN[1:0]          |   |
| R-0h | R-0h | R-xh <sup>(1)</sup> |   | R-xh <sup>(1)</sup> |   | R-xh <sup>(1)</sup> |   |

LEGEND: R = Read only; -n = value after reset

(1) Reset values are dependent on the state of the hardware pin.

**Table 23. STAT\_M2 Register Field Descriptions**

| Bit | Field      | Type | Reset             | Description   |
|-----|------------|------|-------------------|---|
| 7:6 | Reserved   | R    | 0h                | <b>Reserved.</b><br>Always read 0h.   |
| 5:4 | M2PIN[1:0] | R    | xh <sup>(1)</sup> | <b>M2 captured state.</b><br>These bits indicate the captured state of the M2 hardware control pin.<br>00 : GND (hamming code word validation off)<br>01 : IOVDD (hamming code word validation on)<br>10 : No connection<br>11 : Reserved           |
| 3:2 | M1PIN[1:0] | R    | xh <sup>(1)</sup> | <b>M1 captured state.</b><br>These bits indicate the captured state of the M1 hardware control pin.<br>00 : GND (24-bit device word)<br>01 : IOVDD (32-bit device word)<br>10 : No connection (16-bit device word)<br>11 : Reserved                 |
| 1:0 | M0PIN[1:0] | R    | xh <sup>(1)</sup> | <b>M0 captured state.</b><br>These bits indicate the captured state of the M0 hardware control pin.<br>00 : GND (synchronous master mode)<br>01 : IOVDD (asynchronous slave mode )<br>10 : No connection (synchronous slave mode )<br>11 : Reserved |

(1) Reset values are dependent on the state of the hardware pin.

**9.6.1.9 Reserved Registers (address = 08h to 0Ah) [reset = 00h]**

This register is reserved for future use.

**Figure 87. Reserved Registers**

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|------|------|------|------|------|------|------|
| 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read only; -n = value after reset

**Table 24. Reserved Registers Field Descriptions**

| Bit | Field    | Type | Reset | Description                          |
|-----|----------|------|-------|--------------------------------------|
| 7:0 | Reserved | R    | 00h   | <b>Reserved.</b><br>Always read 00h. |

**9.6.1.10 A\_SYS\_CFG: Analog System Configuration Register (address = 0Bh) [reset = 60h]**

This register configures the analog features in the ADS131A0x.

**Figure 88. A\_SYS\_CFG Register**

| 7      | 6      | 5      | 4       | 3         | 2            | 1 | 0 |
|--------|--------|--------|---------|-----------|--------------|---|---|
| VNCPEN | HRM    | 1      | VREF_4V | INT_REFEN | COMP_TH[2:0] |   |   |
| R/W-0h | R/W-1h | R/W-1h | R/W-0h  | R/W-0h    | R/W-0h       |   |   |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 25. A\_SYS\_CFG Register Field Descriptions**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7   | VNCPEN       | R/W  | 0h    | <b>Negative charge pump enable.</b><br>This bit enables the negative charge pump when using a 3.0-V to 3.45-V unipolar power supply.<br>0 : Negative charge pump powered down<br>1 : Negative charge pump enabled   |
| 6   | HRM          | R/W  | 1h    | <b>High-resolution mode.</b><br>This bit selects between high-resolution and low-power mode.<br>0 : Low-power mode<br>1 : High-resolution mode  |
| 5   | Reserved     | R/W  | 1h    | <b>Reserved.</b><br>Always write 1h.  |
| 4   | VREF_4V      | R/W  | 0h    | <b>REFP reference voltage level.</b><br>This bit determines the REFP reference voltage level when using the internal reference.<br>0 : REFP is set to 2.442 V<br>1 : REFP is set to 4.0 V   |
| 3   | INT_REFEN    | R/W  | 0h    | <b>Internal reference enable.</b><br>This bit connects the internal reference voltage to the reference buffer to use the internal reference<br>0 : External reference voltage selected<br>1 : Internal reference voltage enabled and selected   |
| 2:0 | COMP_TH[2:0] | R/W  | 0h    | <b>Fault detect comparator threshold.</b><br>These bits determine the fault detect comparator threshold level settings; see the <a href="#">Input Overrange and Underrange Detection</a> section for details.<br><a href="#">Table 26</a> lists the bit settings for the high- and low-side thresholds. Values are approximate and are referenced to the device analog supply range.<br>When VNCPEN = 0, AVDD and AVSS are used for the high and low threshold.<br>When VNCPEN = 1, AVDD is used for the high threshold value. A –1.5-V supply, generated from the negative charge pump, is used for the low threshold value. |

**Table 26. COMP\_TH[2:0] Bit Settings**

| COMP_TH[2:0] | COMPARATOR HIGH-SIDE THRESHOLD (%) | COMPARATOR LOW-SIDE THRESHOLD (%) |
|--------------|------------------------------------|-----------------------------------|
| 000          | 95                                 | 5                                 |
| 001          | 92.5                               | 7.5                               |
| 010          | 90                                 | 10                                |
| 011          | 87.5                               | 12.5                              |
| 100          | 85                                 | 15                                |
| 101          | 80                                 | 20                                |
| 110          | 75                                 | 25                                |
| 111          | 70                                 | 30                                |

**9.6.1.11 D\_SYS\_CFG: Digital System Configuration Register (address = 0Ch) [reset = 3Ch]**

This register configures the digital features in the ADS131A0x.

**Figure 89. D\_SYS\_CFG Register**

| 7      | 6        | 5          | 4 | 3           | 2 | 1      | 0      |
|--------|----------|------------|---|-------------|---|--------|--------|
| WDT_EN | CRC_MODE | DNDLY[1:0] |   | HIZDLY[1:0] |   | FIXED  | CRC_EN |
| R/W-0h | R/W-0h   | R/W-3h     |   | R/W-3h      |   | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 27. D\_SYS\_CFG Register Field Descriptions**

| Bit | Field       | Type | Reset | Description   |
|-----|-------------|------|-------|---|
| 7   | WDT_EN      | R/W  | 0h    | <b>Watchdog timer enable.</b><br>This bit enables the watchdog timeout counter when set. Issue a hardware or software reset when disabling the watchdog timer for internal device synchronization; see the <a href="#">Watchdog Timer</a> section.<br>0 : Watchdog disabled<br>1 : Watchdog enabled |
| 6   | CRC_MODE    | R/W  | 0h    | <b>CRC mode select.</b><br>This bit determines which bits in the frame the CRC is valid for; see the <a href="#">Cyclic Redundancy Check (CRC)</a> section.<br>0 : CRC is valid on only the device words being sent and received<br>1 : CRC is valid on all bits received and transmitted           |
| 5:4 | DNDLY[1:0]  | R/W  | 3h    | <b><math>\overline{\text{DONE}}</math> delay.</b><br>These bits configure the time before the device asserts $\overline{\text{DONE}}$ after the LSB is shifted out.<br>00 : $\geq$ 6-ns delay<br>01 : $\geq$ 8-ns delay<br>10 : $\geq$ 10-ns delay<br>11 : $\geq$ 12-ns delay                       |
| 3:2 | HIZDLY[1:0] | R/W  | 3h    | <b>Hi-Z delay.</b><br>These bits configure the time that the device asserts Hi-Z on DOUT after the LSB of the data frame is shifted out.<br>00 : $\geq$ 6-ns delay<br>01 : $\geq$ 8-ns delay<br>10 : $\geq$ 10-ns delay<br>11 : $\geq$ 12-ns delay  |
| 1   | FIXED       | R/W  | 0h    | <b>Fixed word size enable.</b><br>This bit sets the data frame size.<br>0 : Device words per data frame depends on whether the CRC and ADCs are enabled<br>1 : Fixed six device words per frame for the ADS131A04 or fixed four device words per data frame for the ADS131A02                       |
| 0   | CRC_EN      | R/W  | 0h    | <b>Cyclic redundancy check enable.</b><br>This bit enables the CRC data word for both the DIN and DOUT data frame transfers. When enabled, DIN commands must pass the CRC checks to be recognized by the device.<br>0 : CRC disabled<br>1 : CRC enabled   |

**9.6.1.12 CLK1: Clock Configuration 1 Register (address = 0Dh) [reset = 08h]**

This register configures the ADC clocking and sets the internal clock dividers.

**Figure 90. CLK1 Register**

| 7      | 6      | 5      | 4      | 3 | 2            | 1 | 0      |
|--------|--------|--------|--------|---|--------------|---|--------|
| CLKSRC | 0      | 0      | 0      |   | CLK_DIV[2:0] |   | 0      |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h |   | R/W-4h       |   | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 28. CLK1 Register Field Descriptions**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7   | CLKSRC       | R/W  | 0h    | <b>ADC clock source.</b><br>This bit selects the source for ICLK; see the <a href="#">Clock</a> section for more information on ADC clocking.<br>0 : XTAL1/CLKIN pin or XTAL1/CLKIN and XTAL2 pins<br>1 : SCLK pin  |
| 6:4 | Reserved     | R/W  | 0h    | <b>Reserved.</b><br>Always write 0h.  |
| 3:1 | CLK_DIV[2:0] | R/W  | 4h    | <b>CLKIN divider ratio.</b><br>These bits set the CLKIN divider ratio to generate the internal $f_{\text{ICLK}}$ frequency. ICLK is used as the $f_{\text{SCLK}}$ output when the ADC is operating in synchronous master mode.<br>000 : Reserved<br>001 : $f_{\text{ICLK}} = f_{\text{CLKIN}} / 2$<br>010 : $f_{\text{ICLK}} = f_{\text{CLKIN}} / 4$<br>011 : $f_{\text{ICLK}} = f_{\text{CLKIN}} / 6$<br>100 : $f_{\text{ICLK}} = f_{\text{CLKIN}} / 8$<br>101 : $f_{\text{ICLK}} = f_{\text{CLKIN}} / 10$<br>110 : $f_{\text{ICLK}} = f_{\text{CLKIN}} / 12$<br>111 : $f_{\text{ICLK}} = f_{\text{CLKIN}} / 14$ |
| 0   | Reserved     | R/W  | 0h    | <b>Reserved.</b><br>Always write 0.   |

**9.6.1.13 CLK2: Clock Configuration 2 Register (address = 0Eh) [reset = 86h]**

This register configures the ADC modulator clock and oversampling ratio for the converter.

**Figure 91. CLK2 Register**

| 7             | 6 | 5 | 4      | 3        | 2 | 1 | 0 |
|---------------|---|---|--------|----------|---|---|---|
| ICLK_DIV[2:0] |   |   | 0      | OSR[3:0] |   |   |   |
| R/W-4h        |   |   | R/W-0h | R/W-6h   |   |   |   |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 29. CLK2 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7:5 | ICLK_DIV[2:0] | R/W  | 4h    | <b>ICLK divider ratio.</b><br>These bits set the divider ratio to generate the ADC modulator clock, $f_{MOD}$ , from the $f_{ICLK}$ signal.<br>000 : Reserved<br>001 : $f_{MOD} = f_{ICLK} / 2$<br>010 : $f_{MOD} = f_{ICLK} / 4$<br>011 : $f_{MOD} = f_{ICLK} / 6$<br>100 : $f_{MOD} = f_{ICLK} / 8$<br>101 : $f_{MOD} = f_{ICLK} / 10$<br>110 : $f_{MOD} = f_{ICLK} / 12$<br>111 : $f_{MOD} = f_{ICLK} / 14$  |
| 4   | Reserved      | R/W  | 0h    | <b>Reserved.</b><br>Always write 0h.  |
| 3:0 | OSR[3:0]      | R/W  | 6h    | <b>Oversampling ratio.</b><br>These bits set the OSR to create the ADC output data rate, $f_{DATA}$ ; see <a href="#">Table 30</a> for more details.<br>0000 : $f_{DATA} = f_{MOD} / 4096$<br>0001 : $f_{DATA} = f_{MOD} / 2048$<br>0010 : $f_{DATA} = f_{MOD} / 1024$<br>0011 : $f_{DATA} = f_{MOD} / 800$<br>0100 : $f_{DATA} = f_{MOD} / 768$<br>0101 : $f_{DATA} = f_{MOD} / 512$<br>0110 : $f_{DATA} = f_{MOD} / 400$<br>0111 : $f_{DATA} = f_{MOD} / 384$<br>1000 : $f_{DATA} = f_{MOD} / 256$<br>1001 : $f_{DATA} = f_{MOD} / 200$<br>1010 : $f_{DATA} = f_{MOD} / 192$<br>1011 : $f_{DATA} = f_{MOD} / 128$<br>1100 : $f_{DATA} = f_{MOD} / 96$<br>1101 : $f_{DATA} = f_{MOD} / 64$<br>1110 : $f_{DATA} = f_{MOD} / 48$<br>1111 : $f_{DATA} = f_{MOD} / 32$ |



**Table 30. Data Rate Settings**

| OSR[3:0] | OSR  | f <sub>DATA</sub> AT 2.048-MHz f <sub>MOD</sub><br>(kHz) | f <sub>DATA</sub> AT 4.096-MHz f <sub>MOD</sub><br>(kHz) | f <sub>DATA</sub> AT 4-MHz f <sub>MOD</sub><br>(kHz) |
|----------|------|--|--|--|
| 0000     | 4096 | 0.500  | 1.000  | 0.977  |
| 0001     | 2048 | 1.000  | 2.000  | 1.953  |
| 0010     | 1024 | 2.000  | 4.000  | 3.906  |
| 0011     | 800  | 2.560  | 5.120  | 5.000  |
| 0100     | 768  | 2.667  | 5.333  | 5.208  |
| 0101     | 512  | 4.000  | 8.000  | 7.813  |
| 0110     | 400  | 5.120  | 10.240   | 10.000   |
| 0111     | 384  | 5.333  | 10.667   | 10.417   |
| 1000     | 256  | 8.000  | 16.000   | 15.625   |
| 1001     | 200  | 10.240   | 20.480   | 20.000   |
| 1010     | 192  | 10.667   | 21.333   | 20.833   |
| 1011     | 128  | 16.000   | 32.000   | 31.250   |
| 1100     | 96   | 21.333   | 42.667   | 41.667   |
| 1101     | 64   | 32.000   | 64.000   | 62.500   |
| 1110     | 48   | 42.667   | 85.333   | 83.333   |
| 1111     | 32   | 64.000   | 128.000  | 125.000  |

**9.6.1.14 ADC\_ENA: ADC Channel Enable Register (address = 0Fh) [reset = 00h]**

This register controls the enabling of ADC channels.

**Figure 92. ADC\_ENA Register**

| 7      | 6      | 5      | 4      | 3        | 2 | 1 | 0 |
|--------|--------|--------|--------|----------|---|---|---|
| 0      | 0      | 0      | 0      | ENA[3:0] |   |   |   |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h   |   |   |   |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 31. ADC\_ENA Register Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7:4 | Reserved | R/W  | 0h    | <b>Reserved.</b><br>Always write 0h.  |
| 3:0 | ENA[3:0] | R/W  | 0h    | <b>Enable ADC channels.</b><br>These bits power-up or power-down the ADC channels. This setting is global for all channels.<br>0000 : All ADC channels powered down<br>1111 : All ADC channels powered up<br>All other settings: Do not use |

**9.6.1.15 Reserved Register (address = 10h) [reset = 00h]**

This register is reserved for future use.

**Figure 93. Reserved Register**

| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 0      | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read only; -n = value after reset

**Table 32. Reserved Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                           |
|-----|----------|------|-------|---------------------------------------|
| 7:0 | Reserved | R/W  | 00h   | <b>Reserved.</b><br>Always write 00h. |

**9.6.2 ADCx: ADC Channel Digital Gain Configuration Registers (address = 11h to 14h) [reset = 00h]**

These registers control the digital gain setting for the individual ADC channel (x denotes the ADC channel). For the ADS131A02, these registers are reserved.

**Figure 94. ADCx Register**

| 7      | 6      | 5      | 4      | 3      | 2           | 1 | 0 |
|--------|--------|--------|--------|--------|-------------|---|---|
| 0      | 0      | 0      | 0      | 0      | GAINx_[2:0] |   |   |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h      |   |   |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 33. ADCx Registers Field Descriptions**

| Bit | Field       | Type | Reset | Description   |
|-----|-------------|------|-------|---|
| 7:3 | Reserved    | R/W  | 00h   | <b>Reserved.</b><br>Always write 00h.   |
| 2:0 | GAINx_[2:0] | R/W  | 0h    | <b>Gain control (digital scaling).</b><br>These bits determine the digital gain of the ADC output.<br>000 : Gain = 1<br>001 : Gain = 2<br>010 : Gain = 4<br>011 : Gain = 8<br>100 : Gain = 16<br>101, 110, 111 : Reserved |

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

#### 10.1.1 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave any unused analog inputs floating or connected to AVSS. For the ADS131A02, the NC pins (pins 5-8) can be left floating or tied directly to AVSS.

Pin 24 is a digital output unconnected (NC) pin. Leave pin 24 floating or tied to GND through a 10-k $\Omega$  pull-down resistor.

Do not float unused digital inputs because excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, IOVDD or DGND, even when in power-down mode.

If the  $\overline{DONE}$  or  $\overline{DRDY}$  outputs are not used, leave these pins (pins 18 and 19, respectively) unconnected or tie these pins to IOVDD using a weak pullup resistor. Current consumed by the pullup resistor flows into the device and therefore increases power consumption.

#### 10.1.2 Power Monitoring Specific Applications

Each channel of the ADS131A0x is identical, giving designers the flexibility to sense voltage or current with any channel. Simultaneous sampling allows the application to calculate instantaneous power for any simultaneous voltage and current measurement. Figure 95 shows an example system that measures voltage and current simultaneously.

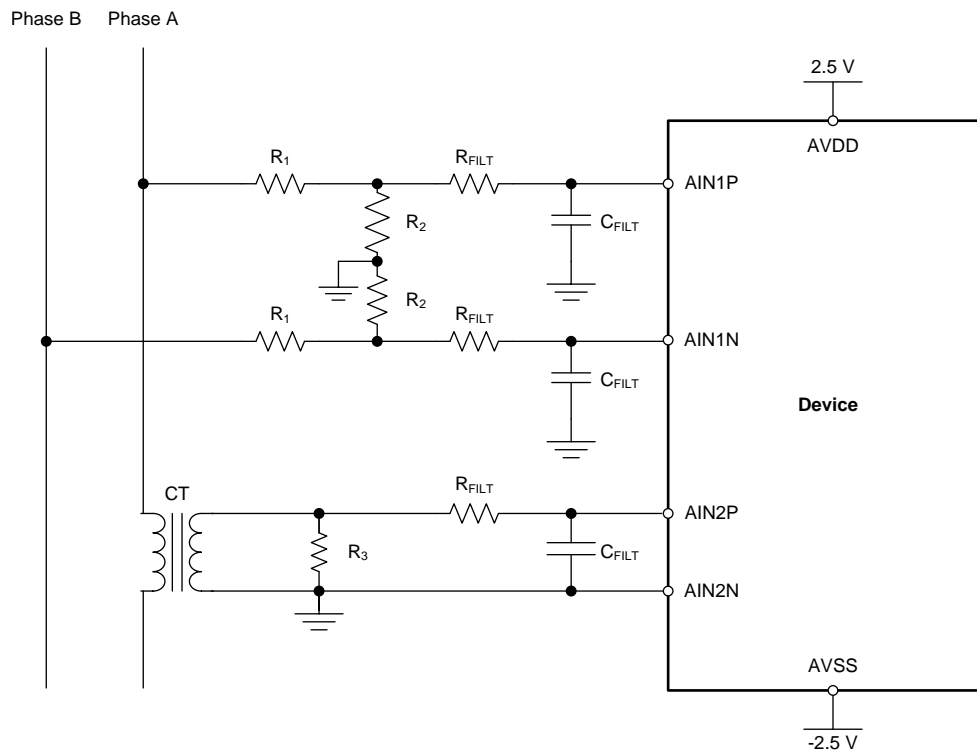


Figure 95. Example Power-Monitoring System

## Application Information (continued)

In [Figure 95](#), channel 1 is dedicated to measuring the voltage between phase A and phase B and channel 2 is dedicated to measuring the current on phase A.

The resistors  $R_1$  and  $R_2$  form a voltage divider that steps the line voltage down to within the measurement range of the ADC.  $R_1$  can be formed by multiple resistors in series to dissipate power across several components. This configuration is also valid if the voltage is measured with respect to neutral instead of between phases.

Channel 2 is dedicated to measuring current that flows on phase A. Resistor  $R_3$  serves as a burden resistor that shunts the current flowing across the secondary coil of the current transformer (CT). Current can also be measured using a Rogowski coil and an analog integrator or by performing integration digitally after a conversion.

The RC filters formed by  $R_{FILT}$  and  $C_{FILT}$  serve as antialiasing filters for the converter. If an application requires a steeper filter roll-off, a second-order RC filter can be used.

### 10.1.3 Multiple Device Configuration

The ADS131A0x allows the designer to add channels to the system by placing an additional device on the SPI bus. The first device in the chain of devices can be configured using any of the interface modes. All subsequent devices must be configured in synchronous slave mode. In all cases, however, the chain of ADS131A0x devices appear to the host as a single device with extra channels with the exception that each device sends individual status and data integrity words. In this manner, no additional pins on the host are required for more devices on the chain. There are no special provisions that must be made in the interface except for extending the frame to the appropriate length.

#### 10.1.3.1 First Device Configured in Asynchronous Interrupt Mode

[Figure 96](#) illustrates a multiple device configuration where the first device is configured in asynchronous interrupt mode as indicated by the state of the  $M0$  pin. The second ADS131A0x device and any additional devices are configured in synchronous slave mode. The  $\overline{DONE}$  pin of each device connects to the  $\overline{CS}$  of the subsequent device. In each case, after a device shifts out all of its data, the device deasserts  $\overline{DONE}$ , selecting the subsequent device for communication. The  $DOUT$  of a device whose contents are already shifted out assumes a high-impedance state, allowing the  $DOUT$  pins of all devices to be tied together. To send commands to specific devices, send the respective command of the device when that device is selected for communication. The  $DRDY$  output of the first device serves as the  $\overline{DRDY}$  input to all other devices to synchronize conversions. [Figure 97](#) illustrates an example interface timing diagram for this configuration.

Application Information (continued)

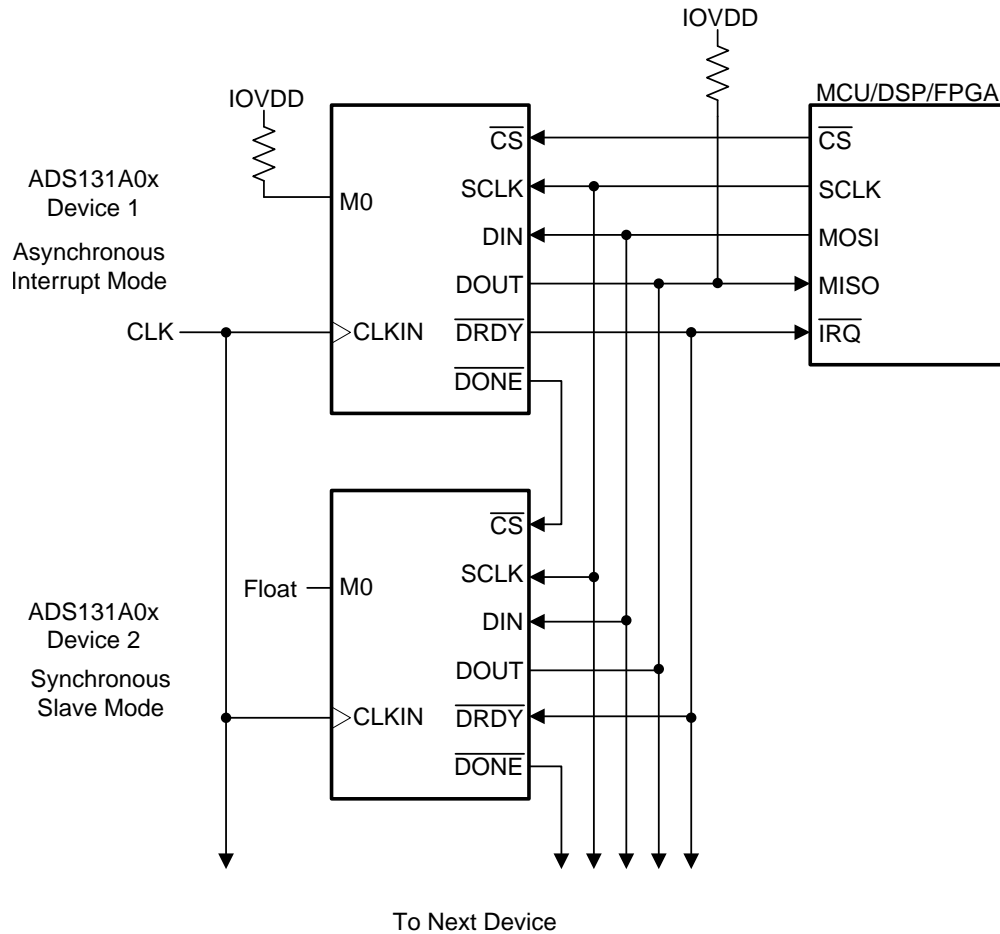
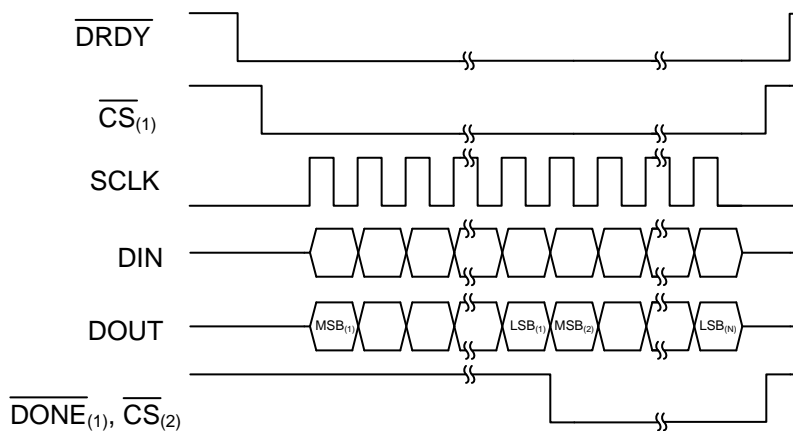


Figure 96. Multiple Device Configuration Using Asynchronous Interrupt Mode



NOTE: (1) denotes device 1, (2) denotes device 2, and (N) denotes device N.

Figure 97. Multiple Device Configuration Timing Diagram when Using Asynchronous Interrupt Mode

## Application Information (continued)

### 10.1.3.2 First Device Configured in Synchronous Master Mode

Figure 98 shows a multiple device configuration where the first device is configured in synchronous master mode as indicated by the state of the M0 pin. The second ADS131A0x device and any additional devices are configured in synchronous slave mode. The DONE pin of each device connects to the CS pin of the subsequent device. In each case, after a device shifts out all of its data, the device deasserts DONE, selecting the subsequent device for communication. Tie the DONE pin of the last device to the CS pin of the first device to allow for an immediate second read back of conversion data in the case a data integrity test failed. The DOUT of a device whose contents are already shifted out assumes a high-impedance state, allowing the DOUT pins of all devices to be tied together. To send commands to specific devices, send the respective command of the device when that device is selected for communication. The DRDY output of the first device serves as the DRDY input to all other devices to synchronize conversions. DRDY also serves as the chip-select or frame sync signal for the host. SCLK is free running with the same frequency as ICLK in this configuration. Figure 99 illustrates an example interface timing diagram for this configuration.

Application Information (continued)

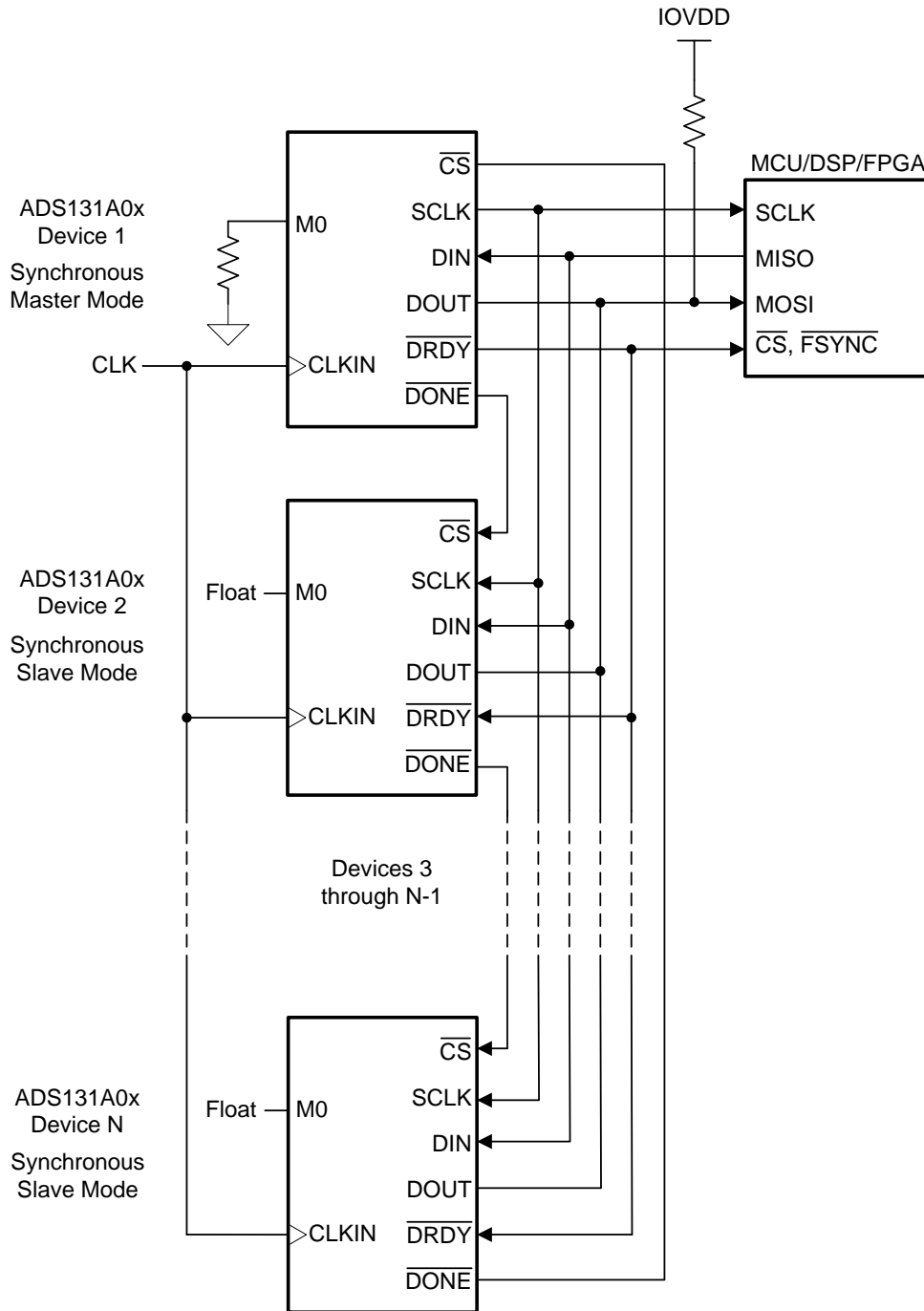
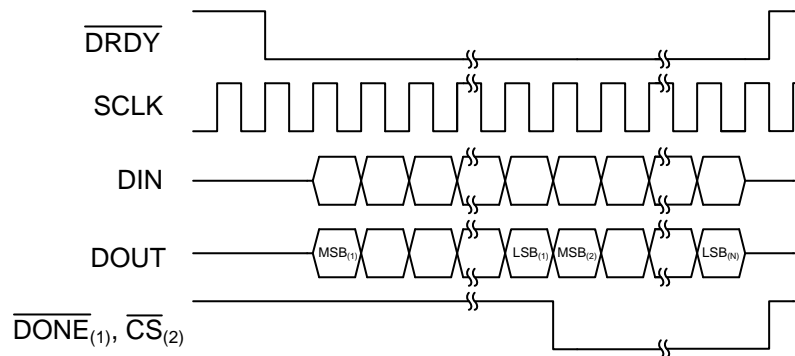


Figure 98. Multiple Device Configuration Using Synchronous Master Mode

**Application Information (continued)**


NOTE: <sub>(1)</sub> denotes device 1, <sub>(2)</sub> denotes device 2, and <sub>(N)</sub> denotes device N.

**Figure 99. Multiple Device Configuration Timing Diagram When Using Synchronous Master Mode**

**10.1.3.3 All Devices Configured in Synchronous Slave Mode**

Figure 100 illustrates a multiple device configuration where all devices are configured in synchronous slave mode. Figure 100 illustrates an external clock at the CLKIN pin, but a free-running SCLK can also be used as the conversion clock in this mode. SCLK must be free-running if the modulator clock is derived from the serial clock (CLKSRC = 1). See the [Synchronous Slave Mode](#) section for more information about clocking the device using SCLK. The  $\overline{DONE}$  pin of each device connects to the  $\overline{CS}$  pin of the subsequent device for communication. The DOUT pin of a device whose contents are already shifted out assumes a high-impedance state, allowing the DOUT pins of all devices to be tied together. To send commands to specific devices, send the respective command to the device when that device is selected for communication. In this configuration, conversions must be synchronized by the master. Synchronization is accomplished by tying the chip select or frame sync output of the host to the  $\overline{DRDY}$  input of each device. See the [Synchronous Slave Mode](#) section for more information about conversion synchronization using slave mode. Figure 101 illustrates an example interface timing diagram for this configuration.



Application Information (continued)

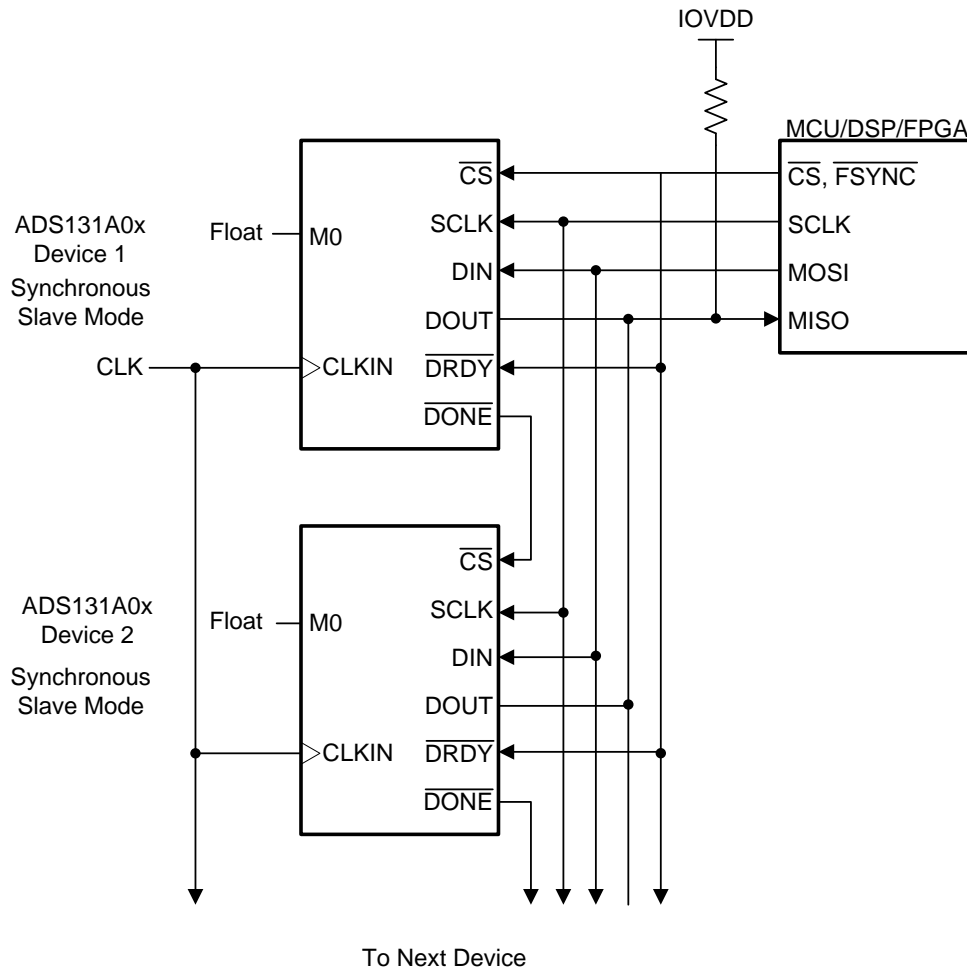
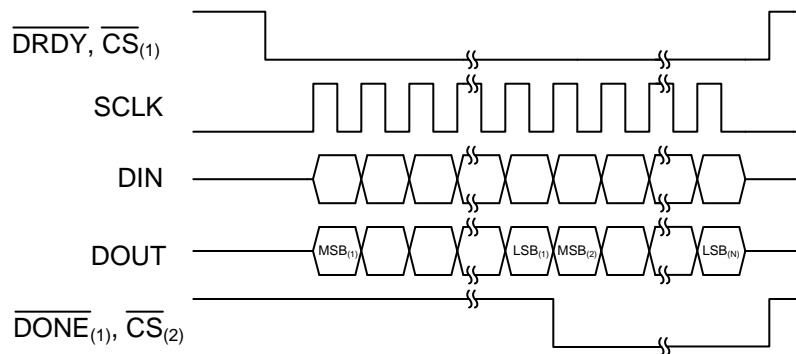


Figure 100. Multiple Device Configuration Using Synchronous Slave Mode



NOTE: <sub>(1)</sub> denotes device 1, <sub>(2)</sub> denotes device 2, and <sub>(N)</sub> denotes device N.

Figure 101. Multiple Device Configuration Timing Diagram When Using Synchronous Slave Mode

## 10.2 Typical Application

Figure 102 shows an ADS131A0x device used as part of a power-metering application. The ADS131A0x device is ideal because this device allows for simultaneous sampling of voltage and current. The upper channel is used to measure voltage, accomplished by stepping down the line voltage with a voltage divider. The lower channel measures current directly from the line by measuring voltage across the burden resistors  $R_4$ .

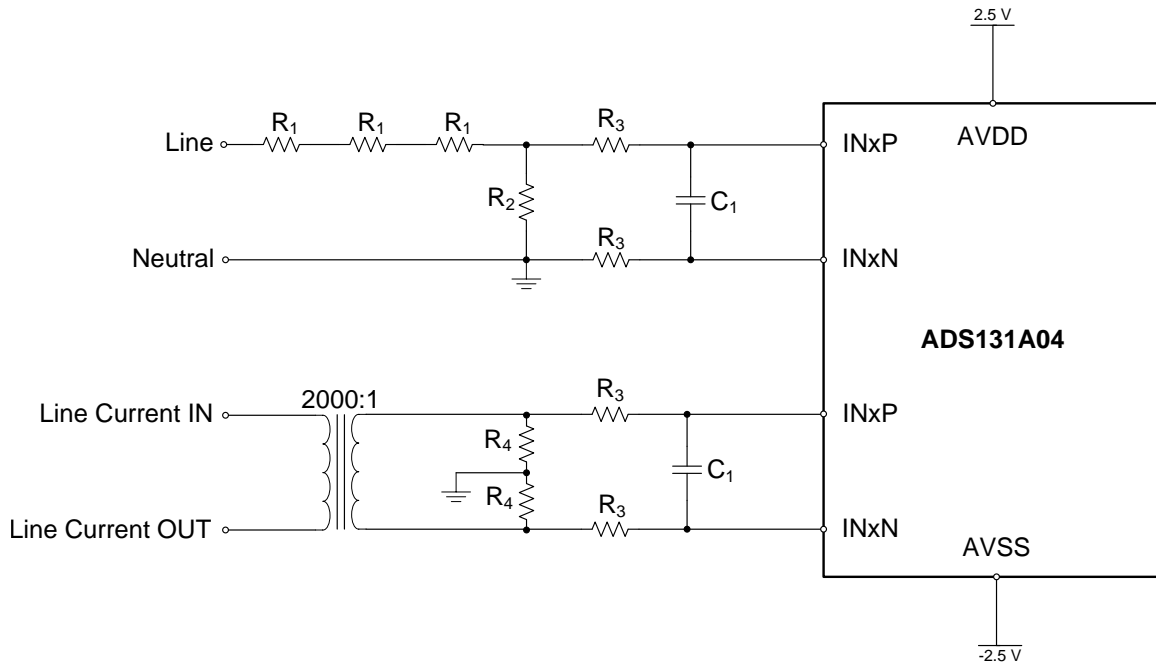


Figure 102. Typical Power Metering Connections

### 10.2.1 Design Requirements

Table 34. Power Metering Design Requirements

| DESIGN PARAMETER               | VALUE   |
|--------------------------------|---|
| Voltage input                  | 230 V <sub>RMS</sub> at 50 Hz                 |
| Current input range            | 0.05 A <sub>RMS</sub> to 100 A <sub>RMS</sub> |
| Active power measurement error | < 0.2%  |

### 10.2.2 Detailed Design Procedure

In this configuration, line voltage is measured as a single-ended input. The 230- $V_{RMS}$  signal must be stepped down such that the signal peaks fall within the measurement range of the ADS131A04 when using the internal 2.442-V reference. A voltage divider using the series combination of multiple  $R_1$  resistors and the  $R_2$  resistor steps the input to within an acceptable range. Using multiple  $R_1$  resistors along with proper spacing disperses energy among several components and provides a line of defense against short-circuits caused when one resistor fails. The output of this voltage divider can be calculated using [Equation 10](#):

$$V_{IN} = V_{LINE} \left( \frac{R_2}{3 \times R_1 + R_2} \right) \quad (10)$$

If  $R_1$  and  $R_2$  are chosen as 330 k $\Omega$  and 3.9 k $\Omega$ , respectively, the voltage at the input of the ADS131A0x is 0.9025  $V_{RMS}$ , corresponding to a 1.276  $V_{peak}$  that is within the measurement range of the ADC.

Line current is measured by stepping the input current down through a current transformer (CT) then shunting the current on the secondary side through burden resistors. Then, the voltage is measured across the resistors and current is back calculated in the processor. The voltage across the burden resistors  $R_4$  is measured differentially by grounding the node between the two resistors. [Equation 11](#) relates the voltage at the input to the ADS131A0x to the line current.

$$V_{IN} = \left( \frac{2 \times I_{LINE} \times R_4}{N} \right) \quad (11)$$

If a CT with a 2000:1 turns ratio is used and  $R_4$  is chosen to be 8.2  $\Omega$ , then 100  $A_{RMS}$  of line current corresponds to 0.82  $V_{RMS}$  (1.16  $V_{peak}$ ) at the input to the ADS131A0x. The design minimum line current of 50  $mA_{RMS}$  corresponds to 0.41  $mV_{RMS}$  (0.58  $mV_{peak}$ ).

The combination of  $R_3$  and  $C_1$  on each line serves as an antialiasing filter. Having  $C_1$  populated differentially between the inputs helps improve common-mode rejection because the tolerance of the capacitor is shared between the inputs. The half-power frequency of this filter can be calculated according to [Equation 12](#):

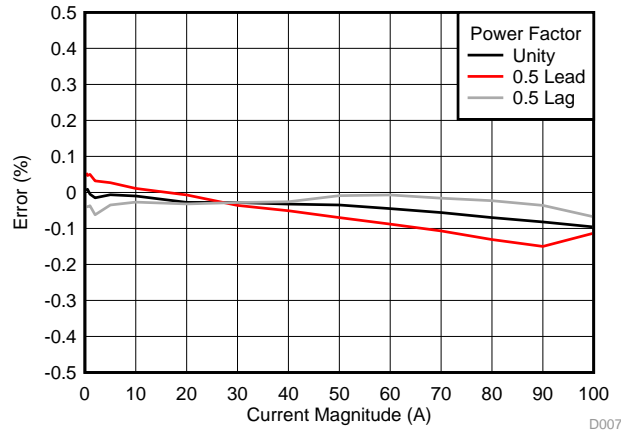
$$f_{-3dB} = \left( \frac{1}{4 \times \pi \times R_3 \times C_1} \right) \quad (12)$$

A filter with  $R_3$  populated as 100  $\Omega$  and  $C_1$  as 2.7 nF gives a cutoff frequency of approximately 295 kHz. This filter provides nearly 17 dB of attenuation at the modulator frequency when the ADS131A04 modulator frequency is set to 2.048 MHz.  $R_3$  must be kept relatively low because large series resistance degrades THD.

To get an accurate picture of instantaneous power, the phase delay of the current transformer must be taken into account. Many kinds of digital filters can be implemented in the application processor to delay the current measurement to better align with the input voltage.

### 10.2.3 Application Curve

Figure 103 shows the active power measurement accuracy for the ADS131A0x across varying currents. Data was taken for a 0.5 lead, 0.5 lag, and unity power factors. For this test, the external 16.384-MHz crystal frequency was divided to give a modulator frequency of 2.048 MHz. Finally, an OSR of 256 was chosen to give the ADS131A04 an output data rate of 8 kSPS.



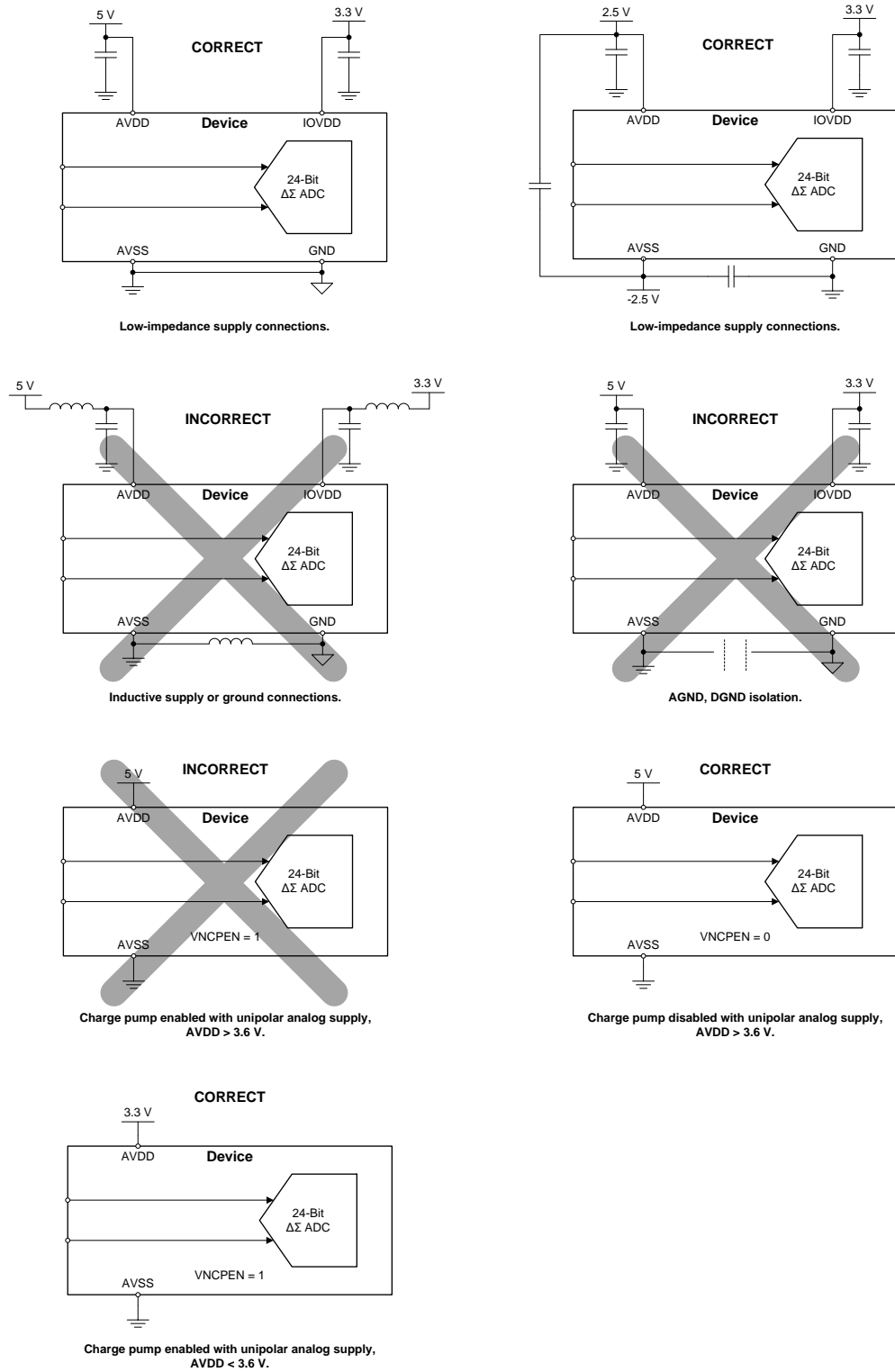
**Figure 103. Active Power Measurement Error**

### 10.3 Do's and Don'ts

- Do partition the analog, digital, and power-supply circuitry into separate sections on the printed circuit board (PCB).
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.
- Do verify that the analog input voltages are within the specified voltage range under all input conditions.
- Do tie unused analog input pins to GND.
- Do provide current limiting to the analog inputs in case overvoltage faults occur.
- Do use a low-dropout (LDO) regulator to reduce ripple voltage generated by switch-mode power supplies. This reduction is especially true for AVDD where the supply noise can affect performance.
- Do keep the input series resistance low to maximize THD performance.
- Do not cross analog and digital signals.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 3.6 V under any conditions, including during power-up and power-down when the negative charge pump is enabled.
- Do not allow the analog power supply voltages (AVDD – AVSS) to exceed 6 V under any conditions, including during power-up and power-down when the negative charge pump is disabled.
- Do not allow the digital supply voltage to exceed 3.9 V under any conditions, including during power-up and power-down.

Figure 104 and Figure 105 illustrate correct and incorrect ADC circuit connections.

**Do's and Don'ts (continued)**



**Figure 104. Correct and Incorrect Circuit Connections**

Do's and Don'ts (continued)

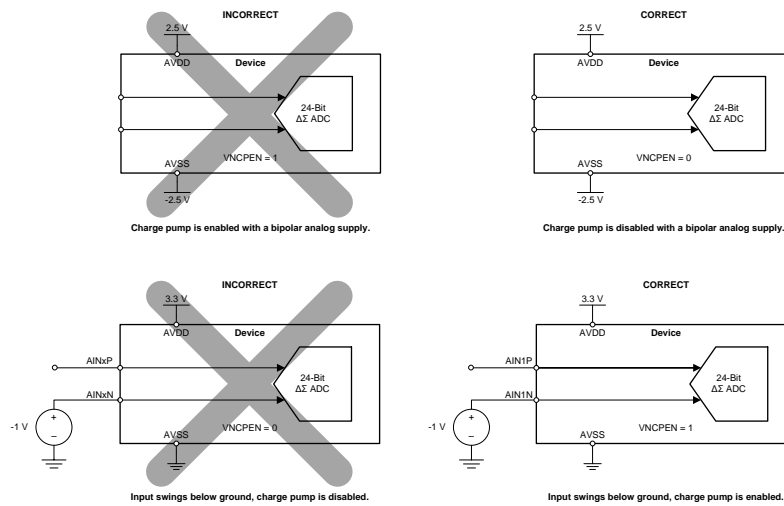
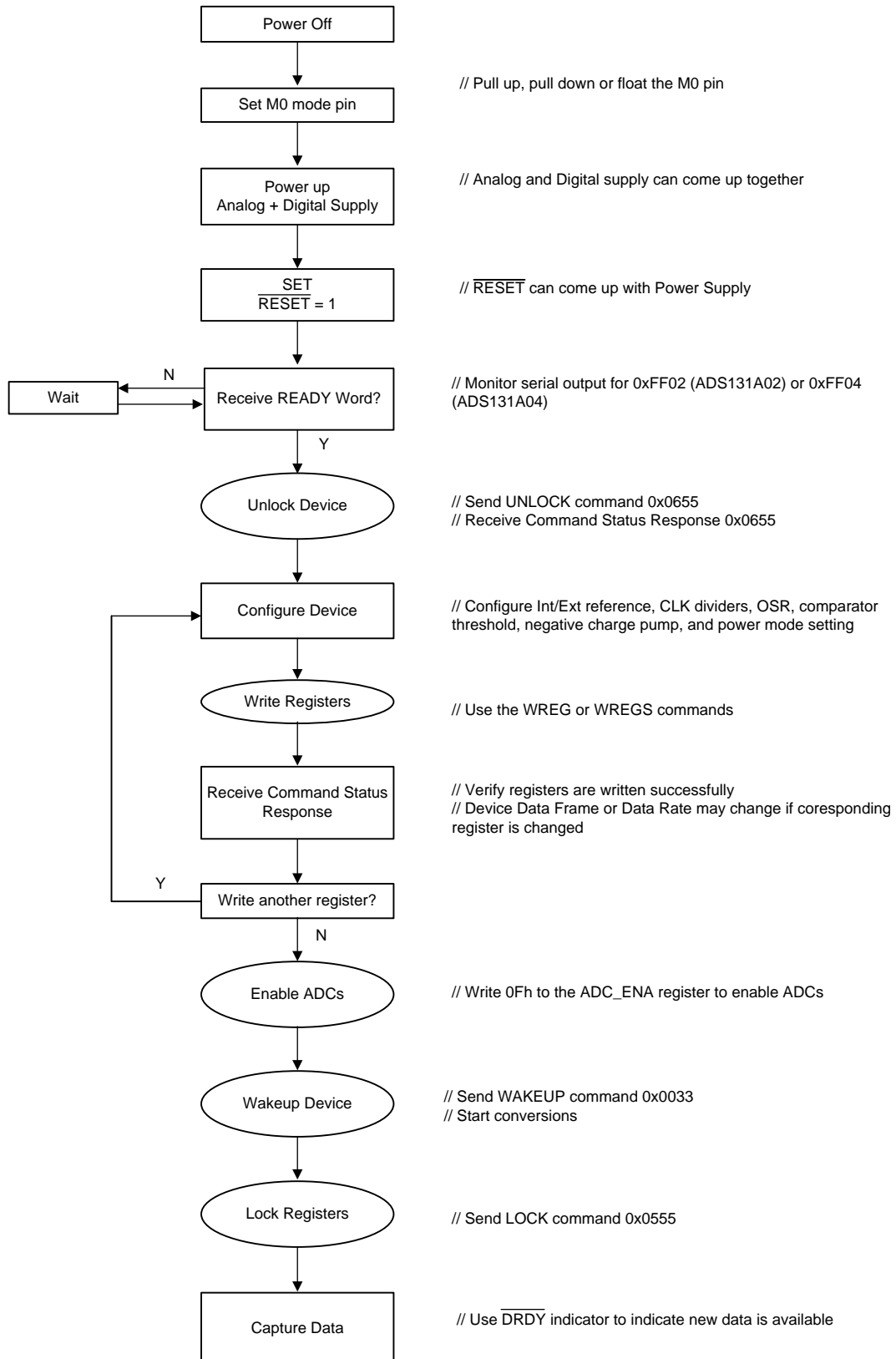


Figure 105. Correct and Incorrect Circuit Connections, Continued

10.4 Initialization Set Up

Figure 106 illustrates a general procedure to configure the ADS131A0x to collect data.

**Initialization Set Up (continued)**



**Figure 106. ADS131A0x Configuration Sequence**

## 11 Power Supply Recommendations

The device requires two power supplies: analog (AVDD, AVSS) and digital (IOVDD, GND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V), unipolar (for example, AVDD = 5 V, AVSS = 0 V), or unipolar using the negative charge pump (for example, AVDD = 3.3 V, AVSS = VNCP), and is independent of the digital power supply. The digital supply range sets the digital I/O levels.

### 11.1 Negative Charge Pump

An optional negative charge pump is available to power AVSS with an operating voltage of –1.95 V. Enabling the negative charge pump allows for input signals below analog ground when using a unipolar analog supply (for example, AVDD = 3.3 V, AVSS = 0 V). The VNCPEN bit in the [A\\_SYS\\_CFG register](#) must be set high by the user to enable the negative charge pump. The VNCP pin outputs the nominal –1.95-V negative charge pump output and requires a capacitor to AVSS in the range of 220 pF to 470 pF. The charge pump operates at a switching frequency of  $2f_{MOD}$ . The minimum ADC absolute input voltage range is –1.5 V with the negative charge pump enabled. The maximum analog supply limit (AVDD – AVSS) is restricted to 3.6 V maximum. Exceeding this limit can permanently damage the device.

The negative charge pump is internally activated when the VNCPEN bit is set to 1 and the device is in wake-up mode with all ADC channels enabled (ADC\_ENA = 0Fh).

Connect VNCP directly to AVSS when not using the negative charge pump.

### 11.2 Internal Digital LDO

The ADS131A0x digital core voltage operates from 1.8 V, created from an internal LDO from IOVDD. The CAP pin outputs the LDO voltage created from the IOVDD supply and requires an external bypass capacitor. When operating from  $V_{IOVDD} > 2$  V, place a 1- $\mu$ F capacitor on the CAP pin to GND. If  $V_{IOVDD} \leq 2$  V, tie the CAP pin directly to the IOVDD pin and decouple both pins using a 1- $\mu$ F capacitor to GND.

### 11.3 Power-Supply Sequencing

The power supplies can be sequenced in any order but the analog or digital inputs must never exceed the respective analog or digital power-supply voltage limits.



### 11.4 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD, AVSS (when using a bipolar supply), and IOVDD must be decoupled with at least a 1- $\mu$ F capacitor, as shown in Figure 107, Figure 108, and Figure 109. A 270-nF capacitor is required on the VNCP pin when using the negative charge pump. Place the bypass capacitors as close to the power-supply pins of the device as possible with low-impedance connections. Using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics are recommended for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. The analog and digital ground are recommended to be connected together as close to the device as possible.

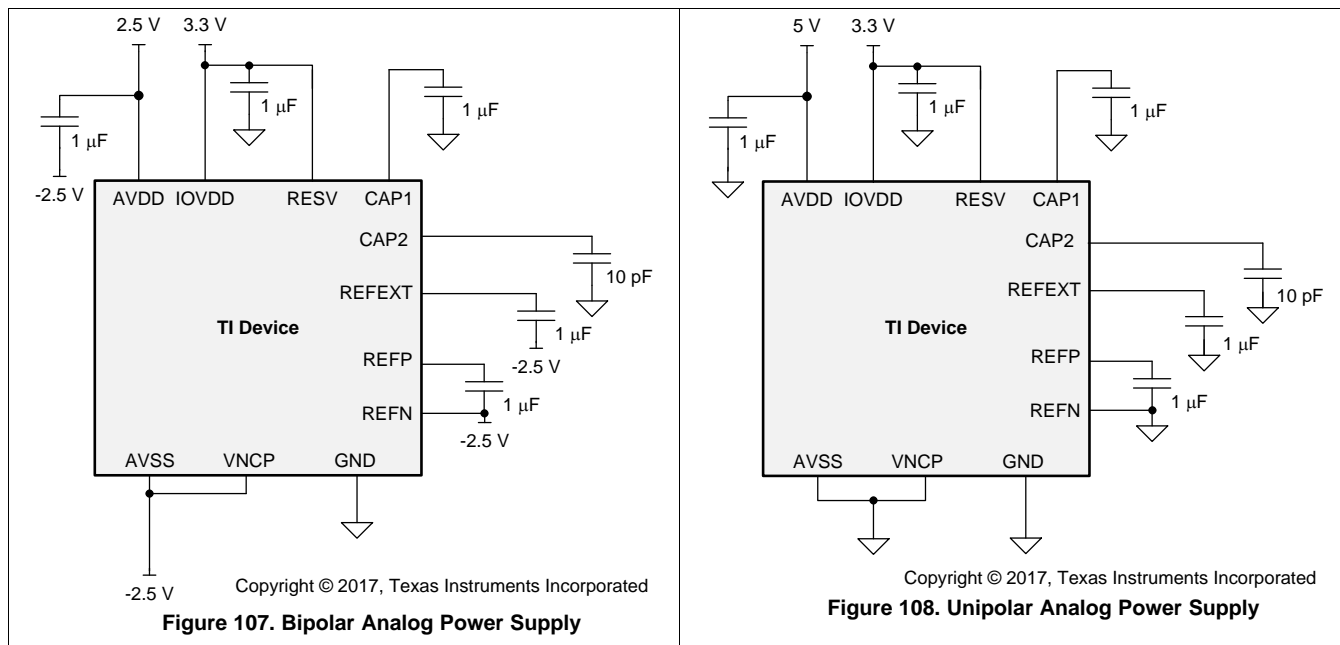


Figure 107. Bipolar Analog Power Supply

Figure 108. Unipolar Analog Power Supply

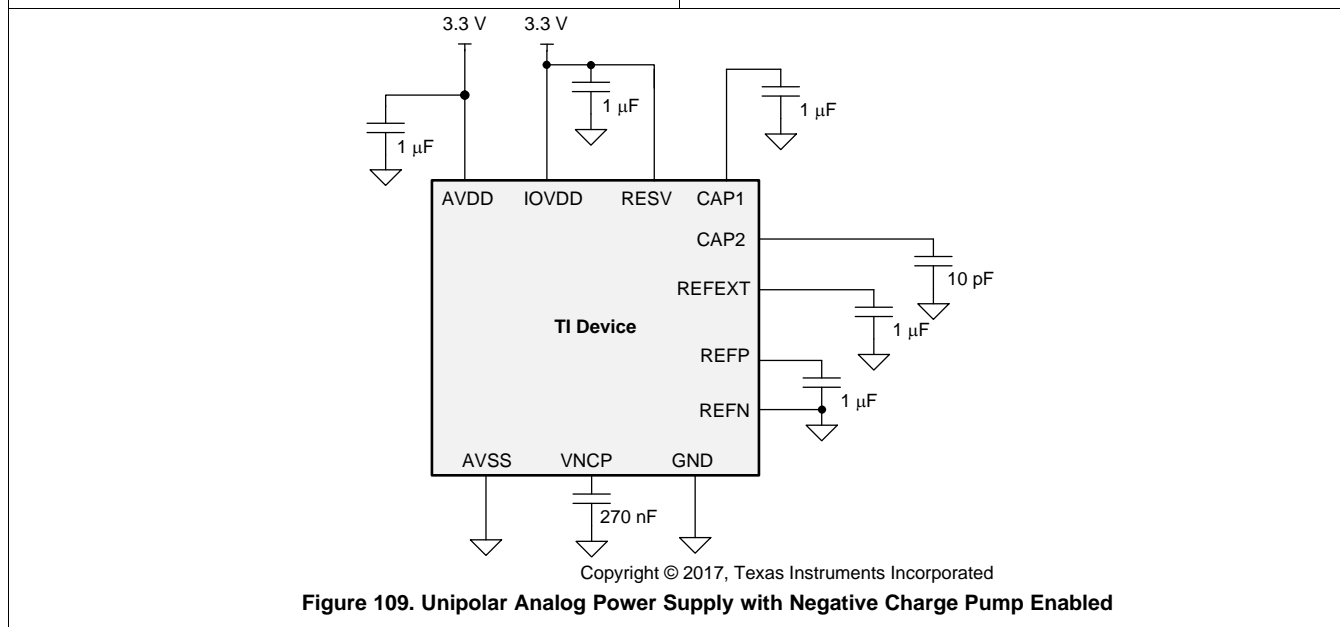


Figure 109. Unipolar Analog Power Supply with Negative Charge Pump Enabled

## 12 Layout

### 12.1 Layout Guidelines

Use a low-impedance connection for ground so that return currents flow undisturbed back to the respective sources. For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. Keep connections to the ground plane as short and direct as possible. When using vias to connect to the ground layer, use multiple vias in parallel to reduce impedance to ground. Figure 110 shows the proper component placement for the system.

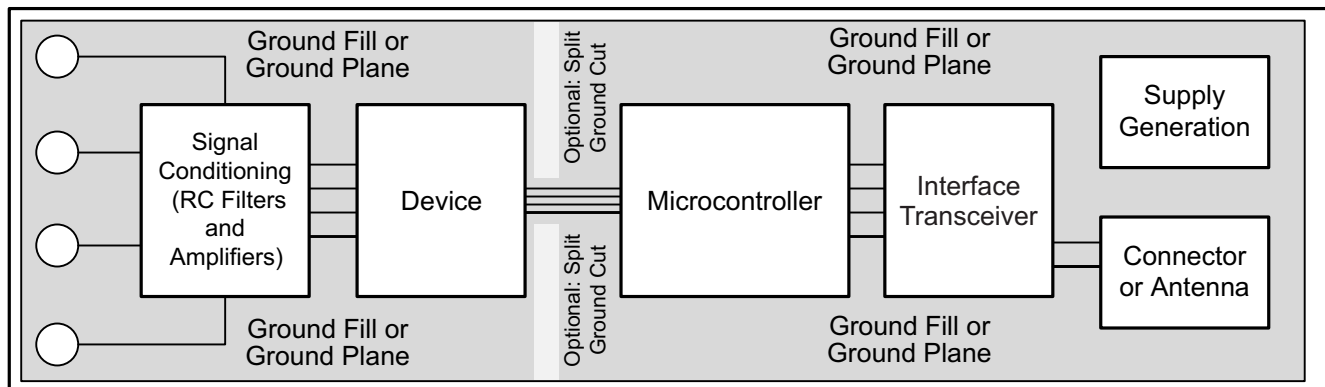
A mixed-signal layout sometimes incorporates separate analog and digital ground planes that are tied together at one location; however, separating the ground planes is not necessary when analog, digital, and power-supply components are properly placed. Proper placement of components partitions the analog, digital, and power-supply circuitry into different PCB regions to prevent digital return currents from coupling into sensitive analog circuitry. If ground plane separation is necessary, then make the connection at the ADC. Connecting individual ground planes at multiple locations creates ground loops, and is not recommended. A single ground plane for the analog and digital grounds avoids ground loops.

Bypass the supply pins with a low-ESR ceramic capacitor. The placement of the bypass capacitors must be as close as possible to the supply pins using short, direct traces. For optimum performance, the ground-side connections of the bypass capacitors must also be made with low-impedance connections. The supply current flows through the bypass capacitor pin first and then to the supply pin to make the bypassing most effective (also known as a Kelvin connection). If multiple ADCs are on the same PCB, use wide power-supply traces or dedicated power-supply planes to minimize the potential of crosstalk between ADCs.

If external filtering is used for the analog inputs, use C0G-type ceramic capacitors when possible. C0G capacitors have stable properties and low-noise characteristics. Ideally, route differential signals as pairs to minimize the loop area between the traces. Route digital circuit traces (such as clock signals) away from all analog pins. Note that the internal reference output return shares the same pin as the AVSS power supply. To minimize coupling between the power-supply trace and reference return trace, route the two traces separately; ideally, as a star connection at the AVSS pin.

Treat the AVSS pin as a sensitive analog signal and connect directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the ADS131A0x if shielding is not implemented. Keep digital signals as far as possible from the analog input signals on the PCB.

The SCLK input of the serial interface must be free from noise and glitches when this device is configured in a slave mode. This configuration is especially true when SCLK is used as the master clock for this device. Even with relatively slow SCLK frequencies, short digital signal rise and fall times can cause excessive ringing and noise. For best performance, keep the digital signal traces short, using termination resistors as needed, and make sure all digital signals are routed directly above the ground plane with minimal use of vias.



**Figure 110. System Component Placement**

## 12.2 Layout Example

Figure 111 is an example layout of the ADS131A0x. This example shows the device supplied with a bipolar supply, though the layout can be replicated for a unipolar case. In general, analog signals and planes are partitioned to the left and digital signals and planes to the right.

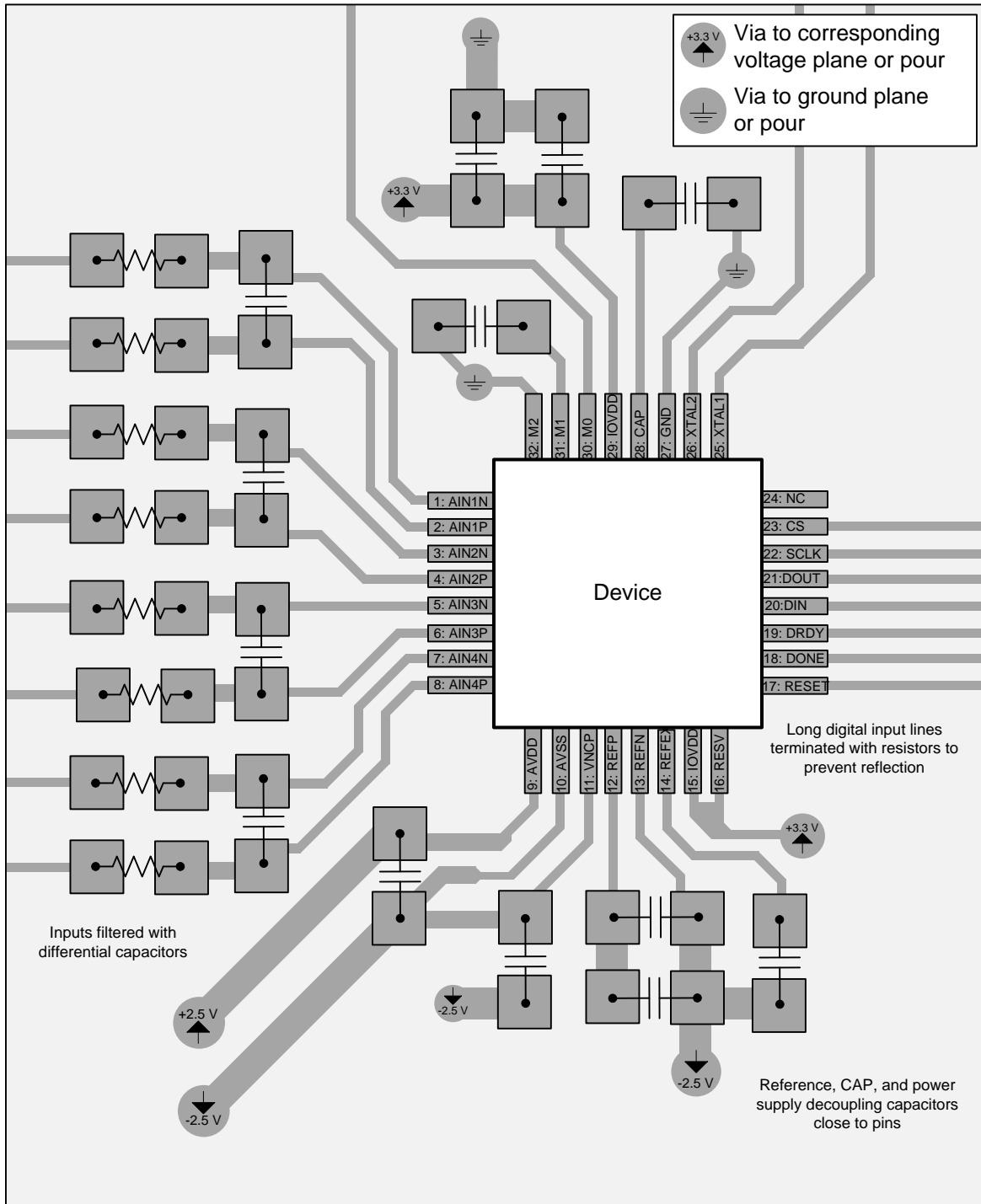


Figure 111. ADS131A0x Layout Example

## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

请参阅如下相关文档：

- 《REF50xx 低噪声、极低漂移、高精度电压基准》（文献编号：SBOS410）
- 《THS4531A 超低功耗、轨到轨输出、全差分放大器》（文献编号：SLOS823）
- 《REF60xx 集成 ADC 驱动器缓冲器的高精度电压基准》（文献编号：SBOS708）

### 13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 35. 相关链接

| 器件        | 产品文件夹                 | 立即订购                  | 技术文档                  | 工具和软件                 | 支持和社区                 |
|-----------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| ADS131A02 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| ADS131A04 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |

### 13.3 接收文档更新通知

如需接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 13.5 商标

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| ADS131A02IPBS    | ACTIVE        | TQFP         | PBS             | 32   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 131A02                  | <a href="#">Samples</a> |
| ADS131A02IPBSR   | ACTIVE        | TQFP         | PBS             | 32   | 1000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 131A02                  | <a href="#">Samples</a> |
| ADS131A04IPBS    | ACTIVE        | TQFP         | PBS             | 32   | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 131A04                  | <a href="#">Samples</a> |
| ADS131A04IPBSR   | ACTIVE        | TQFP         | PBS             | 32   | 1000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | 131A04                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

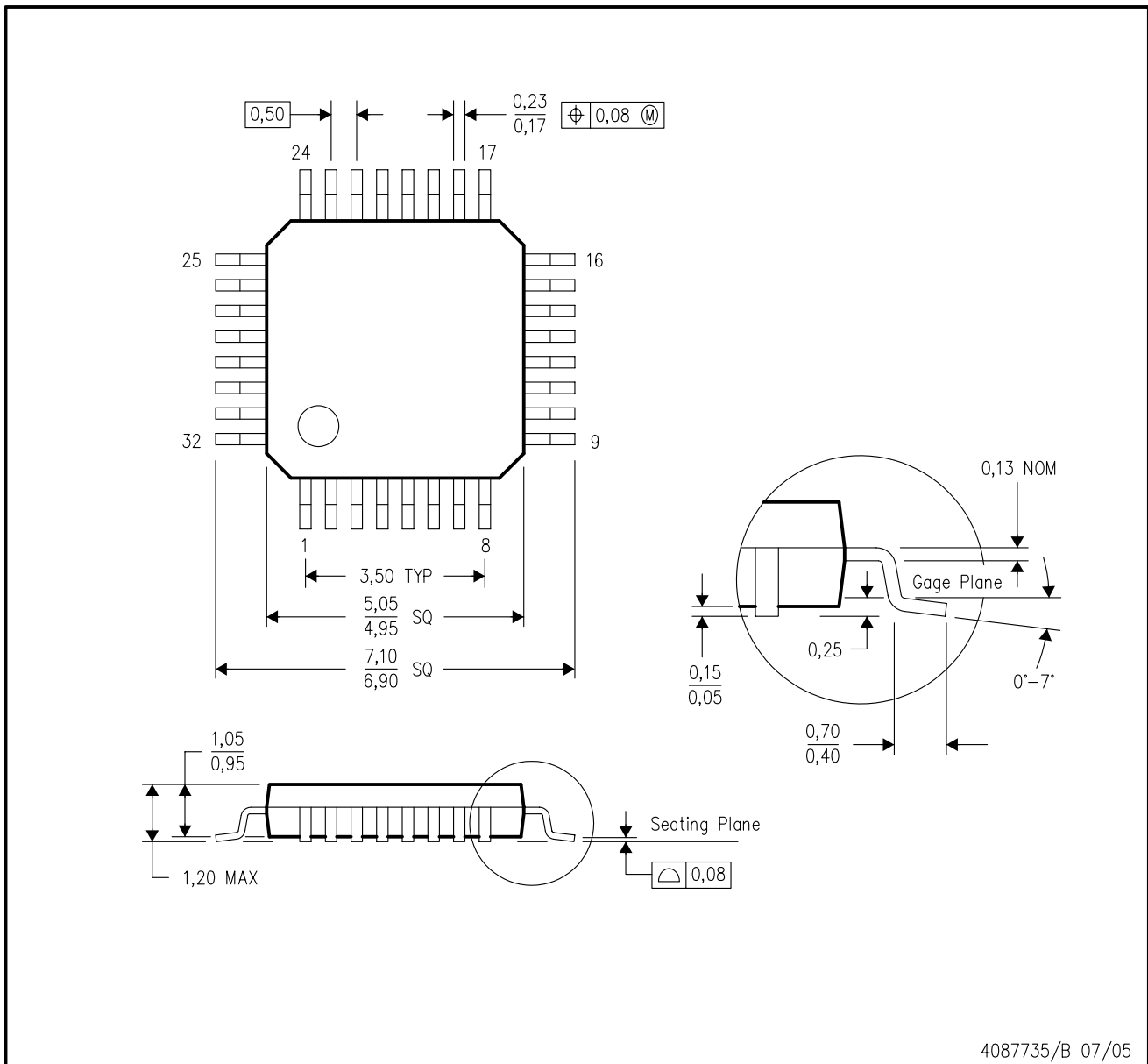
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PBS (S-PQFP-G32)

PLASTIC QUAD FLATPACK

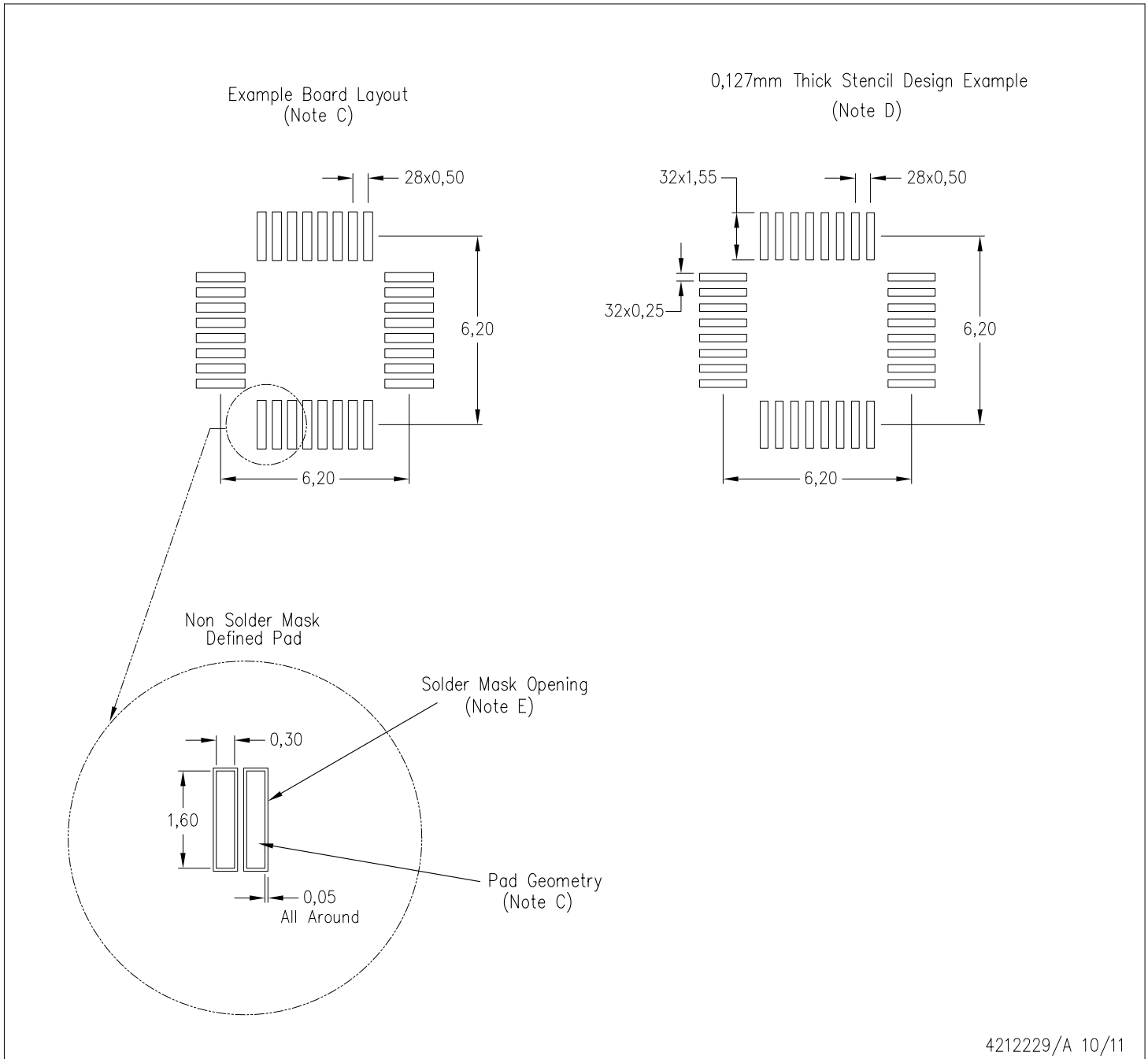


4087735/B 07/05

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.

PBS (S-PQFP-G32)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.



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