1、General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 4K words of EPROM, and 176 bytes of static RAM.

2、Features

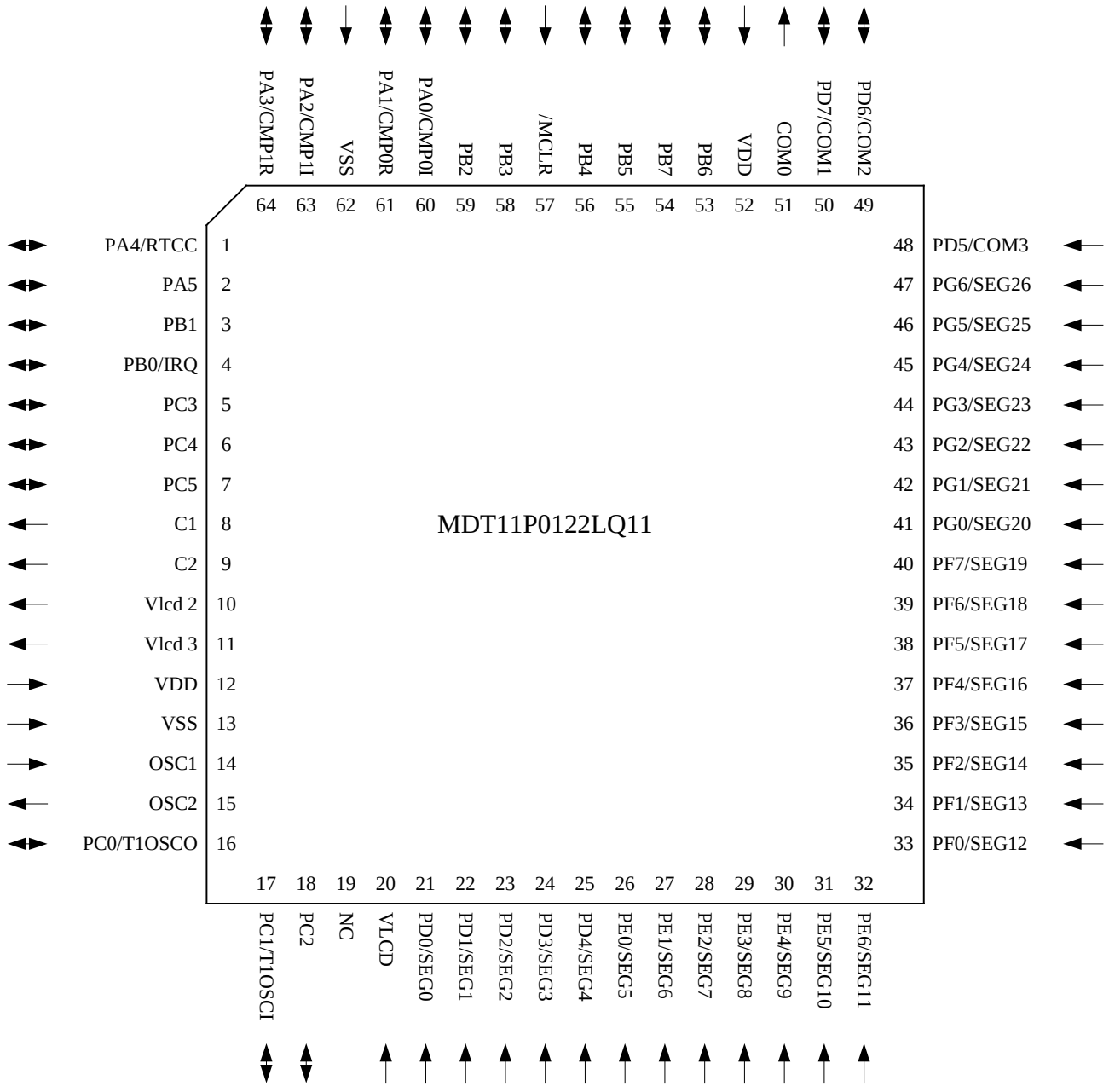
- RISC CPU
- Fully static design
- 37 single word instructions
- 4K x 14 program memory.
- 176 bytes RAM for data
- 25 bi-directional I/O
- Eight level hardware stacks
- Watchdog timer with on-chip RC oscillator.
- Interrupt capability
- Timer0 : 8-bit timer with 8-bit prescaler
- Timer1 : 16-bit timer
- 16-bit Timer1 compare register.
- Sleep mode for power saving.
- PB with port change wake-up interrupt.
- LCD：29 Segments,4 commons.(27 x 4 at LQFP Package)
- 1/2,1/3,1/4 multiplex at 1/3,1/2 bias.
- 2 channel comparator

3. Applications

The application areas of this MDT11P0122 range from appliance motor control and high speed automotive to low power remote transmitters/receivers and tele-communications processors, such as Remote controller, small instruments, toy, automobile and keyboard … etc.

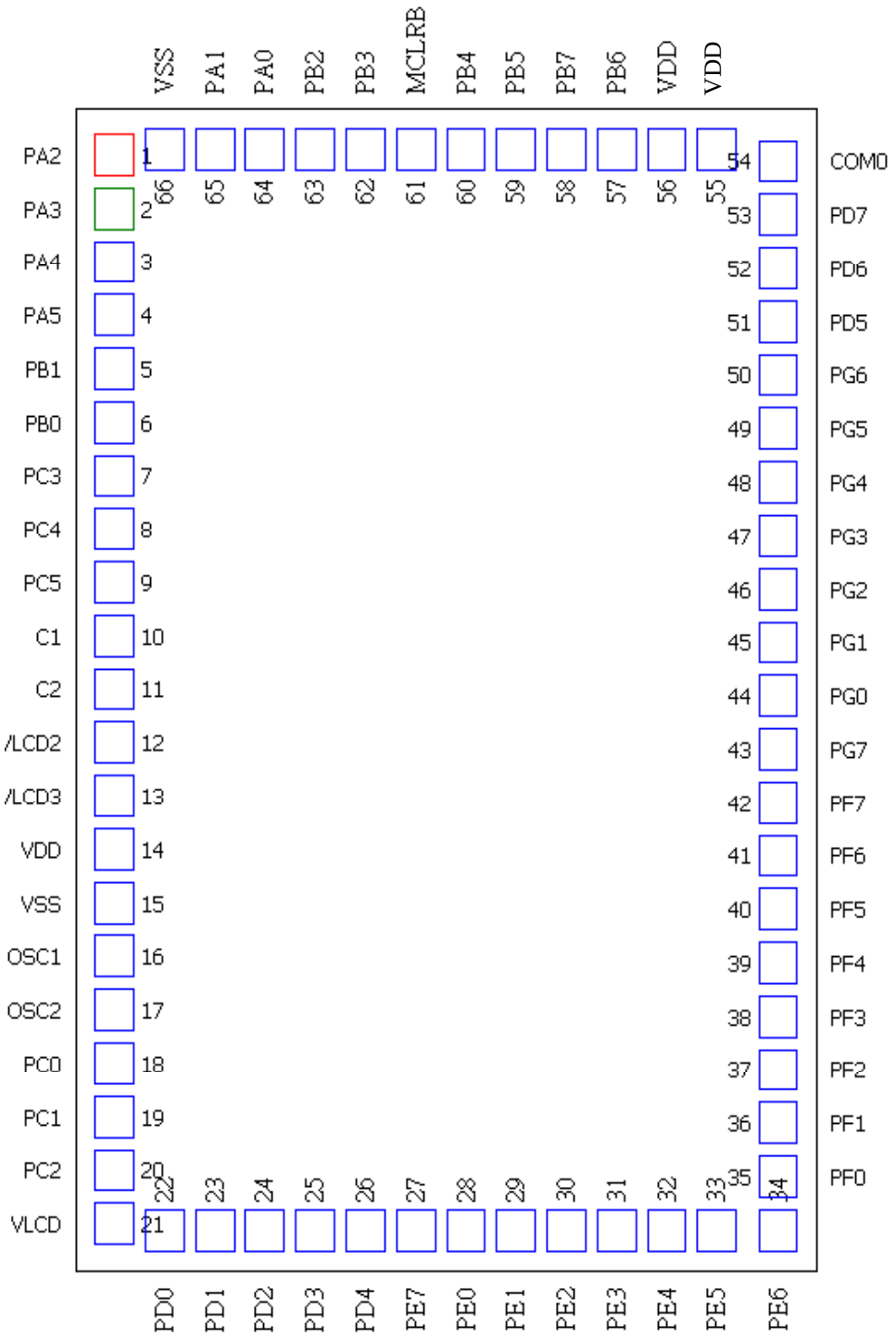
4. IC Diagram

(1)Pin Diagram



Device	LCD dot	Package	Remark
MDT11P0122LQ11	4 X 27	64 PIN LQFP	
MDT11P0122	4 X 29	COB	

(2)pad diagram



IC substrate connect to VSS

VDD (pad 14,55,56), VSS (pad 15, 66) must to be connect

(3)pad Coordinates

PAD-No	PAD Name	X	Y	PAD-No	PAD Name	X	Y
1	PA2	79.2	2091.4	34	PE6	1400.8	79.2
2	PA3	79.2	1991.4	35	PF0	1400.8	179.2
3	PA4	79.2	1891.4	36	PF1	1400.8	279.2
4	PA5	79.2	1791.4	37	PF2	1400.8	379.2
5	PB1	79.2	1691.4	38	PF3	1400.8	479.2
6	PB0	79.2	1591.4	39	PF4	1400.8	579.2
7	PC3	79.2	1491.4	40	PF5	1400.8	679.2
8	PC4	79.2	1391.4	41	PF6	1400.8	779.2
9	PC5	79.2	1291.4	42	PF7	1400.8	879.2
10	C1	79.2	1191.4	43	PG7	1400.8	979.2
11	C2	79.2	1091.4	44	PG0	1400.8	1079.2
12	VLCD2	79.2	991.4	45	PG1	1400.8	1179.2
13	VLCD3	79.2	891.4	46	PG2	1400.8	1279.2
14	VDD	79.2	791.4	47	PG3	1400.8	1379.2
15	VSS	79.2	691.4	48	PG4	1400.8	1479.2
16	OSC1	79.2	591.4	49	PG5	1400.8	1579.2
17	OSC2	79.2	491.4	50	PG6	1400.8	1679.2
18	PC0	79.2	391.4	51	PD5	1400.8	1779.2
19	PC1	79.2	291.4	52	PD6	1400.8	1879.2
20	PC2	79.2	191.4	53	PD7	1400.8	1979.2
21	VLCD	79.2	91.4	54	COM0	1400.8	2079.2
22	PD0	179.2	79.2	55	VDD	1279.2	2100.8
23	PD1	279.2	79.2	56	VDD	1179.2	2100.8
24	PD2	379.2	79.2	57	PB6	1079.2	2100.8
25	PD3	479.2	79.2	58	PB7	979.2	2100.8
26	PD4	579.2	79.2	59	PB5	879.2	2100.8
27	PE7	679.2	79.2	60	PB4	779.2	2100.8
28	PE0	779.2	79.2	61	MCLRB	679.2	2100.8
29	PE1	879.2	79.2	62	PB3	579.2	2100.8
30	PE2	979.2	79.2	63	PB2	479.2	2100.8
31	PE3	1079.2	79.2	64	PA0	379.2	2100.8
32	PE4	1179.2	79.2	65	PA1	279.2	2100.8
33	PE5	1279.2	79.2	66	VSS	179.2	2100.8

5. Pin function description

Pin name	Type	Buffer type	Description	
OSC1	I		Oscillator input	
OSC2	O		Oscillator out	
/MCLR	I	ST	Reset input	
PA0/CMP0I	I/O	TTL	Bi-directional I/O port A. Port A can be software programmed for internal 50KΩ pull-up	PA0 can use TTL level I/O or Comparator input.
PA1/CMP0R	I/O	TTL		PA1 can use TTL level I/O or Comparator input.
PA2/CMP1I	I/O	TTL		PA2 can use TTL level I/O or Comparator input.
PA3/CMP1R	I/O	TTL		PA3 can use TTL level I/O or Comparator input.
PA4/RTCC	I/O	ST		PA4 can be clock input to Timer0.
PA5	I/O	TTL		Bi-directional I/O port
PB0/IRQ	I/O	ST/TTL	Bi-directional I/O port B. Port B can be software programmed for internal 50KΩ pull-up on all pins. PB0-PB7 can generate interrupt on pin state change.	PB0/IRQ can be the external interrupt pin.
PB1	I/O	TTL		PB1 can generate interrupt on pin change.
PB2	I/O	TTL		PB2 can generate interrupt on pin change.
PB3	I/O	TTL		PB3 can generate interrupt on pin change.
PB4	I/O	TTL		PB4 can generate interrupt on pin change.
PB5	I/O	TTL		PB5 can generate interrupt on pin change.
PB6	I/O	TTL		PB6 can generate interrupt on pin change.
PB7	I/O	TTL		PB7 can generate interrupt on pin change.
PC0/T1OSCO	I/O	ST	Bi-directional I/O port C. Port C can be software programmed for internal 100K Ω pull-up on all pins.	PC0 can be Timer1 oscillator output or Timer1 clock input.
PC1/T1OSCI	I/O	ST		PC1 can be Timer1 oscillator input.
PC2/CCP1	I/O	ST		PC2 can be Timer1 compare output.
PC3	I/O	ST		Bi-directional I/O port
PC4	I/O	ST		Bi-directional I/O port
PC5	I/O	ST		Bi-directional I/O port
PD0/SEG00	I/O/L	ST	Bi-directional I/O/LCD Driver port	PD0 are open drain I/O or LCD Segment driver
PD1/SEG01	I/O/L	ST		PD1 are open drain I/O or LCD Segment driver
PD2/SEG02	I/O/L	ST		PD2 are open drain I/O or LCD Segment driver
PD3/SEG03	I/O/L	ST		PD3 are open drain I/O or LCD Segment driver
PD4/SEG04	I/O/L	ST		PD4 are open drain I/O or LCD Segment driver
PD5/COM3	I/L	ST	Digital input or LCD Common Driver port	PD5 are digital input or LCD Common driver
PD6/COM2	I/L	ST		PD6 are digital input or LCD Common driver
PD7/COM1	I/L	ST		PD7 are digital input or LCD Common driver

Pin name	Type	Buffer type	Description
PE0/SEG05	I/L	ST	Digital input or LCD Segment Driver port
PE1/SEG06	I/L	ST	
PE2/SEG07	I/L	ST	
PE3/SEG08	I/L	ST	
PE4/SEG09	I/L	ST	
PE5/SEG10	I/L	ST	
PE6/SEG11	I/L	ST	
PE7/SEG27	I/L	ST	
PF0/SEG12	I/L	ST	
PF1/SEG13	I/L	ST	
PF2/SEG14	I/L	ST	
PF3/SEG15	I/L	ST	
PF4/SEG16	I/L	ST	
PF5/SEG17	I/L	ST	
PF6/SEG18	I/L	ST	
PF7/SEG19	I/L	ST	
PG0/SEG20	I/L	ST	
PG1/SEG21	I/L	ST	
PG2/SEG22	I/L	ST	
PG3/SEG23	I/L	ST	
PG4/SEG24	I/L	ST	
PG5/SEG25	I/L	ST	
PG6/SEG26	I/L	ST	
PG7/SEG28	I/L	ST	
COM0	L	-	LCD Common 0
C1	-	-	LCD voltage charge pump pin 1
C2	-	-	LCD voltage charge pump pin 2
VLCD	-	-	LCD voltage input pin
VLCD2	-	-	LCD voltage pin(1/2VDD)
VLCD3	-	-	LCD voltage pin (3/2VDD)
VDD	-	-	Power input
Vss	-	-	Ground pin

**note : I:input O:output L:lcd

6 Memory Mapping

6.1 Program memory :

0000h	Reset Vector
0001h	
0002h	
0003h	
0004h	Peripheral interrupt Vector
0005h 07FFh	Program memory (Page 0)
0800h 0FFFh	Program memory (Page 1)

6.2 Register file map

	BANK 0	BANK 1	
00h	I. ADDR	I. ADDR	80h
01h	RTCC	TMR	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	MSR	MSR	84h
05h	Port A	CPIO A	85h
06h	Port B	CPIO B	86h
07h	Port C	CPIO C	87h
08h	Port D	CPIO D	88h
09h	Port E	CPIO E	89h
0Ah	PCHLAT	PCHLAT	8Ah
0Bh	INTS	INTS	8Bh
0Ch	PIFB1	PIEB1	8Ch
0Dh			8Dh
0Eh	TMR1L	PSTA	8Eh
0Fh	TMR1H		8Fh
10h	T1STA	CMPPH	90h
11h			91h
12h			92h
13h			93h
14h			94h
15h	CCP1L		95h
16h	CCP1H		96h
17h	CCPCTL		97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh			9Eh
1Fh			9Fh
20h 6Fh	General Purpose Register	General Purpose Register	A0h EFh
70h 7Fh		Access 70h~7Fh	F0h FFh

	BANK 2	BANK 3	
100h	I. ADDR	I. ADDR	180h
101h	RTCC	TMR	181h
102h	PCL	PCL	182h
103h	STATUS	STATUS	183h
104h	MSR	MSR	184h
105h			185h
106h	Port B	CPIO B	186h
107h	Port F	CPIO F	187h
108h	Port G	CPIO G	188h
109h			189h
10Ah	PCHLAT	PCHLAT	18Ah
10Bh	INTS	INTS	18Bh
10Ch			18Ch
10Dh	LCDPFS		18Dh
10Eh	LCDFS		18Eh
10Fh	LCDCTL		18Fh
110h	LCD00		190h
111h	LCD01		191h
112h	LCD02		192h
113h	LCD03		193h
114h	LCD04		194h
115h	LCD05		195h
116h	LCD06		196h
117h	LCD07		197h
118h	LCD08		198h
119h	LCD09		199h
11Ah	LCD10		19Ah
11Bh	LCD11		19Bh
11Ch	LCD12		19Ch
11Dh	LCD13		19Dh
11Eh	LCD14		19Eh
11Fh	LCD15		19Fh
120h 16Fh			1A0h 1EFh
170h 17Fh	Access 70h~7Fh	Access 70h~7Fh	1F0h 1FFh

Unimplemented memory location.

MDT11P0121 REGISTER FILE SUMMARY

Address	NAME	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BANK0									
00	**IAR**	Addressing this location uses the content of MSR to address data memory (not a physical register)							
01	**RTCC**	8 Bit Real time clock / counter							
02	**PCL**	Low order 8 bit of PC							
03	**STATUS**	RBS2	RBS1	RBS0	/TF	/PF	Z	HC	C
04	**MSR**	Indirect Address pointer							
05	**PORT A**	-	-	PA5	PA4	PA3	PA2	PA1	PA0
06	**PORT B**	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
07	**PORT C**	-	-	PC5	PC4	PC3	PC2	PC1	PC0
08	**PORT D**	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
09	**PORT E**	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
0A	**PCHLAT**	Unimplemented, reads as'0'			Write buffer for high byte of PC				
0B	**INTS**	GIS	PEIE	TIS	INTS	RBIE	TIF	INTF	RBIF
0C	**PIFB1**	LCDIF	-	-	-	-	-	-	TMR1IF
0E	**TMR1L**	Timer 1 Least Significant Byte							
0F	**TMR1H**	Timer 1 Most Significant Byte							
10	**T1STA**	-	-	T1CKPS1	T1CKPS0	T1OSCEN	/T1SYNC	TMR1CLK	TMR1ON
15	**CCP1L**	CCP 1 Least Significant Byte							
16	**CCP1H**	CCP 2 Most Significant Byte							
17	**CCP1CTL**	-	-	-	-	-	-	-	CCP1M0
BANK1									
80	**IAR**	Addressing this location uses the content of MSR to address data memory (not a physical register)							
81	**TMR**	PBPH	IES	TCS	TCE	PSC	PS2	PS1	PS0
82	**PCL**	Low order 8 bit of PC							
83	**STATUS**	RBS2	RBS1	RBS0	/TF	/PF	Z	HC	C
84	**MSR**	Indirect Address pointer							
85	**CPIO A**	-	-	PORT A DATA DIRECTION REGISTER					
86	**CPIO B**	PORT B DATA DIRECTION REGISTER							
87	**CPIO C**	-	-	PORT C DATA DIRECTION REGISTER					
88	**CPIO D**	PORT D DATA DIRECTION REGISTER							
89	**CPIO E**	PORT E DATA DIRECTION REGISTER							
8A	**PCHLAT**	Unimplemented, reads as'0'			Write buffer for high byte of PC				
8B	**INTS**	GIS	PEIE	TIS	INTS	RBIE	TIF	INTF	RBIF
8C	**PIEB1**	LCDIE	-	-	-	-	-	-	TMR1IE
8E	**PSTA**	-	-	-	-	-	-	PORB	-
90	**CMPPH**	-	-	PCHR	PAHR	CMPRS1	CMPRS0	CMPS1	CMPS0
BANK2									
107	**PORT F**	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
108	**PORT G**	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
10D	**LCDPFS**	DL29	DL27	DL20	DL16	DL12	DL09	DL05	DL00
10E	**LCDFS**	-	-	-	-	FS3	FS2	FS1	FS0
10F	**LCDCTL**	LCDE	SLPE	BIASS	CRS	CLKS1	CLKS0	LCDS1	LCDS0
110~11F	**LCD00 ~ LCD15**	LCD data register 00~15							
BANK3									
187	**CPIO F**	PORT F DATA DIRECTION REGISTER							
188	**CPIO G**	PORT G DATA DIRECTION REGISTER							

- **BANK 1**

R00 IAR(Indirect addressing register)

R01 RTCC (Real Time Counter/Counter Register)

Timer0 register

R02 PCL (Program Counter Low Byte)

Low order 8 bits of the Program Counter (PC)

R03 STATUS (Status register)

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PF	Power loss Flag bit
4	TO	WDT TIME OUT bit
5	RBS0	Register page select bit 0 0： 00/H --- 7F/H 0 1： 80/H --- FF/H 1 0：100/H --- 17F/H 1 1：180/H --- 1FF/H
6	RBS1	
7	RBS2	Register page select bit 0： 00/H--- FF/H 1：100/H---1FF/H

R04H : MSR (Memory Select Register)

Indirect data memory address pointer.

R05H : Port A

PortA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
	-	-	Always available					

PA0~PA5：portA I/O register.

PA6~PA7：always read as 0.

R06H : Port B

PortB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
	Always available							

PB0~PB7：Have pin change interrupt

R07H : Port C

PortC	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
	-	-	Always available					

PC0~PC5：portC I/O register.

PC6~PC7：always read as 0.

R08H : Port D

PortD	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	Always available							

R09H : Port E

PortE	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	Always available							

R0AH : PCHLAT(Program counter high byte.)

BIT 7~0	-	-	-	PCH4	PCH3	PCH2	PCH1	PCH0

Bit0~4：Hiht byte of PC.

Bit5~7：always read as 0

R0BH : INTS(Interrupt control register.)

Bit	Symbol	Function
0	RBIF	PORT B change interrupt flag.
1	INTF	PB0/IRQ external interrupt flag bit.
2	TIF	Timer0 overflow interrupt flag bit.
3	RBIE	0 ： disable PB change interrupt 1 ： enable PB change interrupt
4	INTS	0 ： disable INT interrupt 1 ： enable INT interrupt
5	TIS	0 ： disable TMR0 interrupt 1 ： enable TMR0 interrupt
6	PEIE	0 ： disable all peripheral interrupt 1 ： enable all peripheral interrupt
7	GIS	0 ： disable global interrupt 1 ： enable global interrupt

R0CH : PIFB1(Peripheral interrupt flag register.)

BIT 7~0	LCDIF	-	-	-	-	-	-	TMR1IF

Bit 0：Timer1 overflow interrupt flag bit

Bit 7：LCD interrupt flag bit

Bit1~6：always read as 0

R0EH : TMR1L(Timer1 data register low byte.)

ROFH : TMR1H(Timer1 data register high byte.)

R10H : T1STA(Timer1 control register)

Bit	Symbol	Function
0	TMR1ON	0 ： Stop TMR1 1 ： Enable TMR1
1	TMR1CLK	0 ： Internal clock (Fosc/4) 1 ： External clock from pin PC0
2	$\overline{\text{T1SYNC}}$	TMR1CLK = 1 0 ： Synchronize external clock 1 ： Do not synchronize external clock TMR1CLK = 0 This bit is ignored
3	T1OSCEN	0 ： TMR1 Oscillator is shut off 1 ： TMR1 Oscillator is enable
4~5	T1CKPS1 ~ T1CKPS0	1 1 = 1：8 Prescale value 1 0 = 1：4 Prescale value 0 1 = 1：2 Prescale value 0 0 = 1：1 Prescale value
6~7	-	Unimplemented

R15H : CCP1L(Timer1 compare LSB)

R16H : CCP1H(Timer1 compare MSB)

R17H : CCPCTL

Bit	Symbol	Function
0	CCPM0	0 ： COMPARE off 1 ： COMPARE on
1~7	-	Unimplemented.

R20H~R7FH : General purpose register

- **BANK 1**

R81H : TMR(Time Mode Register)

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
0~2	PS0~2	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 0 1	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit 0 : RTCC 1 : Watchdog Timer		
4	TCE	RTCC signal edge : 0 : Increment on low-to-high transition on RTCC pin 1 : Increment on high-to-low transition on RTCC pin		
5	TCS	RTCC signal set : 0 : Internal instruction cycle clock 1 : Transition on RTCC pin		
6	IES	Interrupt edge select 0 : Interrupt on falling edge on PB0 1 : Interrupt on rising edge on PB0		
7	/PBPH	PORTB pull-hi 0 : PORTB pull-hi are enable 1 : PORTB pull-hi are disable		

R85H : CPIO A (Control Port I/O Mode Register)

0： I/O pin in output mode;

1： I/O pin in input mode.

R86H : CPIO B (Control Port I/O Mode Register)

0： I/O pin in output mode;

1： I/O pin in input mode.

R87H : CPIO C (Control Port I/O Mode Register)

0： I/O pin in output mode;

1： I/O pin in input mode.

R88H : CPIO D (Control Port I/O Mode Register)

0： I/O pin in output mode;

1： I/O pin in input mode.

R89H : CPIO E (Control Port I/O Mode Register)

0： I/O pin in output mode;

1： I/O pin in input mode.

R8CH : PIEB1

Bit	Symbol	Function
0	TMR1IE	TMR1 interrupt enable bit 0 ： disable TMR1 interrupt 1 ： enable TMR1 interrupt
1~6	-	Unimplemented.
7	LCDIE	LCD interrupt enable bit 0 : disable LCD interrupt 1 : enable LCD interrupt

R8EH : PSTA

Bit	Symbol	Function
0	-	Unimplemented.
1	PORB	0:Power on Reset occurred 1:No Power on Reset occurred
2~7	-	Unimplemented.

R90H:CMPPH

Bit	Symbol	Function
0	CMPS0	0:PA0,PA1 as TTL input 1:PA0,PA1 as Comparaotr input
1	CMPS1	0:PA2,PA3 as TTL input 1:PA2,PA3 as Comparaotr input
2~3	CMPRS0~1	1 1 = PA1,PA3 select extrenal vrefence voltage 1 0 = PA1,PA3 select 3/4 VDD as vrefence voltage 0 1 = PA1,PA3 select 1/2 VDD as vrefence voltage 0 0 = PA1,PA3 select 1/4 VDD as vrefence voltage
4	PAHR	0:Port A pull up enable 1:Port A pull up disable
5	PCHR	0:Port C pull up enable 1:Port C pull up disable
6~7	-	-

- **BANK2**

R107H : PortF

PortF	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0
	Always read available							

108H : PortG

PortG	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
	Always read available							

R10DH ：LCDPFS(Lcd pin function select)

Bit	Symbol	Function
0	DL00	0 ： PD0~PD4 as digital input 1 ： PD0~PD4 as LCD driver
1	DL05	0 ： PE0~PE3 as digital input 1 ： PE0~PE3 as LCD driver
2	DL09	0 ： PE4~PE6 as digital input 1 ： PE4~PE6 as LCD driver
3	DL12	0 ： PF0~PF3 as digital input 1 ： PF0~PF3 as LCD driver
4	DL16	0 ： PF4~PF7 as digital input 1 ： PF4~PF7 as LCD driver
5	DL20	0 ： PG0~PG6 as digital input 1 ： PG0~PG6 as LCD driver
6	DL27	0 ： PG7,PE7 as digital input 1 ： PG7,PE7 as LCD driver
7	DL29	0 ： PD5~PD7 as digital input 1 ： PD5,PD7 as LCD driver

R10EH : LCDFS(LCD frame frequency select)

BIT 7~0	-	-	-	-	FS3	FS2	FS1	FS0

Common select	Frame frequency
1/2	Clock/[128 * (FS3:FS0+1)]
1/3	Clock/[96 * (FS3:FS0+1)]
1/4	Clock/[128 * (FS3:FS0+1)]

R10FH : LCDCTL(LCD control)

Bit	Symbol	Function
0~1	LCDS0~1	LCD Common select bits 0 0： -- 0 1： 1/2 (use COM 0,1) 1 0： 1/3 (use COM 0,1,2) 1 1： 1/4 (use COM 0,1,2,3)
2~3	CLKS0~1	Clock select 0 0： sysclk/256 0 1： Timer1 clk (must enable T1 osc) 1 X： internal RC
4	CRS	Cap mode and Resistor mode select 0 ： Resistor mode 1 ： Cap mode
5	BIASS	BIAS Select 0 ： Use 1/2 bias mode 1 ： Use 1/3 bias mode
6	SLPE	LCD enabled in Sleep mode 0 ： LCD enable in sleep mode 1 ： LCD disable in sleep mode
7	LCDE	LCD enable bit 0 ： LCD disable 1 ： LCD enable

R110H~R11FH : LCD00~LCD15(LCD data register 00~15)

Address	Symbol	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R110H	LCD00	SEG07 COM0	SEG06 COM0	SEG05 COM0	SEG04 COM0	SEG03 COM0	SEG02 COM0	SEG01 COM0	SEG00 COM0
R111H	LCD01	SEG15 COM0	SEG14 COM0	SEG13 COM0	SEG12 COM0	SEG11 COM0	SEG10 COM0	SEG09 COM0	SEG08 COM0
R112H	LCD02	SEG23 COM0	SEG22 COM0	SEG21 COM0	SEG20 COM0	SEG19 COM0	SEG18 COM0	SEG17 COM0	SEG16 COM0
R113H	LCD03	*SEG31 COM0	*SEG30 COM0	*SEG29 COM0	SEG28 COM0	SEG27 COM0	SEG26 COM0	SEG25 COM0	SEG24 COM0
R114H	LCD04	SEG07 COM1	SEG06 COM1	SEG05 COM1	SEG04 COM1	SEG03 COM1	SEG02 COM1	SEG01 COM1	SEG00 COM1
R115H	LCD05	SEG15 COM1	SEG14 COM1	SEG13 COM1	SEG12 COM1	SEG11 COM1	SEG10 COM1	SEG09 COM1	SEG08 COM1
R116H	LCD06	SEG23 COM1	SEG22 COM1	SEG21 COM1	SEG20 COM1	SEG19 COM1	SEG18 COM1	SEG17 COM1	SEG16 COM1
R117H	LCD07	*SEG31 COM1	*SEG30 COM1	*SEG29 COM1	SEG28 COM1	SEG27 COM1	SEG26 COM1	SEG25 COM1	SEG24 COM1
R118H	LCD08	SEG07 COM2	SEG06 COM2	SEG05 COM2	SEG04 COM2	SEG03 COM2	SEG02 COM2	SEG01 COM2	SEG00 COM2
R119H	LCD09	SEG15 COM2	SEG14 COM2	SEG13 COM2	SEG12 COM2	SEG11 COM2	SEG10 COM2	SEG09 COM2	SEG08 COM2
R11AH	LCD10	SEG23 COM2	SEG22 COM2	SEG21 COM2	SEG20 COM2	SEG19 COM2	SEG18 COM2	SEG17 COM2	SEG16 COM2
R11BH	LCD11	*SEG31 COM2	*SEG30 COM2	*SEG29 COM2	SEG28 COM2	SEG27 COM2	SEG26 COM2	SEG25 COM2	SEG24 COM2
R11CH	LCD12	SEG07 COM3	SEG06 COM3	SEG05 COM3	SEG04 COM3	SEG03 COM3	SEG02 COM3	SEG01 COM3	SEG00 COM3
R11DH	LCD13	SEG15 COM3	SEG14 COM3	SEG13 COM3	SEG12 COM3	SEG11 COM3	SEG10 COM3	SEG09 COM3	SEG08 COM3
R11EH	LCD14	SEG23 COM3	SEG22 COM3	SEG21 COM3	SEG20 COM3	SEG19 COM3	SEG18 COM3	SEG17 COM3	SEG16 COM3
R11FH	LCD15	*SEG31 COM3	*SEG30 COM3	*SEG29 COM3	SEG28 COM3	SEG27 COM3	SEG26 COM3	SEG25 COM3	SEG24 COM3

* These bits don't display, but can used as general ram.

- **BANK3**

R187H : CPIO F

R188H : CPIO G

7.Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	N/A	N/A	N/A
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC+1
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--00 0000	--00 0000	--uu uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT C	07h	--xx xxxx	--uu uuuu	--uu uuuu
PORT D	08h	0000 0000	0000 0000	uuuu uuuu
PORT E	09h	0000 0000	uuuu uuuu	uuuu uuuu
PCHLAT	0Ah	---- 0000	---- 0000	---- uuuu
INS	0Bh	0000 0001	0000 0001	uuuu uuuu
PIFB1	0Ch	1 --- --- x	1 --- --- u	U --- --- u
TMR1L	0Eh	xxxx xxxx	uuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuu uuuu	uuuu uuuu
T1STA	10h	--00 0000	--00 0000	--uu uuuu
CCPR1L	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPCTL	17h	---- ---0	---- ---0	---- ---u
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	--11 1111	--11 1111	--uu uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu
CPIOC	87h	--11 1111	--11 1111	--uu uuuu
CPIOD	88h	1111 1111	1111 1111	uuuu uuuu
CPIOE	89h	1111 1111	1111 1111	uuuu uuuu
PIEB1	8Ch	---- ---0	---- ---0	---- ---u
PWRCON	8Eh	---- --#-	---- --u-	---- --u-
CMPPH	90h	0011 0000	0011 uuuu	00uu uuuu
PORT F	107h	0000 0000	0000 0000	uuuu uuuu
PORT G	108h	0000 0000	0000 0000	uuuu uuuu

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
LCDPFS	10Dh	1111 1111	1111 1111	uuuu uuuu
LCDFS	10Eh	---- 0000	---- 0000	---- uuuu
LCDCTL	10Fh	0000 0000	0000 0000	uuuu uuuu
Lcd00~15	110h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CPIO F	186h	1111 1111	1111 1111	uuuu uuuu
CPIO G	187h	1111 1111	1111 1111	uuuu uuuu

Note ： u＝unchanged， x＝unknown， - ＝unimplemented， read as “0”
#＝value depends on the condition of the following table

Condition	Status bit 4	Status bit 3	PWRCON bit 1
POWR ON RESET	1	1	0
/MCLR reset (not during SLEEP)	u	u	u
/MCLR reset during SLEEP	1	0	u
WDT reset (not during SLEEP)	0	1	u
WDT reset during SLEEP	0	0	u
Interrupt Wake-up during SLEEP	1	0	u

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMR register	W→TMR	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) (4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z

Instruction Code	Mnemonic Operands	Function	Operation	Status
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110001 iiiiiiii	RTIW i	Return, place immediate to W	Stack→PC, i→W	None
110111 iiiiiiii	ADDWI	Add immediate to W	PC+1→PC, W+i→W	C,HC,Z
111000 iiiiiiii	SUBWI	Subtract W from immediate	i-W→W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack→PC,1→GIS	None
010000 00000100	RET	Return from subroutine	Stack→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register	0	:	Working register
CPIO	:	Control I/O port register	1	:	General register
		(PA, PB, PC Only)	R	:	General register address
TF	:	Timer overflow flag	C	:	Carry flag
PF	:	Power loss flag	HC	:	Half carry
PC	:	Program Counter	Z	:	Zero flag
OSC	:	Oscillator	/	:	Complement

Inclu.	:	Inclusive ‘∪’	x	:	Don’t care
Exclu.	:	Exclusive ‘⊕’	i	:	Immediate data (8 bits)
AND	:	Logic AND ‘∩’	n	:	Immediate address

9. Electrical Characteristics

(Operating temperature at 25℃).

1、Operation Current:

(1) HF (C=10p), WDT – disable, PED – disable

	4M	10M	20M	Sleep
2.5V	480uA	1mA	2.1mA	1uA
3.0V	600uA	1.3mA	2.5mA	1uA
4.0V	1mA	2mA	4mA	1uA
5.0V	1.5mA	2.9mA	5.3mA	1uA
5.5V	1.8mA	4mA	6.8mA	1uA

* These parameters are for reference only.

(2) XT (C=10p), WDT – disable, PED – disable

	1M	4M	10M	Sleep
2.5V	130uA	440uA	1mA	1uA
3.0V	160uA	560uA	1.2mA	1uA
4.0V	400uA	900uA	2mA	1uA
5.0V	700uA	1.3mA	2.8mA	1uA
5.5V	940uA	1.6mA	3.3mA	1uA

These parameters are for reference only.

(3) LF (C=10p), WDT – disable, PED – disable

	32K	455K	1M	Sleep
2.5V	30uA	80uA	170uA	1uA
3.0V	40uA	120uA	210uA	1uA
4.0V	90uA	210uA	420uA	1uA
5.0V	180uA	450uA	600uA	1uA
5.5V	270uA	600uA	900uA	1uA

These parameters are for reference only.

(4)RC, WDT – disable, PED – disable, @VDD = 5.0V

C	R	Freq.	Current
3p	4.7k	6.4M	4mA
	10k	4.4M	2mA
	47k	1.2M	600uA
	100k	576k	400uA
	300k	192k	250uA
	470k	122k	200uA
20p	4.7k	3.5M	2.7mA
	10k	2.4M	1.5mA
	47k	624k	500uA
	100k	304k	350uA
	300k	102k	250uA
	470k	64k	200uA
100p	4.7k	1.1M	1.7mA
	10k	720k	900uA
	47k	180k	300uA
	100k	87k	250uA
	300k	29k	200uA
	470k	17k	200uA
300p	4.7k	434k	1.4mA
	10k	297k	700uA
	47k	75k	250uA
	100k	36k	200uA
	300k	12k	200uA
	470k	7k	200uA

These parameters are for reference only.

(5)RC, WDT – disable, PED – disable, @VDD = 3.0V

C	R	Freq.	Current
3p	4.7k	8M	2mA
	10k	5.4M	1.2mA
	47k	1.5M	300uA
	100k	764k	160uA
	300k	260k	60uA
	470k	164k	60uA
20p	4.7k	4.8M	1.5mA
	10k	3.3M	800uA
	47k	856k	170uA
	100k	424k	100uA
	300k	144k	60uA
	470k	92k	60uA
100p	4.7k	1.8M	1mA
	10k	1.2M	500uA
	47k	308k	120uA
	100k	152k	60uA
	300k	52k	60uA
	470k	32k	60uA
300p	4.7k	760k	800uA
	10k	488k	400uA
	47k	124k	100uA
	100k	60k	60uA
	300k	20k	60uA
	470k	13k	60uA

These parameters are for reference only.

2. Input Voltage (VDD = 5V):

	PA~PC	Min	Max
Vil	TTL	VSS	0.8V
	Schmitt trigger	VSS	0.6V
Vih	TTL	3.0V	VDD
	Schmitt trigger	3.8V	VDD

These parameters are for reference only.

Input Voltage (VDD = 3V):

	PA~PC	Min	Max
Vil	TTL	VSS	0.4V
	Schmitt trigger	VSS	0.2V
Vih	TTL	2.0V	VDD
	Schmitt trigger	2.6V	VDD

These parameters are for reference only.

3. Output Voltage (VDD = 5V):

	PA~PC	Condition
Voh	3.0V	Ioh = -20mA
Vol	0.9V	Iol = 20mA
Voh	4.0V	Ioh = -5mA
Vol	0.6V	Iol = 5mA

These parameters are for reference only.

Output Voltage (VDD = 3V):

	PA~PC	Condition
Voh	1.0V	Ioh = -10mA
Vol	0.6V	Iol = 10mA
Voh	2.0V	Ioh = -5mA
Vol	0.4V	Iol = 5mA

These parameters are for reference only.

4. Output Current (Max.) (VDD = 5V):

	Current
Source current	25mA
Sink current	40mA

These parameters are for reference only.

5. The basic WDT time-out cycle time:

	Time
2.5V	26ms
3.0V	24ms
4.0V	21.7ms
5.0V	20ms
5.5V	19.5ms

These parameters are for reference only.

6. Pull high resistor:

VDD	5V	3V
PA、PB	50KΩ±20%	100KΩ±20%
PC	100KΩ±20%	200KΩ±20%

These parameters are for reference only.

7. Sleep current

(1) Sleep with wdt enable currnet

	Current
2.5V	3u
3.0V	5u
4.0V	10u
5.0V	14u

These parameters are for reference only.

(2)Sleep with LCD enable no load.

	CAP. MODE WITH 32K T1OSC AT 1/2BIAS	RES. MODE WITH 32K T1OSC AT 1/2BIAS
3.0V	5.5u	10u
5.0V	15u	45u

These parameters are for reference only.

8. Comparator Response time(VDD=5V)

Vref	Vin	Response time
VDD/4	Vref ± 0.2v	8μS
VDD/2	Vref ± 0.2v	8μS
VDD3/4	Vref ± 0.2v	8μS
VDD-0.8	Vref ± 0.2v	8μS

9. MCLR filter time:

VDD	5V
Time	600ns±20%

These parameters are for reference only.

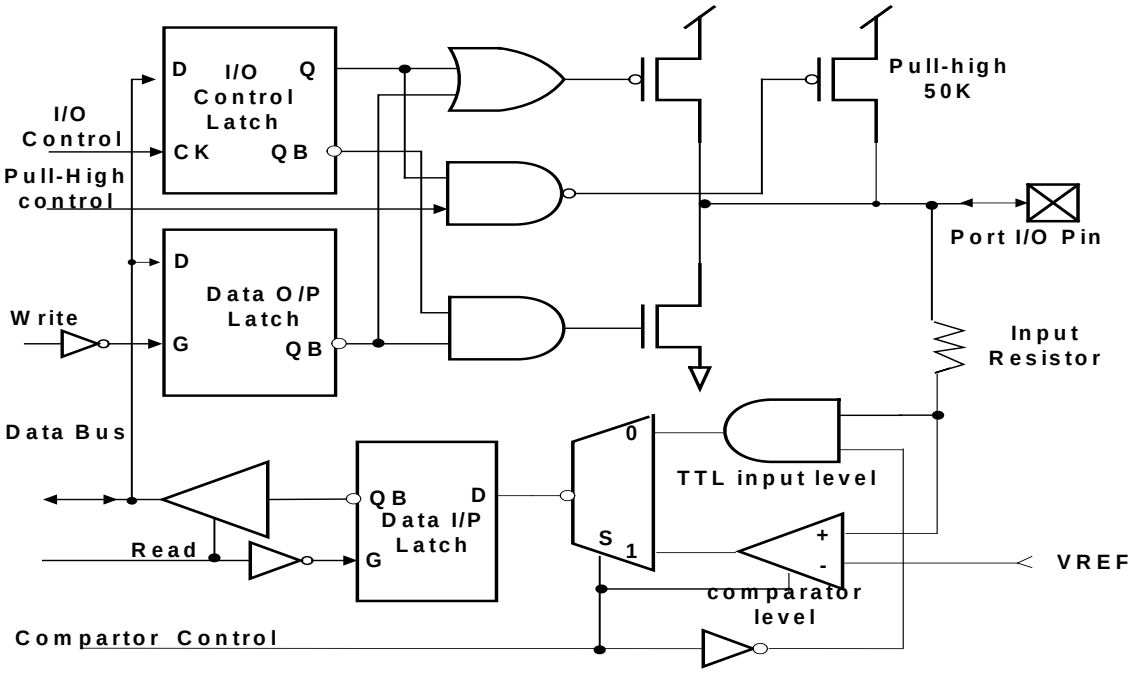
10. Internal LCD resister current between vlcd pin and VDD

	1/2BIAS	1/3BIAS
5V	40μA	10μA
3.0V	6μA	0.4μA

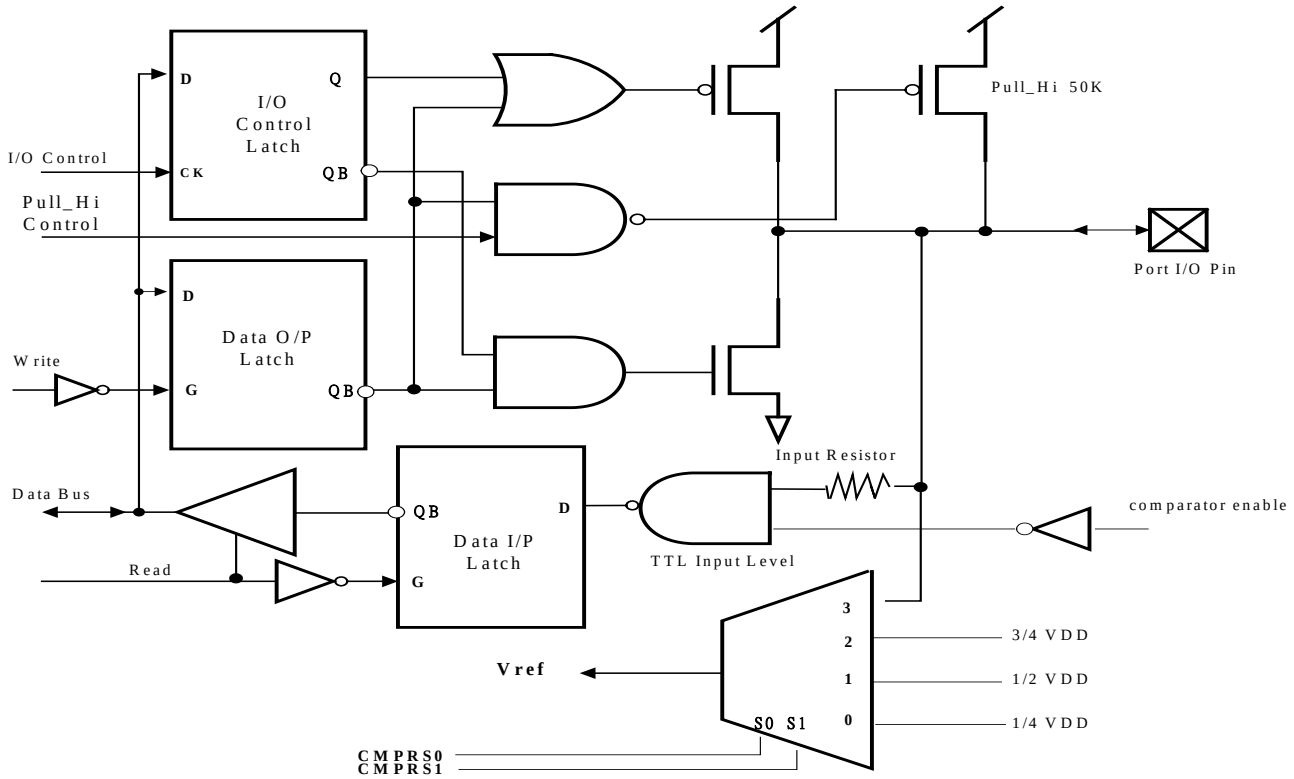
10. Equivalent Circuit

- ***Port A***

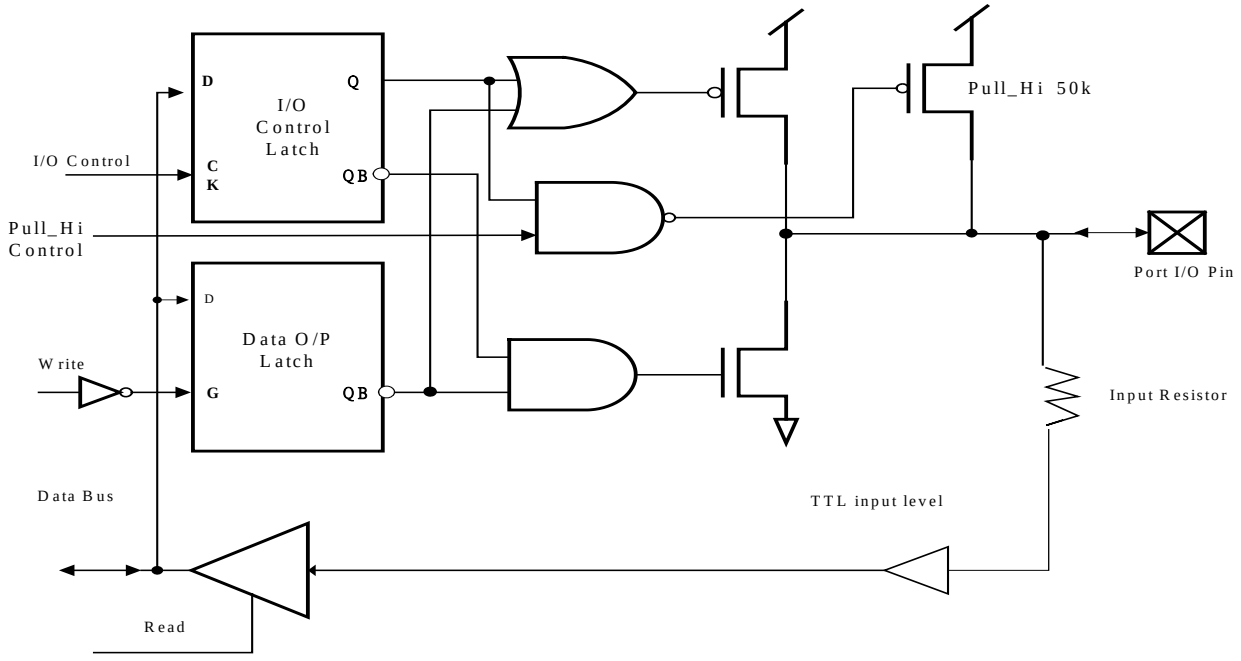
PA0,PA2



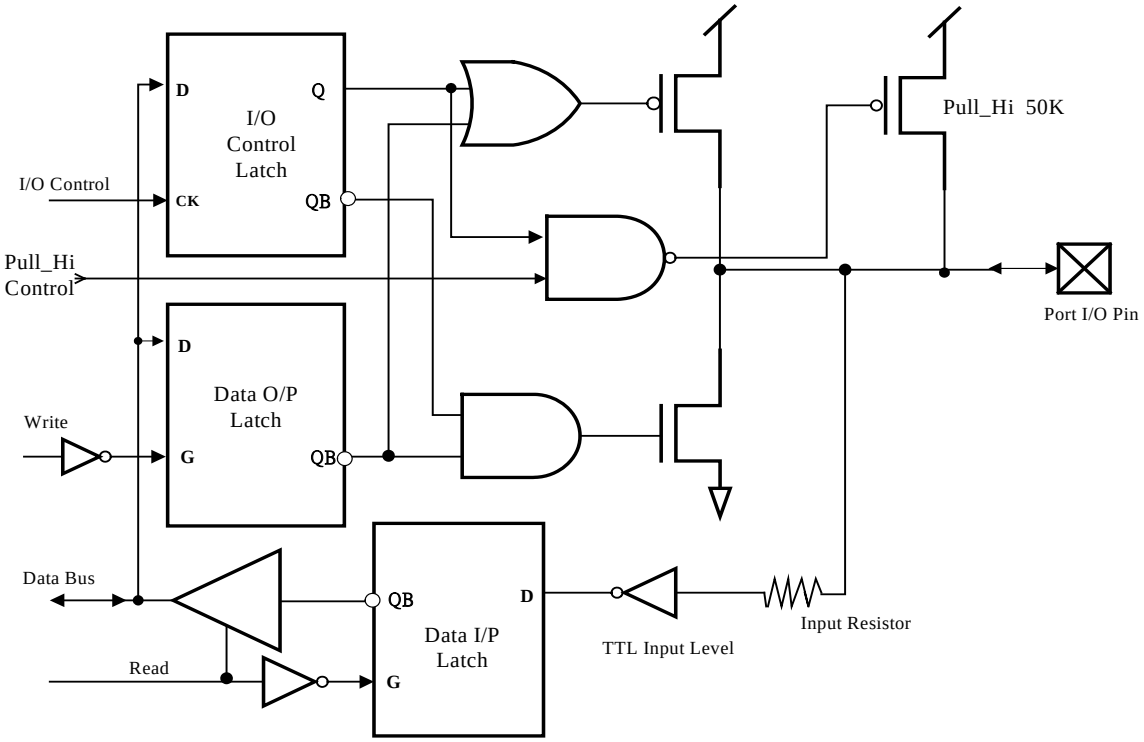
PA1,PA3



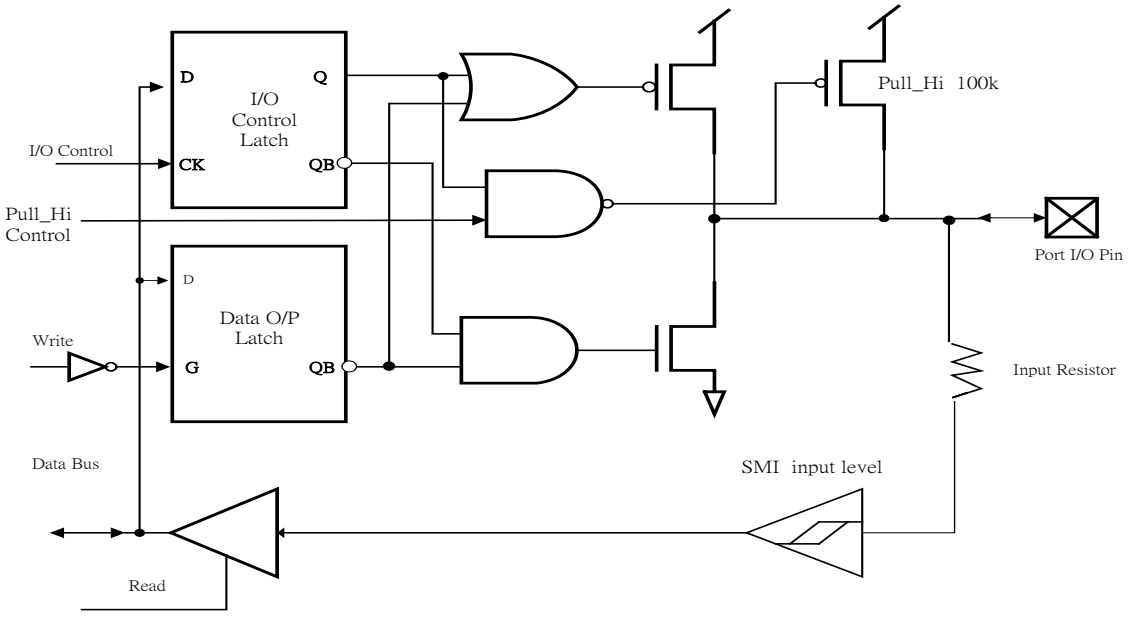
PA4,PA5



Port B

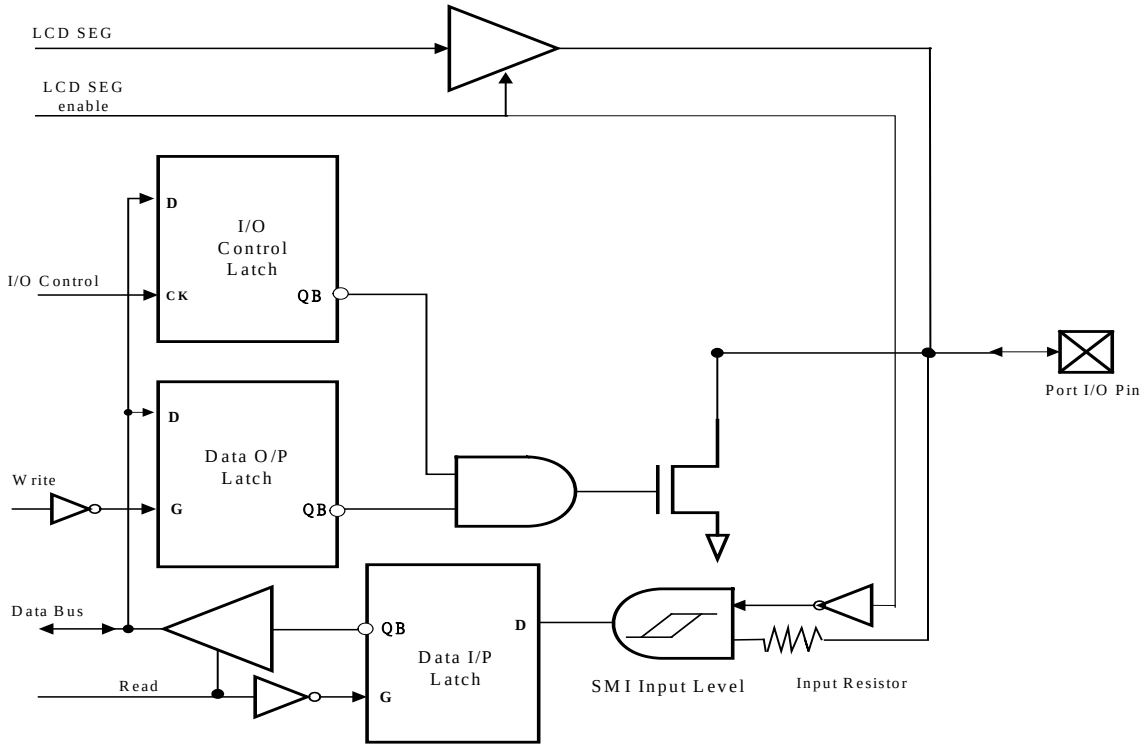

D
Q
I/O
Control
Latch
CK
QB
I/O Control
Pull_Hi
Control
Pull_Hi 50K
Port I/O Pin
D
Data O/P
Latch
Write
G
QB
Data Bus
QB
D
Data I/P
Latch
G
Read
TTL Input Level
Input Resistor

Port C

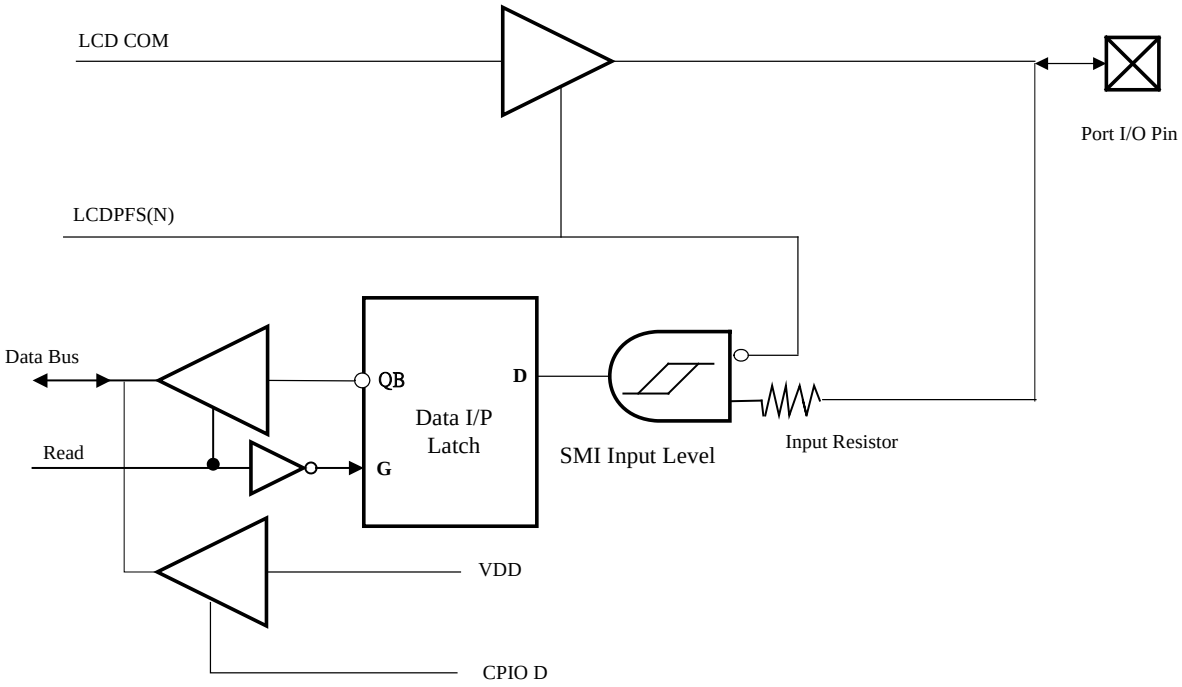

D
Q
I/O
Control
Latch
CK
QB
I/O Control
Pull_Hi
Control
Pull_Hi 100k
Port I/O Pin
D
Data O/P
Latch
Write
G
QB
Input Resistor
Data Bus
SMI input level
Read

Port D

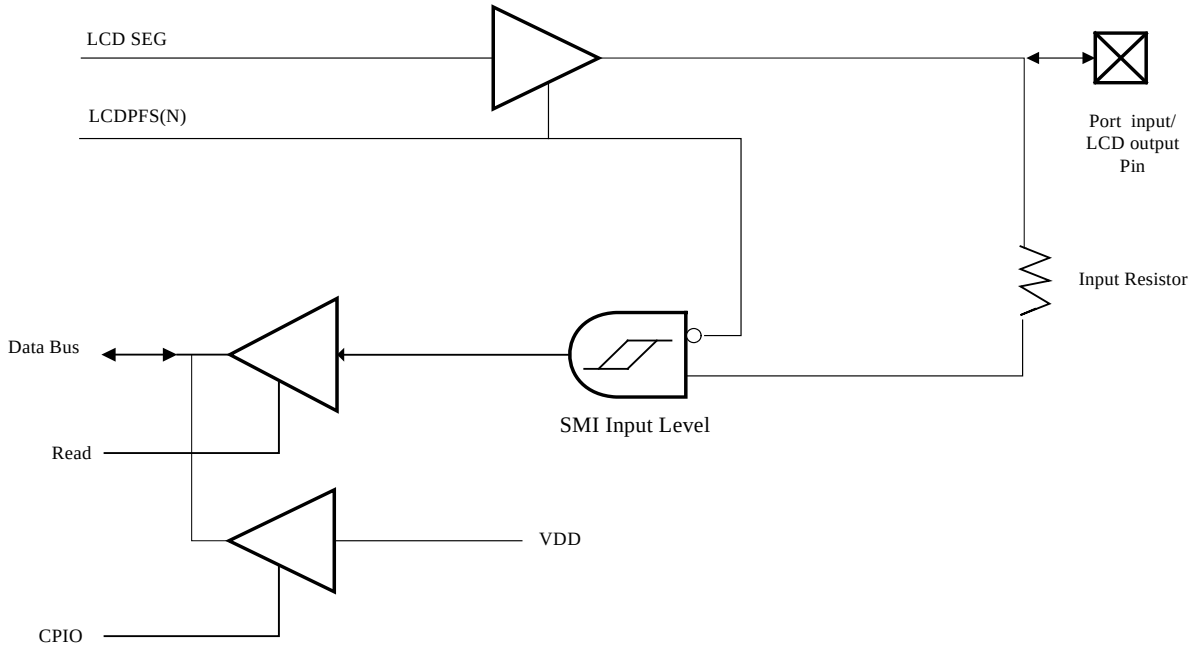
PD0~PD3



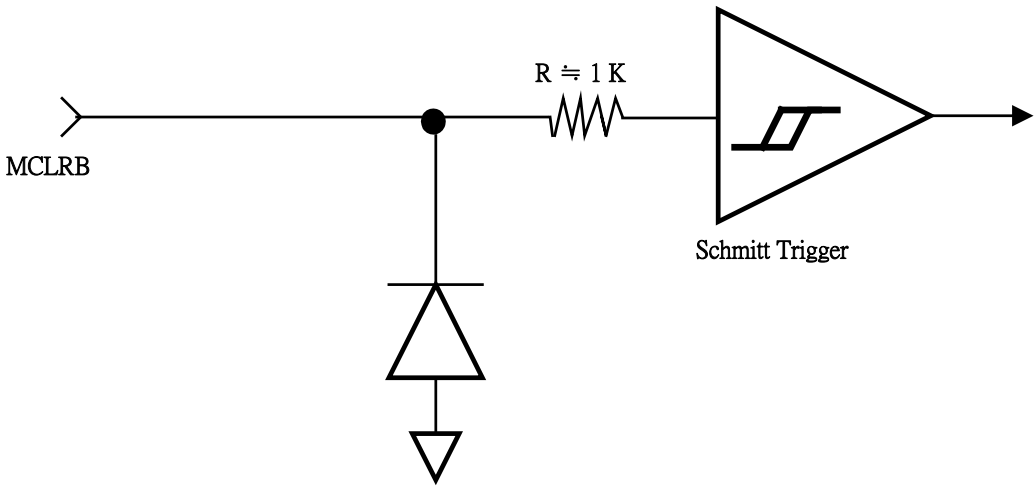
PD5~PD7



Port E、F、G

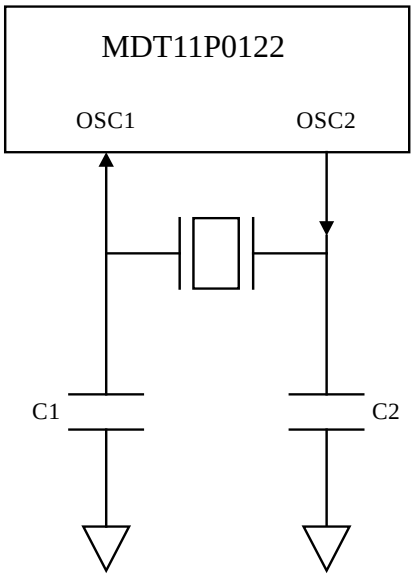


MCLRB PIN



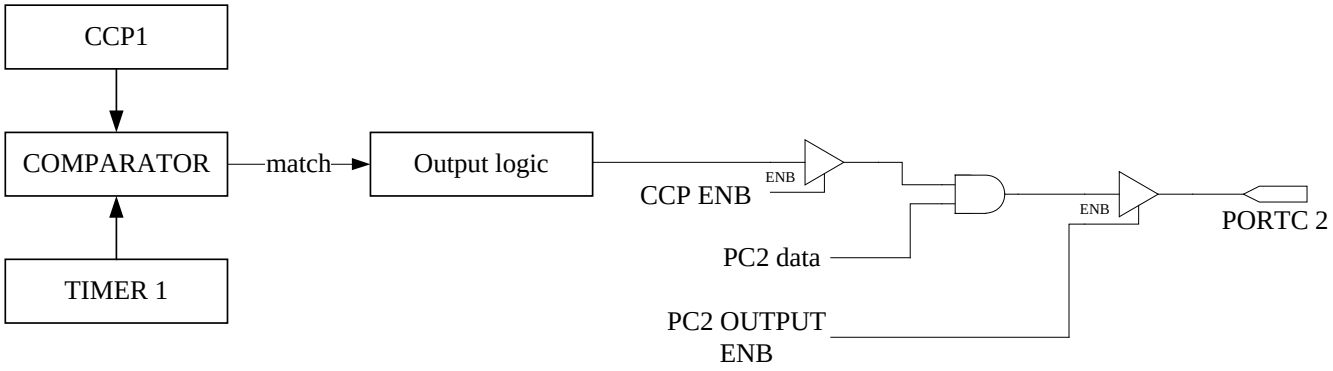
11. External Capacitor Selection For Crystal Oscillator

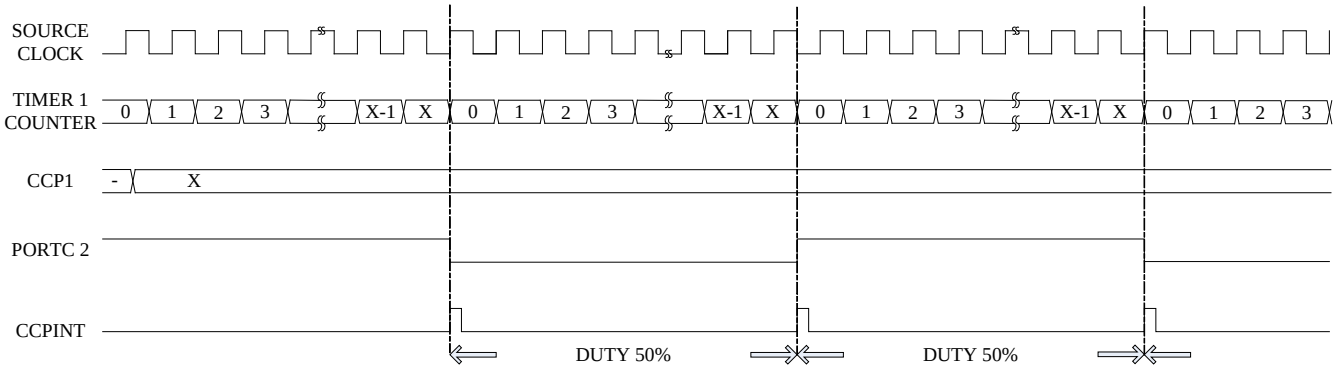
Osc. Type	Resonator Freq.	C1	C2
HF	20 MHz	5 pF ~10 pF	10 pF ~30 pF
	10 MHz	10 pF ~50 pF	20 pF ~100 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
XT	10 MHz	10 pF ~30 pF	10 pF ~50 pF
	4 MHz	10 pF ~50 pF	20 pF ~100 pF
	1 MHz	10 pF ~30 pF	20 pF ~50 pF
LF	1 MHz	3 pF ~5 pF	3 pF ~5 pF
	455 K	10 pF ~30 pF	20 pF ~50 pF
	32 K	10 pF ~20 pF	15 pF ~30 pF



To increase the stability of oscillator and the ability of anti-noise, the above values of the external capacitor are for reference only, but the higher capacitance also increases the start-up time.

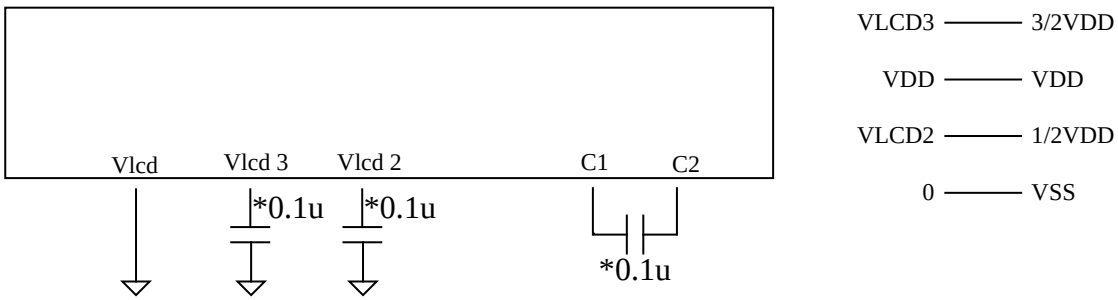
12. Timer1 compare mode





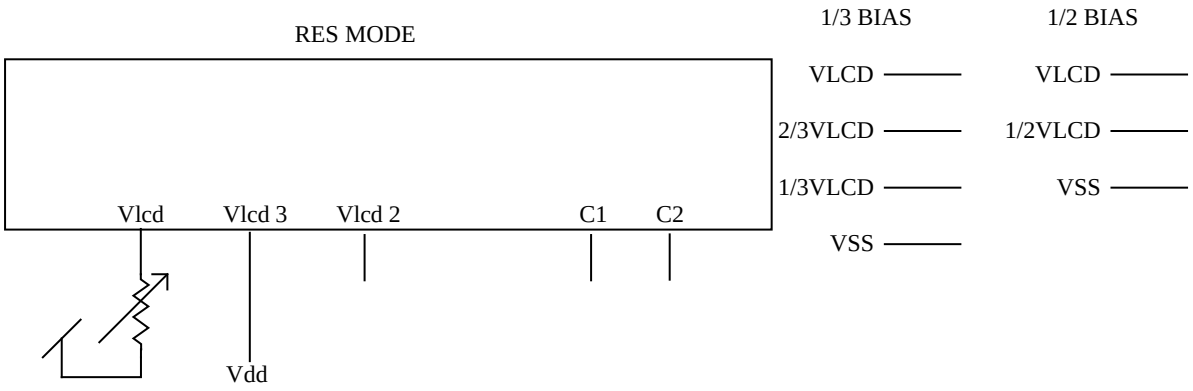
13. LCD APPLICATION

(1) LCD voltage generation at CAP mode



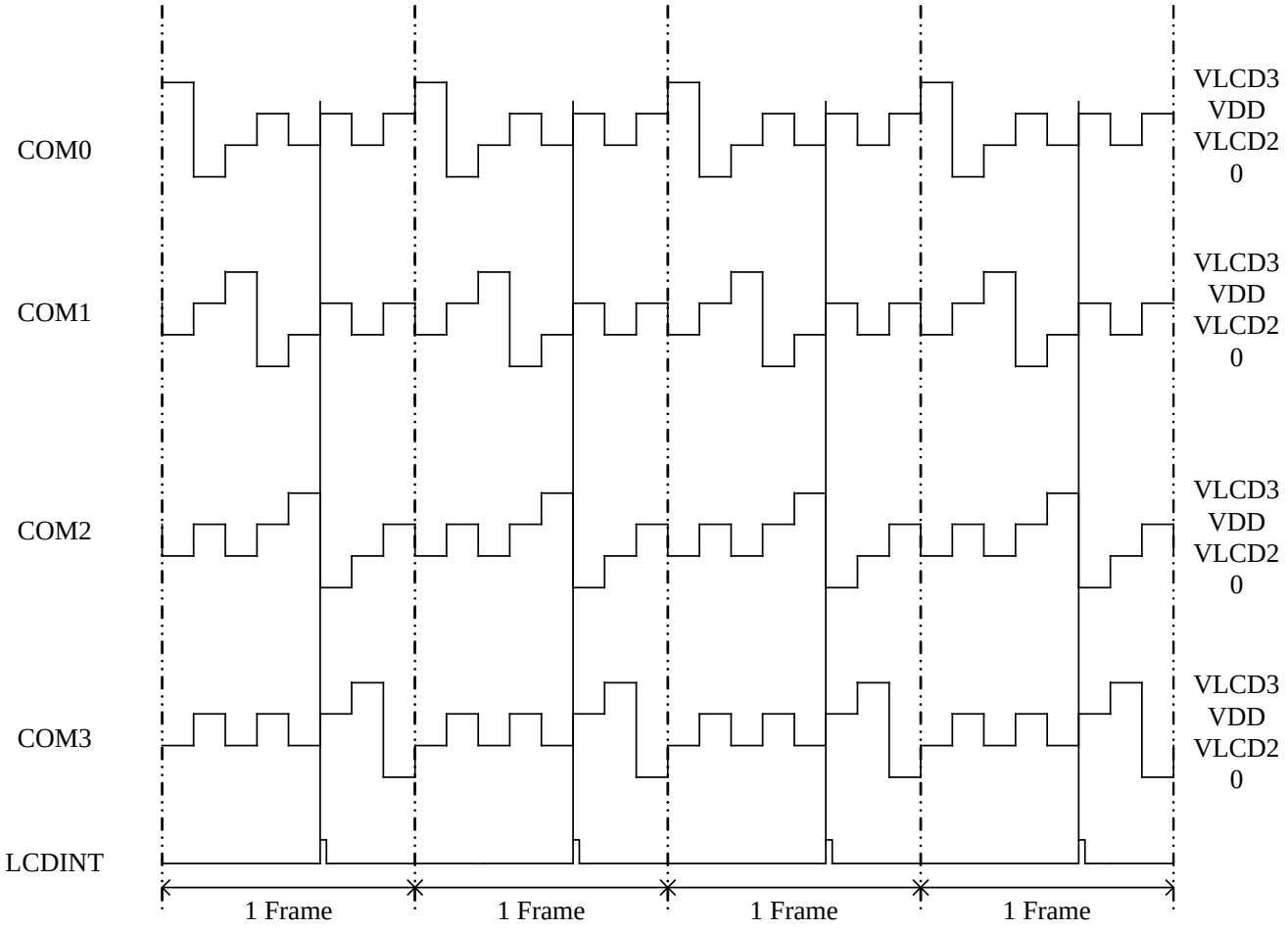
*These value are adjusted to the application by designer

(2) LCD voltage generation at resister mode



* Designer can adjust vlcd resister to change lcd voltage at resister mode.

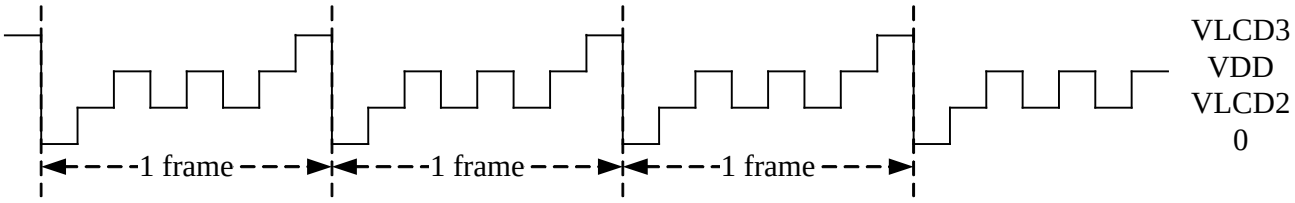
(3) LCD Interrupt (in 1/3 bias, 1/4 duty)



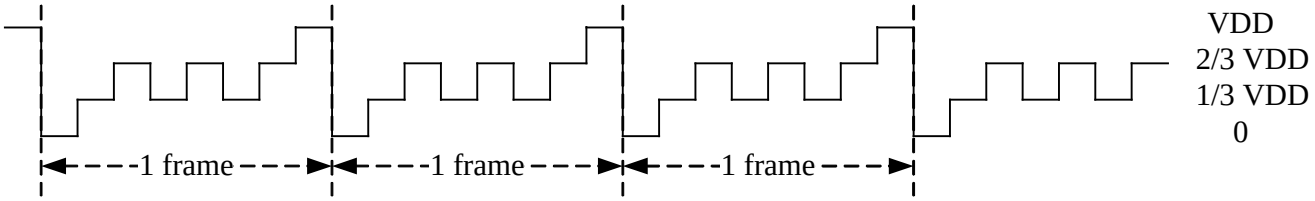
This interrupt can be used to write next frame data

(4) LCD waveform voltage diagram

1/3 BIAS 1/4 duty AT CAP



1/3 BIAS 1/4 duty AT RES



1/2 BIAS AT 1/4 duty RES/CAP