

# F100364

## Low Power 16-Input Multiplexer

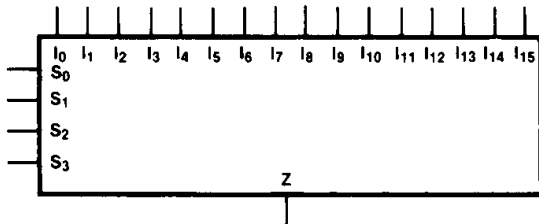
### General Description

The F100364 is a 16-input multiplexer. Data paths are controlled by four Select lines ( $S_0$ – $S_3$ ). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data. All inputs have 50 k $\Omega$  pulldown resistors.

### Features

- 35% power reduction of the F100164
- 2000V ESD protection
- Pin/function compatible with F100164
- Voltage compensated operating range =  $-4.2V$  to  $-5.7V$

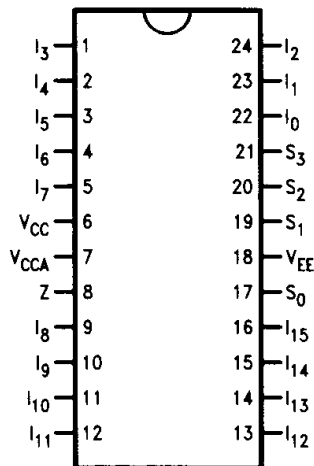
### Logic Symbol



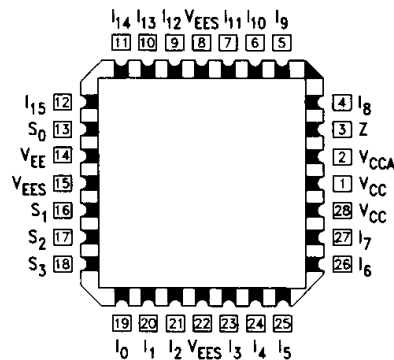
TL/F/10265-1

Pin Names	Description
$I_0$ – $I_{15}$	Data Inputs
$S_0$ – $S_3$	Select Inputs
Z	Data Output

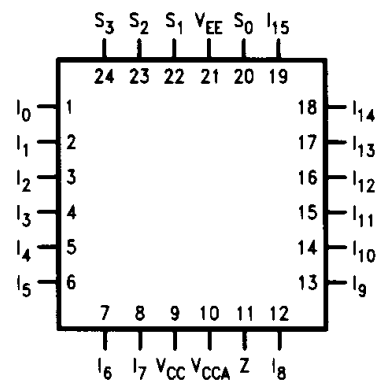
### Connection Diagrams

**24-Pin DIP**


TL/F/10265-2

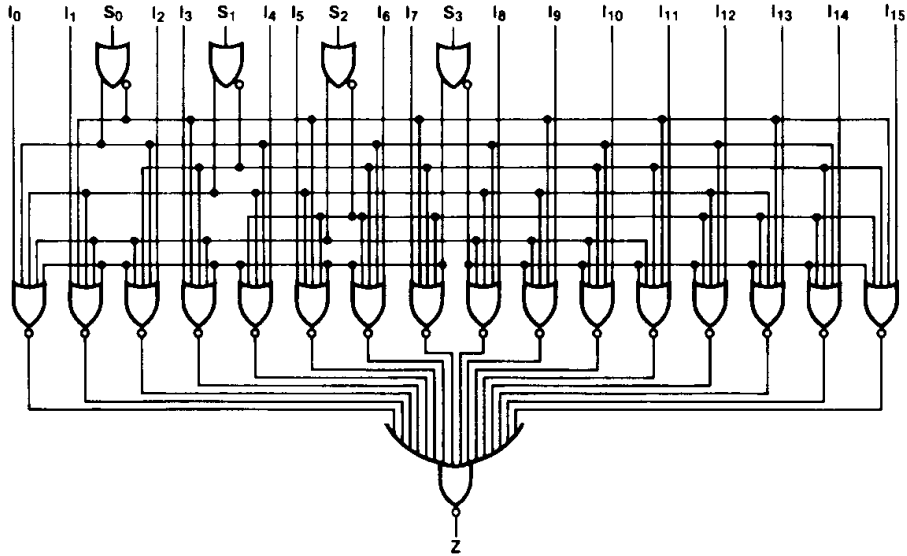
**28-Pin PCC**


TL/F/10265-4

**24-Pin Quad Cerpak**


TL/F/10265-3

## Logic Diagram



TL/F/10265-5

## Truth Table

Select Inputs				Output
S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	Z
L	L	L	L	I <sub>0</sub>
H	L	L	L	I <sub>1</sub>
L	H	L	L	I <sub>2</sub>
H	H	L	L	I <sub>3</sub>
L	L	H	L	I <sub>4</sub>
H	L	H	L	I <sub>5</sub>
L	H	H	L	I <sub>6</sub>
H	H	H	L	I <sub>7</sub>
L	L	L	H	I <sub>8</sub>
H	L	L	H	I <sub>9</sub>
L	H	L	H	I <sub>10</sub>
H	H	L	H	I <sub>11</sub>
L	L	H	H	I <sub>12</sub>
H	L	H	H	I <sub>13</sub>
L	H	H	H	I <sub>14</sub>
H	H	H	H	I <sub>15</sub>

H = HIGH Voltage Level  
L = LOW Voltage Level

## Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T <sub>STG</sub> )	-65°C to +150°C
Maximum Junction Temperature (T <sub>J</sub> )	
Ceramic	+175°C
Plastic	+150°C
Pin Potential to Ground Pin (V <sub>EE</sub> )	-7.0V to +0.5V
Input Voltage (DC)	V <sub>EE</sub> to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≤ 2000V

## Recommended Operating Conditions

Case Temperature (T <sub>C</sub> )	
Commercial	0°C to +85°C
Military	-55°C to +125°C
Supply Voltage (V <sub>EE</sub> )	
Commercial	-5.7V to -4.2V
Military	-5.7V to -4.2V

## Commercial Version

### DC Electrical Characteristics

V<sub>EE</sub> = -4.2V to -5.7V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V <sub>OH</sub>	Output HIGH Voltage	-1025	-955	-870	mV	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V
V <sub>OL</sub>	Output LOW Voltage	-1830	-1705	-1620	mV		
V <sub>OHC</sub>	Output HIGH Voltage	-1035			mV	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V
V <sub>OLC</sub>	Output LOW Voltage			-1610	mV		
V <sub>IH</sub>	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.5			μA	V <sub>IN</sub> = V <sub>IL</sub> (Min)	
I <sub>IH</sub>	Input HIGH Current			300	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max)	
I <sub>EE</sub>	Power Supply Current	-89		-45	mA	Inputs Open	

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operate under "worst case" conditions.

### Ceramic Dual-In-Line Package AC Electrical Characteristics

V<sub>EE</sub> = -4.2V to -5.7V, V<sub>CC</sub> = V<sub>CCA</sub> = GND

Symbol	Parameter	T <sub>C</sub> = 0°C		T <sub>C</sub> = +25°C		T <sub>C</sub> = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>0</sub> -I <sub>15</sub> to Output	0.90	2.00	0.90	2.00	0.90	2.10	ns	Figures 1, 2
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>0</sub> , S <sub>1</sub> to Output	1.40	2.80	1.40	2.80	1.50	2.90	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>2</sub> , S <sub>3</sub> to Output	1.00	2.20	1.00	2.20	1.10	2.40	ns	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	

## Commercial Version (Continued)

### PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_0-I_{15}$ to Output	0.90	1.80	0.90	1.80	0.90	1.90	ns	Figures 1, 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0, S_1$ to Output	1.40	2.60	1.40	2.60	1.50	2.70	ns	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_2, S_3$ to Output	1.00	2.00	1.00	2.00	1.10	2.20	ns	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	
$t_{S-G-G}$	Skew Gate to Gate		TBD		TBD		TBD	PS	PCC Only (Note 1)

**Note 1:** Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

## Military Version—Preliminary

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3
		-1085	-870	mV	$-55^\circ C$			
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3
		-1830	-1555	mV	$-55^\circ C$			
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3
		-1085		mV	$-55^\circ C$			
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with $50\Omega$ to $-2.0V$	1, 2, 3
			-1555	mV	$-55^\circ C$			
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for All Inputs		1, 2, 3, 4
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for All Inputs		1, 2, 3, 4
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$	1, 2, 3	

## Military Version—Preliminary (Continued)

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$I_{IH}$	Input HIGH Current		300	$\mu A$	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	1, 2, 3
			450	$\mu A$	$-55^\circ C$		
$I_{EE}$	Power Supply Current	-95	-35	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open	1, 2, 3

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups, 1, 2, 3, 7 and 8.

**Note 3:** Sampled tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7 and 8.

**Note 4:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

### Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = 25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_0-I_{15}$ to Output	0.50	2.60	0.60	2.40	0.60	2.80	ns	Figures 1, 2	1, 2, 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0, S_1$ to Output	0.70	3.30	0.90	3.10	1.00	3.50	ns		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_2, S_3$ to Output	0.50	2.90	0.70	2.60	0.60	3.00	ns		
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.20	1.20	0.20	1.20	0.20	1.20	ns		4

### Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I_0-I_{15}$ to Output	0.50	2.60	0.60	2.40	0.60	2.80	ns	Figures 1, 2	1, 2, 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0, S_1$ to Output	0.70	3.30	0.90	3.10	1.00	3.50	ns		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_2, S_3$ to Output	0.50	2.90	0.70	2.60	0.60	3.00	ns		
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.20	1.20	0.20	1.20	0.20	1.20	ns		4

**Note 1:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 2:** Screen tested 100% on each device at  $+25^\circ C$ , temperature only, Subgroup A9.

**Note 3:** Sample tested (Method 5005, Table I) on each Mfg. lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$ , and  $-55^\circ C$  temp., Subgroups A10 and A11.

**Note 4:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$  and  $-55^\circ C$  temperature (design characterization data).

## Test Circuit

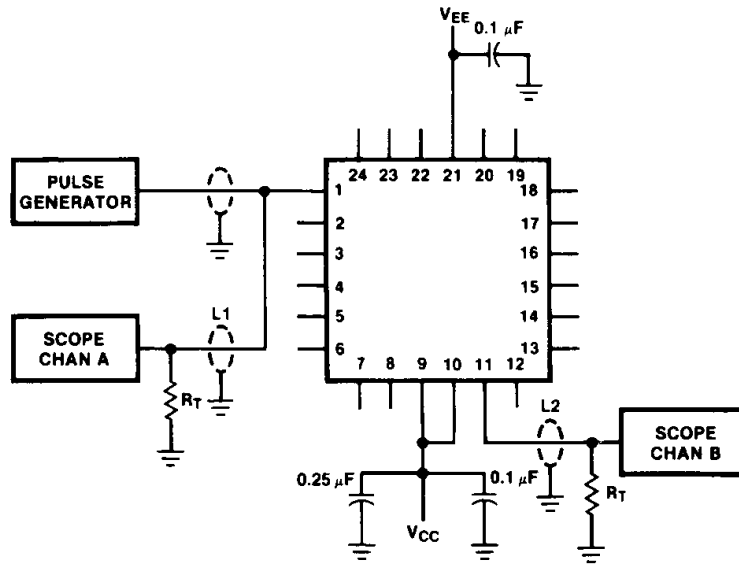


FIGURE 1. AC Test Circuit

TL/F/10265-6

## Switching Waveforms

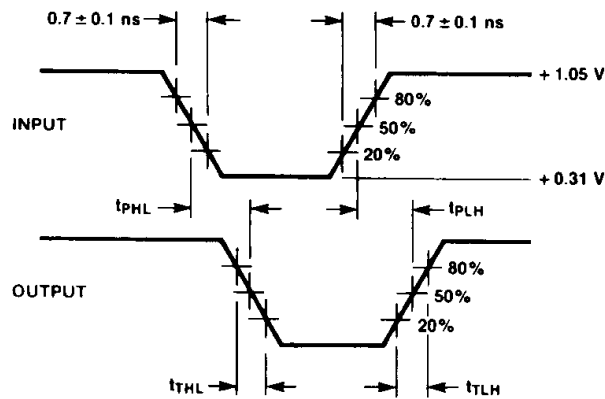


FIGURE 2. Propagation Delay and Transition Times

TL/F/10265-7

### Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = Equal length 50Ω impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling 0.1 μF from GND to  $V_{CC}$  and  $V_{EE}$

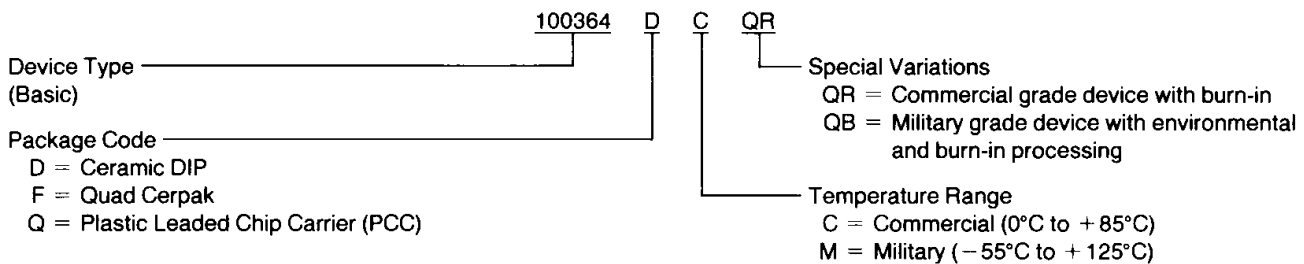
All unused outputs are loaded with 50Ω to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

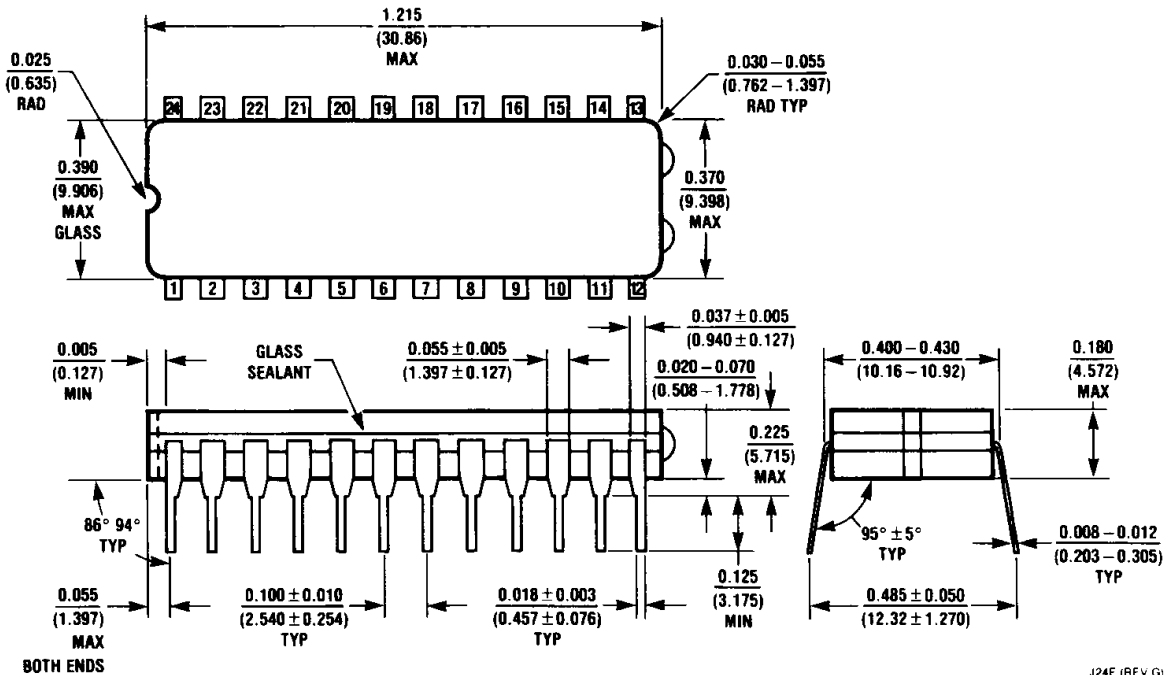
Pin numbers shown are for flatpak; for DIP see logic symbol

## Ordering Information

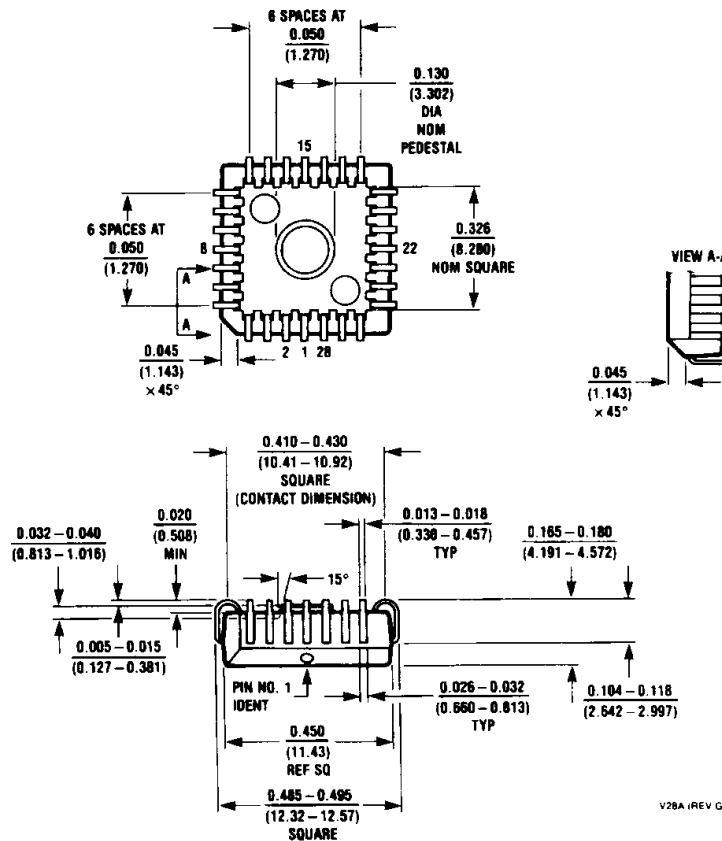
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



**Physical Dimensions** inches (millimeters)



**24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)**  
NS Package Number J24E

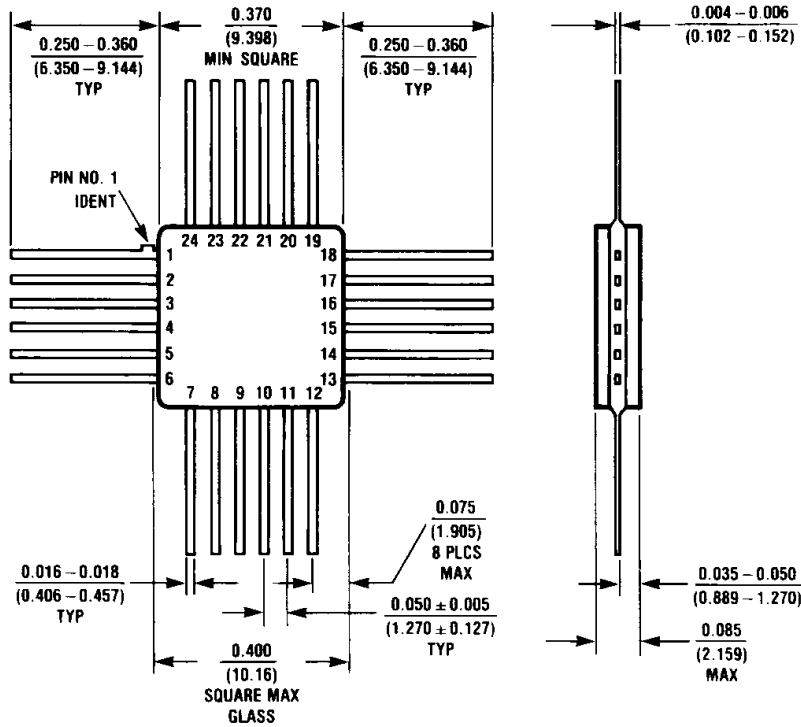


**28-Lead Plastic Chip Carrier (Q)**  
NS Package Number V28A

**Note:** Pedestal as shown on base is not available for F100K ECL products.

**Physical Dimensions** inches (millimeters) (Continued)

Lit. # 114925



W24B (REV C)

**24-Lead Quad Cerpak (F)  
NS Package Number W24B**

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