

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89870 Series

MB89875/P875/PV870

■ DESCRIPTION

The MB89870 series is a line of single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, timers, a PWM timer, a serial interface, an A/D converter, an external interrupt, an LCD controller/driver, and a watch prescaler.

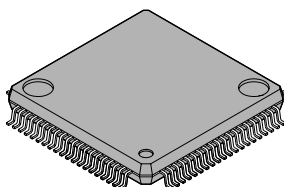
■ FEATURES

- F²MC-8L family CPU core
- Dual-clock control system
- Maximum memory space: 64 Kbytes
- Minimum execution time: 0.4 μ s/10 MHz
- Interrupt processing time: 3.6 μ s/10 MHz
- I/O ports: max. 45 channels
- 21-bit timebase timer
- 8-bit PWM timer: 1 channel, 1 output channel
- 8/16-bit timer/counter: 2 channels (16 bits \times 1 channel)
- 8-bit serial I/O: 1 channel
- 10-bit A/D converter: 8 channels
- OP amp: 4 channels
- External interrupt (wake-up function): 8 channels

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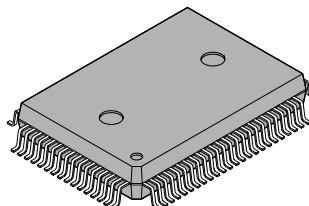
■ PACKAGE

80-pin Plastic LQFP



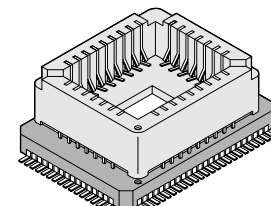
(FPT-80P-M05)

80-pin Plastic QFP



(FPT-80P-M06)

80-pin Ceramic MQFP



(MQP-80C-P01)

MB89870 Series

(Continued)

- Watch prescaler (15 bits)
- LCD controller/driver: 16 to 24 segments × 2 to 4 commons
- Power-on reset function
- Low-power consumption modes (subclock mode, watch mode, sleep mode, and stop mode)
- LQFP-80 (0.50-mm pitch) and QFP-80 (0.80-mm pitch) package

■ PRODUCT LINEUP

| Part number Parameter | MB89875 | MB89P875 | MB89PV870 |
|--------------------------|--|----------------------------------|---|
| Classification | Mass production product (mask ROM product) | One-time PROM product | Piggyback/evaluation product (for development) |
| ROM size | 16 K × 8 bits (internal mask ROM) | 16 K × 8 bits (internal PROM) | 32 K × 8 bits (external ROM) |
| RAM size | 512 × 8 bits | | 1 K × 8 bits |
| LCD display RAM | 12 × 8 bits | | |
| CPU functions | Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 μs/10 MHz to 6.4 μs/10 MHz, 61.0 μs/32.768 kHz Interrupt processing time: 3.6 μs/10 MHz to 57.6 μs/10 MHz, 549.3 μs/32.768 kHz | | |
| Ports | General-purpose I/O ports (CMOS): 45 (42 ports also serve as peripherals and 8 ports are also an N-ch open-drain type.) | | |
| 8-bit PWM timer | 8-bit interval timer operation (square output capable, operating clock cycle: 0.4 μs to 3.3 ms) × 1 channel 7/8-bit resolution PWM operation (conversion cycle: 51.2 μs to 839 ms) × 1 channel | | |
| Timers | 8-bit timer operation (operating clock cycle) × 2 channels 16-bit timer operation (operating clock cycle) × 1 channel | | |
| 8-bit Serial I/O | 8 bits LSB first/MSB first selectable One clock selectable from four operation clocks (one external shift clock, three internal shift clocks: 0.8 μs, 3.2 μs, 12.8 μs) | | |
| LCD controller | 24 segments × 4 commons | | |
| 10-bit A/D converter | 10-bit resolution × 8 channels A/D conversion mode (conversion time: 13.2 μs) Sense mode (conversion time: 7.2 μs) | | |
| OP amps | 4 channels The output can be used for A/D converter input. | | |

(Continued)

MB89870 Series

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| Part number Parameter | MB89875 | MB89P875 | MB89PV870 |
|--------------------------------------|--|----------------|-----------------|
| External interrupt | 8 independent channels (edge selection, interrupt vector, and source flag) Rising edge/falling edge selectable (4 channels) Rising edge/falling edge/both edges selectable (4 channels) Used also for wake-up from stop/sleep mode (Edge detection is also permitted in stop mode.) | | |
| Low-power Consumption (Standby mode) | Subclock mode, sleep mode, watch mode, and stop mode | | |
| Process | CMOS | | |
| Operating voltage* | 2.2 V to 6.0 V | 2.7 V to 6.0 V | |
| EPROM for use | | | MBM27C256A-20TV |

* : Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)

■ PACKAGE AND CORRESPONDING PRODUCTS

| Package | MB89875 MB89P875 | MB89PV870 |
|-------------|---------------------|-----------|
| FPT-80P-M05 | ○ | × |
| FPT-80P-M06 | ○ | × |
| MQP-80C-P01 | × | ○ |

○ : Available × : Not available

Note: For more information about each package, see section “■ Package Dimensions.”

MB89870 Series

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89PV870, the program area starts from address 8006_H but on the MB89P875 and MB89875 starts from 8000_H.
(On the MB89P875, addresses BFF0_H to BFF6_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89PV870 and MB89875, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P875.)

2. Current Consumption

- In the case of the MB89PV870, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.
However, the current consumption in sleep/stop modes is the same. (For more information, see sections “■ Electrical Characteristics” and “■ Example Characteristics.”)

3. Mask Options

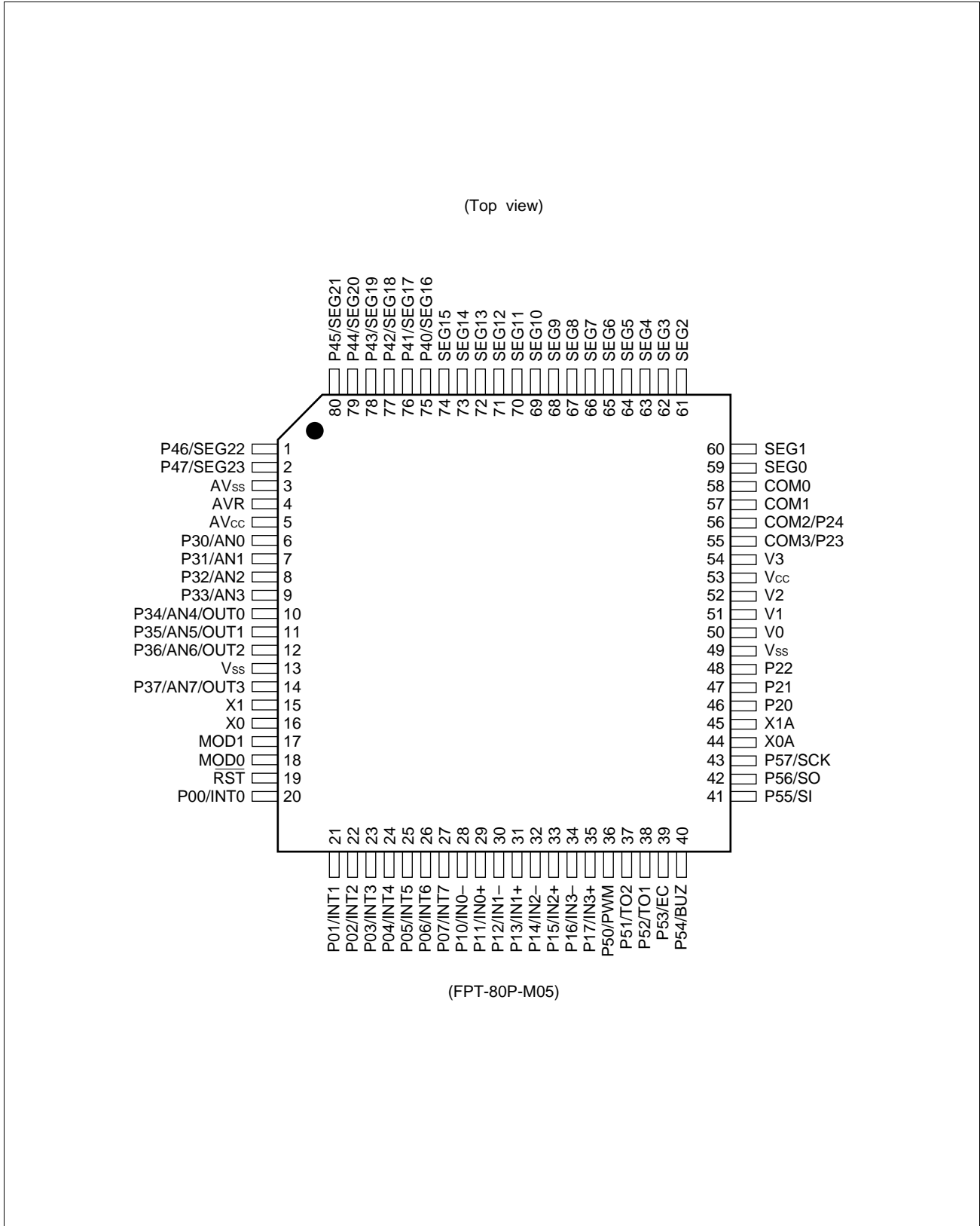
Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section “■ Mask Options.”

Take particular care on the following points:

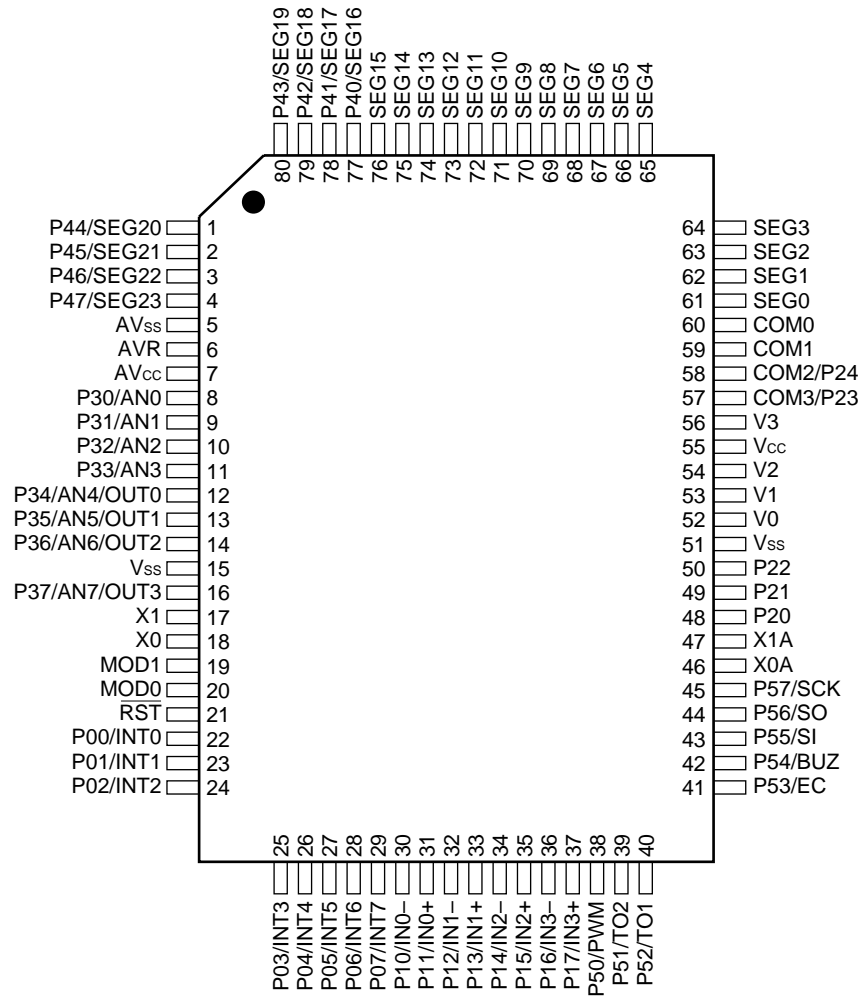
- A pull-up resistor cannot be selectable for P30 to P37 if they are used as the analog input pin for an A/D converter.
- A pull-up resistor cannot be selectable for P10 to P17, and P34 to P37 if an OP amp is used.
- A pull-up resistor is not selectable for P40 to P47 and P23, P24 if they are used as LCD pins.
- Options are fixed on the MB89PV870.

PIN ASSIGNMENT

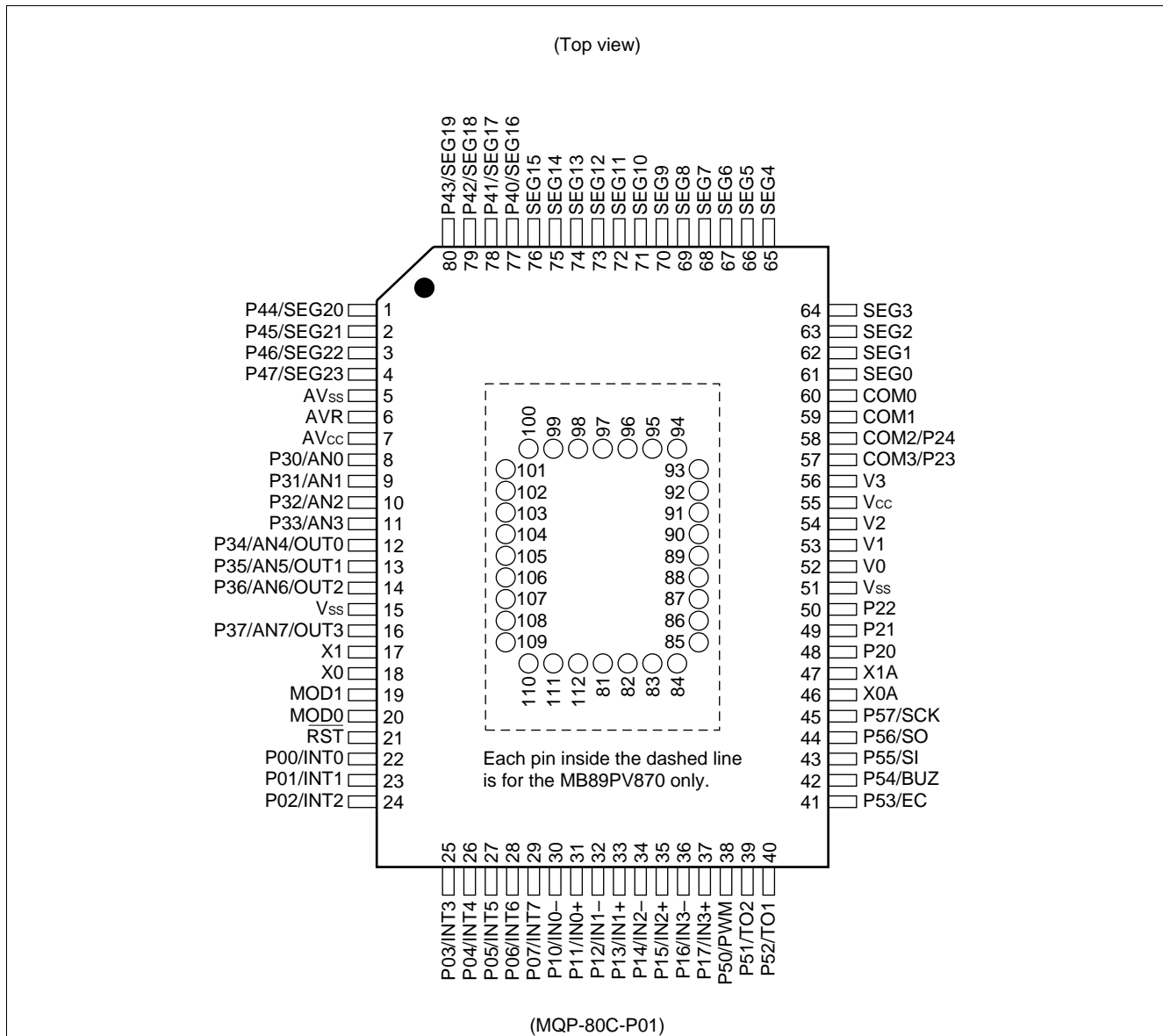


MB89870 Series

(Top view)



(FPT-80P-M06)



• Pin assignment on package top (MB89PV870 only)

| Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 81 | N.C. | 89 | A2 | 97 | N.C. | 105 | \overline{OE} |
| 82 | V _{PP} | 90 | A1 | 98 | O4 | 106 | N.C. |
| 83 | A12 | 91 | A0 | 99 | O5 | 107 | A11 |
| 84 | A7 | 92 | N.C. | 100 | O6 | 108 | A9 |
| 85 | A6 | 93 | O1 | 101 | O7 | 109 | A8 |
| 86 | A5 | 94 | O2 | 102 | O8 | 110 | A13 |
| 87 | A4 | 95 | O3 | 103 | \overline{CE} | 111 | A14 |
| 88 | A3 | 96 | V _{SS} | 104 | A10 | 112 | V _{CC} |

N.C.: Internally connected. Do not use.

MB89870 Series

■ PIN DESCRIPTION

| Pin no. | | Pin name | Circuit type | Function |
|---|---|---|--------------|---|
| LQFP ^{*1} | QFP ^{*2} MQFP ^{*3} | | | |
| 15 | 17 | X1 | A | Main clock crystal oscillator pins (max. 10 MHz) |
| 16 | 18 | X0 | | |
| 44 | 46 | X0A | B | Subclock crystal oscillator pins (32.768 kHz) |
| 45 | 47 | X1A | | |
| 17 | 19 | MOD1 | C | Operating mode selection pins Connect to V _{SS} (GND) when using. |
| 18 | 20 | MOD0 | | |
| 19 | 21 | $\overline{\text{RST}}$ | J | Reset I/O pin “L” is output from this pin by an internal source. The internal circuit is initialized by the input of “L”. |
| 20 to 27 | 22 to 29 | P00/INT0 to P07/INT7 | D | General-purpose I/O ports Also serve as an external interrupt input (wake-up function). External interrupt input is hysteresis input. |
| 28, 29, 30, 31, 32, 33, 34, 35 | 30, 31, 32, 33, 34, 35, 36, 37 | P10/IN0–, P11/IN0+, P12/IN1–, P13/IN1+, P14/IN2–, P15/IN2+, P16/IN3–, P17/IN3+ | E | General-purpose I/O ports Also serve as the input for the OP amp |
| 46 to 48 | 48 to 50 | P20 to P22 | F | General-purpose I/O ports |
| 6 to 9 | 8 to 11 | P30/AN0 to P33/AN3 | E | General-purpose I/O ports Also serve as the input for the A/D converter. |
| 10 to 14 | 12 to 16 | P34/AN4/OUT0 to P37/AN7/OUT3 | G | General-purpose I/O ports Also serve as the A/D converter input and the output for the OP amp. |
| 75 to 80, 1,2 | 77 to 80, 1 to 4 | P40/SEG16 to P47/SEG23 | H | General-purpose I/O ports Also serve as an LCD controller/driver segment output. |
| 36 | 38 | P50/PWM | F | General-purpose I/O port The output type can be switched between N-ch open-drain and CMOS. Also serves as an 8-bit PWM timer. |
| 37, 38, 39 | 39, 40, 41 | P51/TO2, P52/TO1, P53/EC | F | General-purpose I/O ports The output type can be switched between N-ch open-drain and CMOS. Also serves as an 8/16-bit timer/counter. |

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: MQP-80C-P01

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MB89870 Series

(Continued)

| Pin no. | | Pin name | Circuit type | Function |
|--------------------|---|-------------------------------|--------------|---|
| LQFP ^{*1} | QFP ^{*2} MQFP ^{*3} | | | |
| 40 | 42 | P54/BUZ | F | General-purpose I/O port The output type can be switched between N-ch open-drain and CMOS. Also serves as a buzzer output. |
| 41, 42, 43 | 43, 44, 45 | P55/SI, P56/SO, P57/SCK | F | General-purpose I/O ports The output type can be switched between N-ch open-drain and CMOS. Also serve as an 8-bit serial I/O. |
| 59 to 74 | 61 to 76 | SEG15 to SEG0 | I | LCD controller/driver segment output pins |
| 58, 57 | 60, 59 | COM0, COM1 | I | LCD controller/driver common output pins |
| 56, 55 | 58, 57 | COM2/P24, COM3/P23 | H | LCD controller/driver common output pins These pins can be used as general-purpose I/O ports when they are not used as common output pins. |
| 50 to 54 | 52 to 56 | V3 to V0 | — | LCD driving power supply pins |
| 5 | 7 | AV _{CC} | — | A/D converter and OP amp power supply pin |
| 4 | 6 | AV _R | — | A/D converter reference voltage input pin |
| 3 | 5 | AV _{SS} | — | A/D converter and OP amp power supply (GND) pin |
| 53 | 55 | V _{CC} | — | Power supply pin |
| 13, 49 | 15, 51 | V _{SS} | — | Power supply (GND) pins |

*1: FPT-80P-M05

*2: FPT-80P-M06

*3: MQP-80C-P01

MB89870 Series

• External EPROM pins (MB89PV870 only)

| Pin no. | Pin name | I/O | Function |
|---------|-----------------|-----|--|
| 82 | V _{PP} | O | "H" level output pin |
| 83 | A12 | O | Address output pins |
| 84 | A7 | | |
| 85 | A6 | | |
| 86 | A5 | | |
| 87 | A4 | | |
| 88 | A3 | | |
| 89 | A2 | | |
| 90 | A1 | | |
| 91 | A0 | | |
| 93 | O1 | I | Data input pins |
| 94 | O2 | | |
| 95 | O3 | | |
| 96 | V _{SS} | O | Power supply (GND) pin |
| 98 | O4 | I | Data input pins |
| 99 | O5 | | |
| 100 | O6 | | |
| 101 | O7 | | |
| 102 | O8 | | |
| 103 | \overline{CE} | | |
| 104 | A10 | O | Address output pin |
| 105 | \overline{OE} | O | ROM output enable pin Outputs "L" at all times. |
| 107 | A11 | O | Address output pins |
| 108 | A9 | | |
| 109 | A8 | | |
| 110 | A13 | | |
| 111 | A14 | O | |
| 112 | V _{CC} | O | EPROM power supply pin |
| 81 | N.C. | — | Internally connected pins Be sure to leave them open. |
| 92 | | | |
| 97 | | | |
| 106 | | | |

■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|----------------------------------|--|
| A | <p>Main clock control signal</p> | <p>Main clock</p> <ul style="list-style-type: none"> At an oscillation feedback resistor of approximately 1 MΩ/5.0 V |
| B | <p>Subclock control signal</p> | <p>Subclock</p> <ul style="list-style-type: none"> At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V |
| C | | <ul style="list-style-type: none"> CMOS hysteresis input |
| D | | <ul style="list-style-type: none"> CMOS I/O (when selected as general-purpose ports) Hysteresis input (when selected as an external interrupt input) Pull-up resistor optional at approximately 50 kΩ/5.0 V |
| E | <p>Analog input</p> | <ul style="list-style-type: none"> Analog input CMOS I/O (when selected as general-purpose ports) Pull-up resistor optional at approximately 50 kΩ/5.0 V |

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MB89870 Series

(Continued)

| Type | Circuit | Remarks |
|------|---------|---|
| F | | <ul style="list-style-type: none"> • CMOS I/O (when selected as general-purpose ports) • P50 to P57 are output only and can be switched between CMOS output and N-ch open-drain output. • Pull-up resistor optional at approximately 50 kΩ/5.0 V |
| G | | <ul style="list-style-type: none"> • Analog input • Analog output • CMOS I/O (when selected as general-purpose ports) • Pull-up resistor optional at approximately 50 kΩ/5.0 V |
| H | | <ul style="list-style-type: none"> • LCD controller/driver output • CMOS I/O (when selected as general-purpose ports) • Pull-up resistor optional at approximately 50 kΩ/5.0 V |
| I | | <ul style="list-style-type: none"> • LCD controller/driver output |
| J | | <ul style="list-style-type: none"> • At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • CMOS hysteresis input |

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS} .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be $AV_{CC} = DAVC = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

MB89870 Series

PROGRAMMING TO THE EPROM ON THE MB89P875

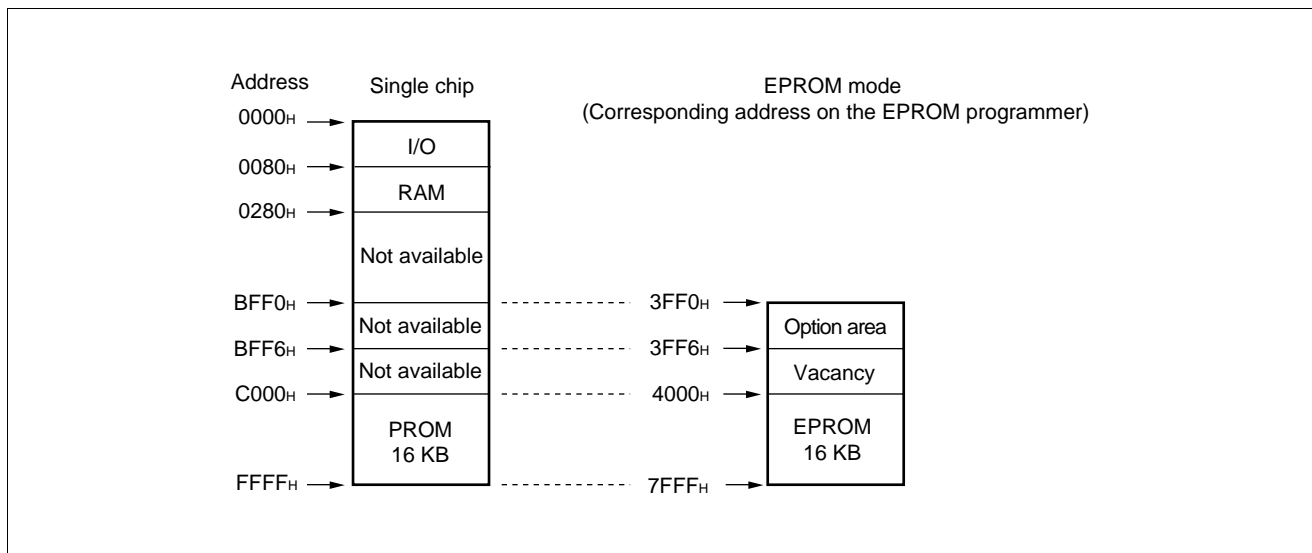
The MB89P875 is an OTPROM version of the MB89870 series.

1. Features

- 16-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in each mode such as 16-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

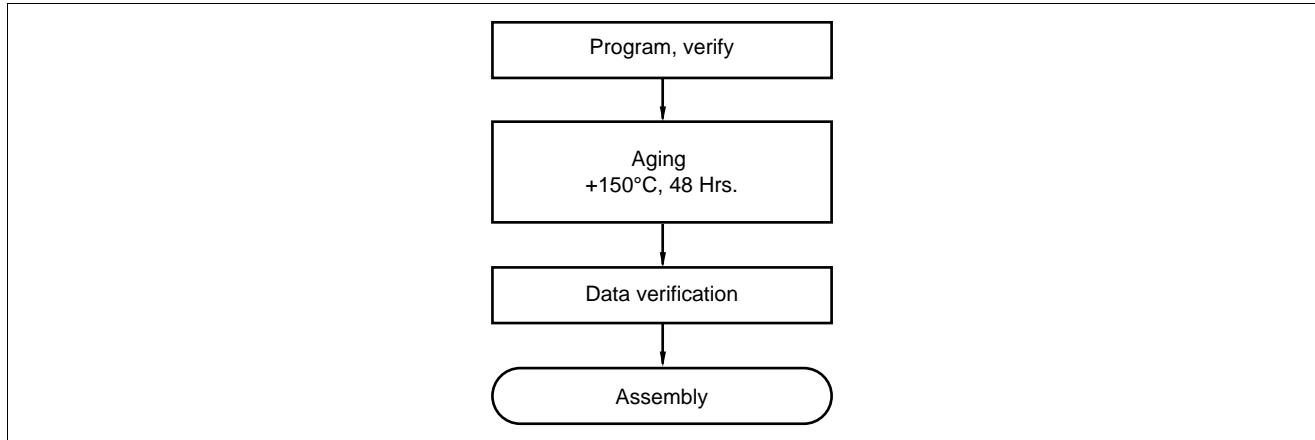
In EPROM mode, the MB89P875 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter. When the operating ROM area for a single chip is 16 Kbytes (C000H to FFFFH) the PROM can be programmed as follows:

• Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 4000H to 7FFFH (note that addresses C000H to FFFFH while operating as a single chip assign to 4000H to 7FFFH in EPROM mode). Load option data into addresses 3FF0H to 3FF6H of the EPROM programmer. (For information about each corresponding option, see "7. Setting OTPROM Options.")
- (3) Program to 3FF0H to 7FFFH with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

| Part No. | Package | Compatible socket adapter Sun Hayato Co., Ltd. | Recommended programmer manufacturer and programmer name | |
|-------------|---------|---|--|-----------------|
| | | | Minato Electronics Inc. | Advantest Corp. |
| | | | 1890A | R4945A |
| MB89P875PFV | LQFP-80 | ROM-80SQF-28DP-8L | Recommended | Recommended |
| MB89P875PF | QFP-80 | ROM-80QF-28DP-8L3 | Recommended | Recommended |

Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403

FAX (81)-3-5396-9106

Minato Electronics Inc.: TEL: USA (1)-916-348-6066

JAPAN (81)-45-591-5611

Advantest Corp.: TEL: Except JAPAN (81)-3-3930-4111

MB89870 Series

7. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

| Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|--------------------------------|--------------------------------|---------------------------------------|--|-------------------------------------|-------------------------------------|--|---|
| 3FF0 _H | Vacancy | Vacancy | Vacancy | Single/dual-clock system 1: Dual clock 0: Single clock | Reset pin output 1: Yes 0: No | Power-on reset 1: Yes 0: No | Oscillation stabilization time | |
| | Readable and writable | Readable and writable | Readable and writable | | | | 00: 2 ¹⁸ /F _{CH} 01: 2 ¹⁷ /F _{CH} | 10: 2 ¹³ /F _{CH} 11: 0 |
| 3FF1 _H | P07 Pull-up 1: No 0: Yes | P06 Pull-up 1: No 0: Yes | P05 Pull-up 1: No 0: Yes | P04 Pull-up 1: No 0: Yes | P03 Pull-up 1: No 0: Yes | P02 Pull-up 1: No 0: Yes | P01 Pull-up 1: No 0: Yes | P00 Pull-up 1: No 0: Yes |
| 3FF2 _H | Vacancy | Vacancy | P44 to P47 Pull-up 1: No 0: Yes | P40 to P43 Pull-up 1: No 0: Yes | P16, P17 Pull-up 1: No 0: Yes | P14, P15 Pull-up 1: No 0: Yes | P12, P13 Pull-up 1: No 0: Yes | P10, P11 Pull-up 1: No 0: Yes |
| | Readable and writable | Readable and writable | | | | | | |
| 3FF3 _H | P37 Pull-up 1: No 0: Yes | P36 Pull-up 1: No 0: Yes | P35 Pull-up 1: No 0: Yes | P34 Pull-up 1: No 0: Yes | P33 Pull-up 1: No 0: Yes | P32 Pull-up 1: No 0: Yes | P31 Pull-up 1: No 0: Yes | P30 Pull-up 1: No 0: Yes |
| 3FF4 _H | P57 Pull-up 1: No 0: Yes | P56 Pull-up 1: No 0: Yes | P55 Pull-up 1: No 0: Yes | P54 Pull-up 1: No 0: Yes | P53 Pull-up 1: No 0: Yes | P52 Pull-up 1: No 0: Yes | P51 Pull-up 1: No 0: Yes | P50 Pull-up 1: No 0: Yes |
| 3FF5 _H | Vacancy | Vacancy | Vacancy | P24 Pull-up 1: No 0: Yes | P23 Pull-up 1: No 0: Yes | P22 Pull-up 1: No 0: Yes | P21 Pull-up 1: No 0: Yes | P20 Pull-up 1: No 0: Yes |
| | Readable and writable | Readable and writable | Readable and writable | | | | | |
| 3FF6 _H | Vacancy | Vacancy | Vacancy | Vacancy | Vacancy | Vacancy | Vacancy | Reserved bit |
| | Readable and writable | Readable and writable | Readable and writable | Readable and writable | Readable and writable | Readable and writable | Readable and writable | Readable and writable |

Note: Each bit is set to '1' as the initialized value.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

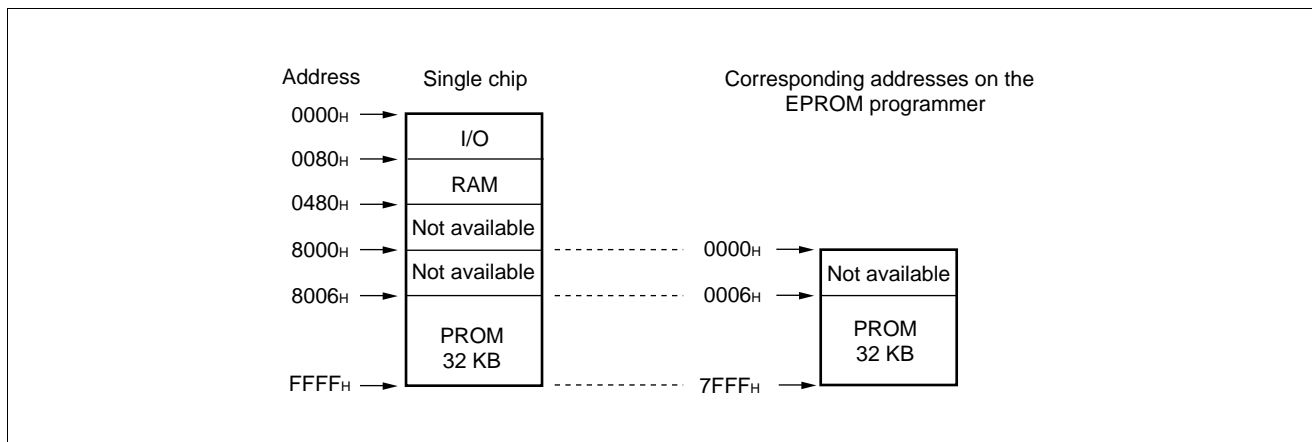
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

| Package | Compatible socket part number |
|--------------------|-------------------------------|
| LCC-32 (Rectangle) | ROM-32LC-28DP-YG |
| LCC-32 (Square) | ROM-32LC-28DP-S |

Inquiry: Sun Hayato Co., Ltd.: TEL (81)-3-3986-0403
FAX (81)-3-5396-9106

3. Memory Space

Memory space in 32-Kbyte PROM is diagrammed below.

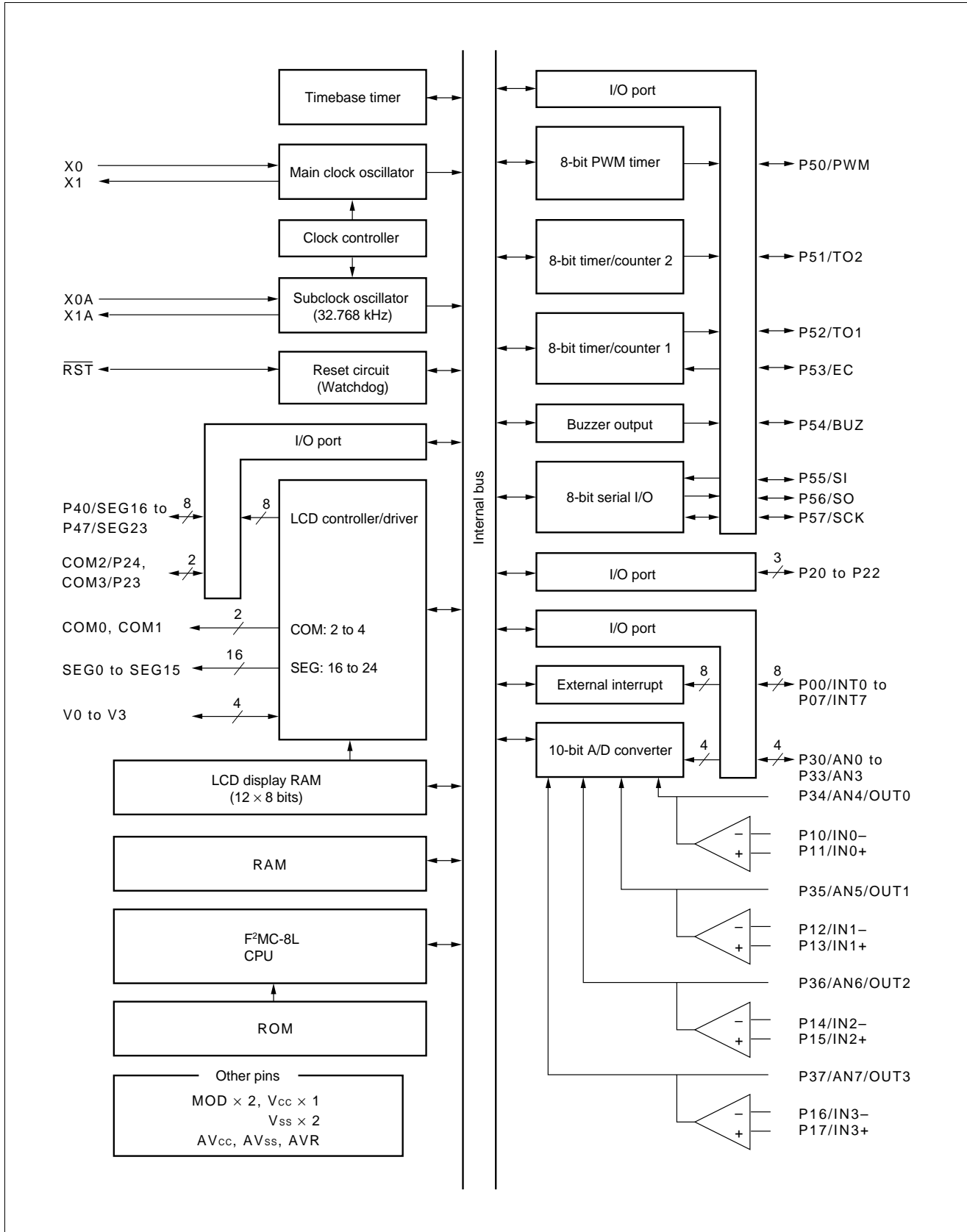


4. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0006H to 7FFFH.
- (3) Program to 0000H to 7FFFH with the EPROM programmer.

MB89870 Series

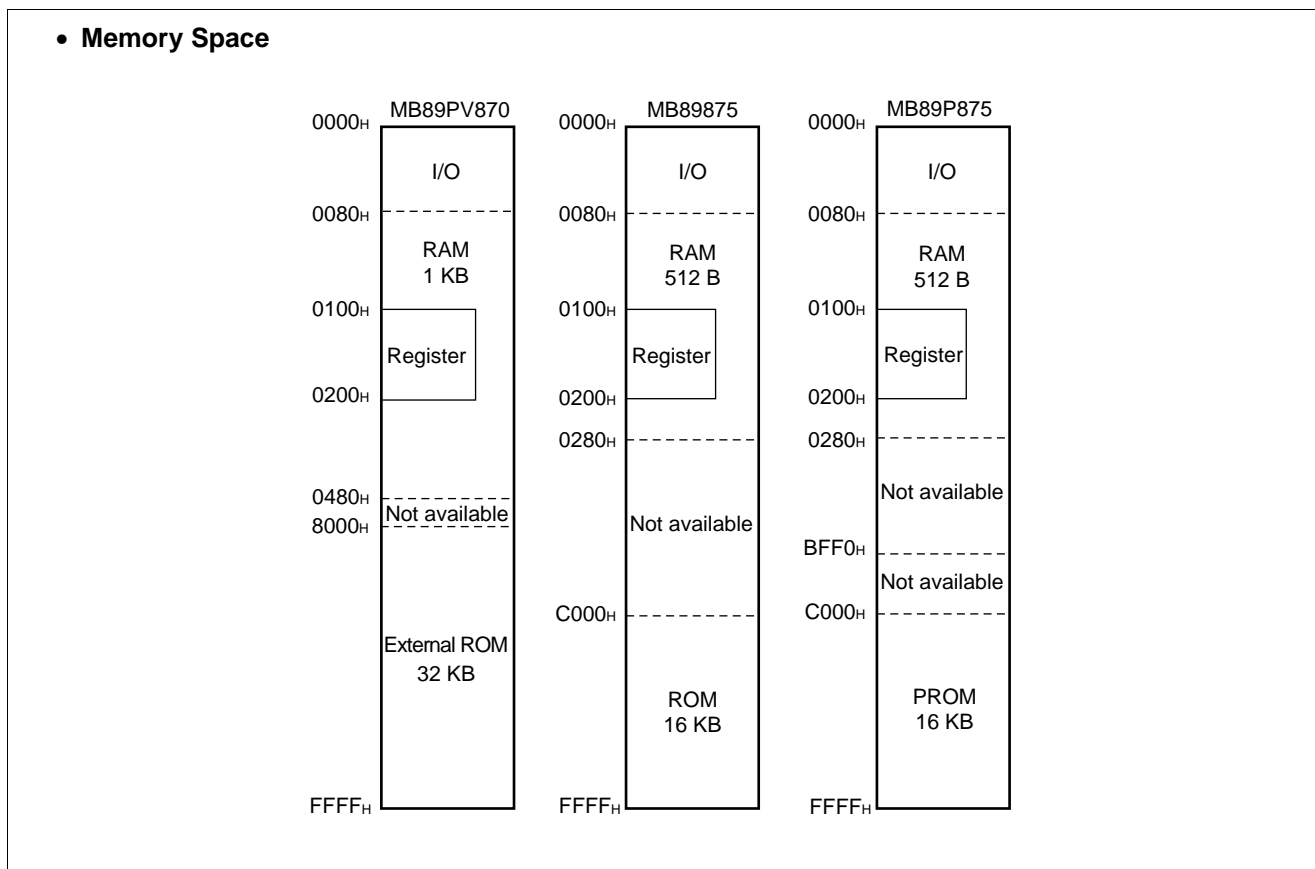
■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

The microcontrollers of the MB89870 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89870 series is structured as illustrated below.

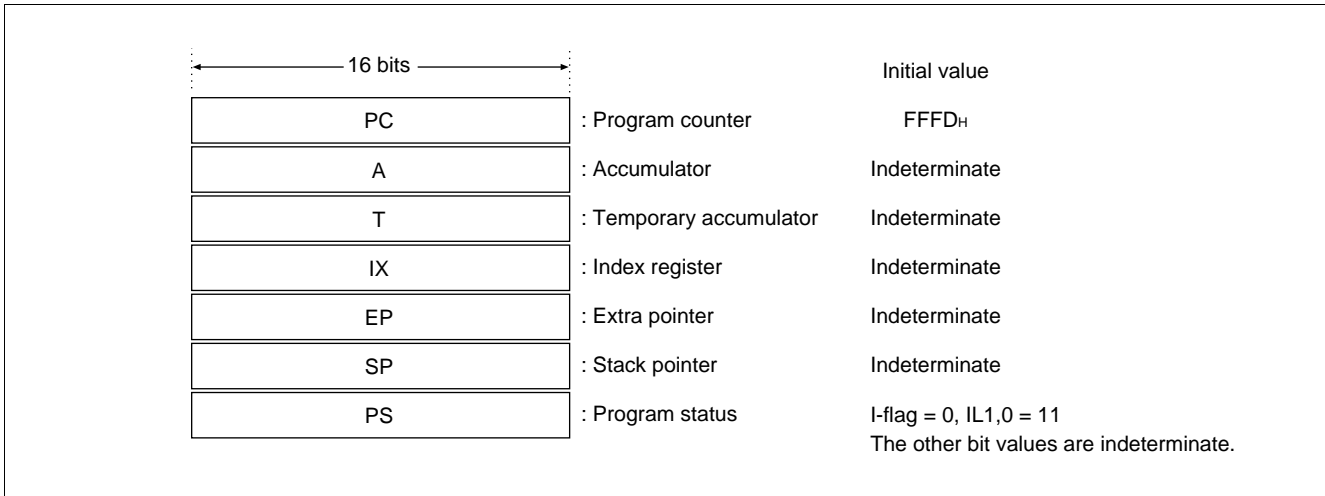


MB89870 Series

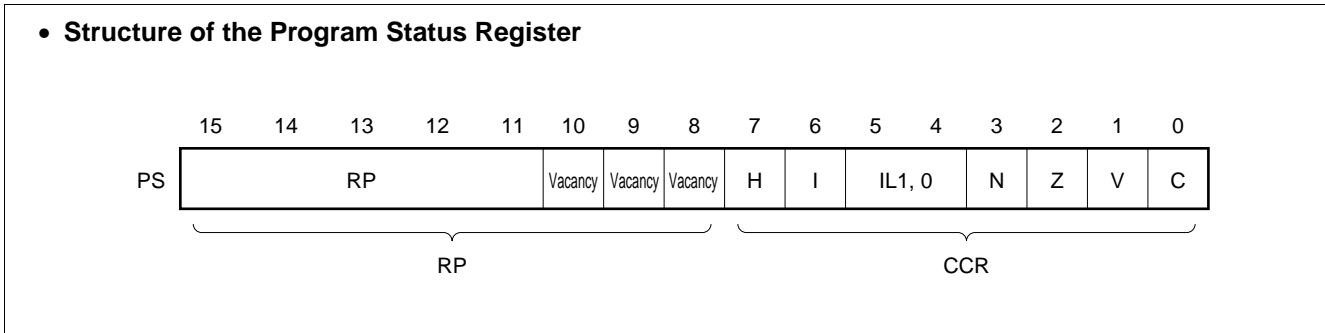
2. Registers

The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

- Program counter (PC): A 16-bit register for indicating instruction storage positions
- Accumulator (A): A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T): A 16-bit register which performs arithmetic operations with the accumulator
When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX): A 16-bit register for index modification
- Extra pointer (EP): A 16-bit pointer for indicating a memory address
- Stack pointer (SP): A 16-bit register for indicating a stack area
- Program status (PS): A 16-bit register for storing a register pointer, a condition code

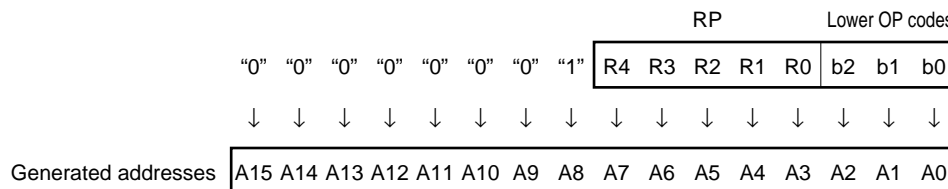


The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

• **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

| IL1 | IL0 | Interrupt level | High-low |
|-----|-----|-----------------|----------|
| 0 | 0 | 1 | High |
| 0 | 1 | | ↑ |
| 1 | 0 | 2 | ↓ |
| 1 | 1 | 3 | |

N-flag: Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to the shift-out value in the case of a shift instruction.

MB89870 Series

The following general-purpose registers are provided:

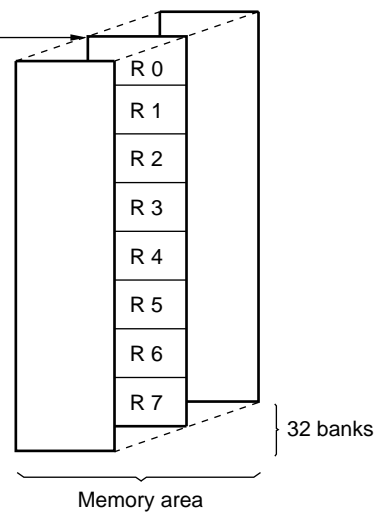
General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89875 (RAM 512×8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

• Register Bank Configuraiton

This address = $0100_{\text{H}} + 8 \times (\text{RP})$



■ I/O MAP

| Address | Read/write | Register name | Register description |
|---------|------------|---------------|----------------------------------|
| 00H | R/W | PDR0 | Port 0 data register |
| 01H | W | DDR0 | Port 0 data direction register |
| 02H | R/W | PDR1 | Port 1 data register |
| 03H | W | DDR1 | Port 1 data direction register |
| 04H | R/W | PDR2 | Port 2 data register |
| 05H | R/W | DDR2 | Port 2 data direction register |
| 06H | | | Vacancy |
| 07H | R/W | SCC | System clock control register |
| 08H | R/W | SMC | Standby control register |
| 09H | R/W | WDTE | Watchdog timer control register |
| 0AH | R/W | TBCR | Timebase timer control register |
| 0BH | R/W | WCR | Watch prescaler control register |
| 0CH | R/W | PDR3 | Port 3 data register |
| 0DH | R/W | DDR3 | Port 3 data direction register |
| 0EH | R/W | PDR4 | Port 4 data register |
| 0FH | R/W | DDR4 | Port 4 data direction register |
| 10H | | | Vacancy |
| 11H | | | Vacancy |
| 12H | | | Vacancy |
| 13H | | | Vacancy |
| 14H | | | Vacancy |
| 15H | | | Vacancy |
| 16H | R/W | PDR5 | Port 5 data register |
| 17H | R/W | DDR5 | Port 5 data direction register |
| 18H | | | Vacancy |
| 19H | | | Vacancy |
| 1AH | R/W | CHG5 | Port 5 switching register |
| 1BH | | | Vacancy |
| 1CH | | | Vacancy |
| 1DH | W | ICR3 | Port 3 input control register |
| 1EH | R/W | CNTR | PWM control register |
| 1FH | W | COMP | PWM compare register |

(Continued)

MB89870 Series

(Continued)

| Address | Read/write | Register name | Register description |
|------------------------------------|------------|---------------|--|
| 20 _H | | | Vacancy |
| 21 _H | | | Vacancy |
| 22 _H | | | Vacancy |
| 23 _H | | | Vacancy |
| 24 _H | R/W | T2CR | Timer 2 control register |
| 25 _H | R/W | T1CR | Timer 1 control register |
| 26 _H | R/W | T2DR | Timer 2 data register |
| 27 _H | R/W | T1DR | Timer 1 data register |
| 28 _H | R/W | SMR | Serial mode register |
| 29 _H | R/W | SDR | Serial data register |
| 2A _H | | | Vacancy |
| 2B _H | | | Vacancy |
| 2C _H | R/W | OPC | OP amp control register |
| 2D _H | R/W | ADC1 | A/D converter control register 1 |
| 2E _H | R/W | ADC2 | A/D converter control register 2 |
| 2F _H | R/W | ADCH | A/D converter data register H |
| 30 _H | R/W | ADCL | A/D converter data register L |
| 31 _H | R/W | EIE1 | External interrupt 1 enable register |
| 32 _H | R/W | EIF1 | External interrupt 1 flag register |
| 33 _H | R/W | EIE2 | External interrupt 2 enable register |
| 34 _H to 5F _H | | | Vacancy |
| 60 _H to 6B _H | R/W | VRAM | Display data RAM |
| 6C _H to 6F _H | | | Vacancy |
| 70 _H | R/W | LCR1 | LCD controller/driver control register 1 |
| 71 _H | R/W | LCR2 | LCD controller/driver control register 2 |
| 72 _H to 7B _H | | | Vacancy |
| 7C _H | W | ILR1 | Interrupt level setting register 1 |
| 7D _H | W | ILR2 | Interrupt level setting register 2 |
| 7E _H | W | ILR3 | Interrupt level setting register 3 |
| 7F _H | | | Vacancy |

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|--|-----------------------|----------------|----------------|------|--|
| | | Min. | Max. | | |
| Power supply voltage | V_{CC} AV_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | * |
| A/D converter reference input voltage | AVR | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | |
| LCD power supply voltage | V0 to V3 | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V | V0 to V3 must not exceed V_{CC} . |
| Input voltage | V_I | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| Output voltage | V_O | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| “L” level maximum output current | I_{OL} | — | 20 | mA | |
| “L” level average output current | I_{OLAV} | — | 4 | mA | Average value (operating current × operating rate) |
| “L” level total maximum output current | ΣI_{OL} | — | 100 | mA | |
| “L” level total average output current | ΣI_{OLAV} | — | 40 | mA | Average value (operating current × operating rate) |
| “H” level maximum output current | I_{OH} | — | -20 | mA | |
| “H” level average output current | I_{OHAV} | — | -4 | mA | Average value (operating current × operating rate) |
| “H” level total maximum output current | ΣI_{OH} | — | -50 | mA | |
| “H” level total average output current | ΣI_{OHAV} | — | -20 | mA | Average value (operating current × operating rate) |
| Power consumption | P_D | — | 300 | mW | |
| Operating temperature | T_A | -40 | +85 | °C | |
| Storage temperature | T_{stg} | -55 | +150 | °C | |

* : Use AV_{CC} and V_{CC} set at the same voltage.

Take care so that AVR does not exceed $AV_{CC} + 0.3\text{ V}$ and AV_{CC} does not exceed V_{CC} , such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB89870 Series

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks |
|---------------------------------------|-------------------------------------|-----------------|------------------|------|--|
| | | Min. | Max. | | |
| Power supply voltage | V _{CC} AV _{CC} | 2.2* | 6.0* | V | Normal operation assurance range* MB89875 |
| | | 2.7 | 6.0 | V | Normal operation assurance range MB89PV870/P875 |
| | | 1.5 | 6.0 | V | Retains the RAM state in stop mode |
| A/D converter reference input voltage | AVR | 0.0 | AV _{CC} | V | |
| LCD power supply voltage | V0 to V3 | V _{SS} | V _{CC} | V | LCD power supply range (The optimum value is dependent on the LCD element in use.) |
| Operating temperature | T _A | -40 | +85 | °C | |

* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

Figure 1 Operating Voltage vs. Main Clock Operating Frequency

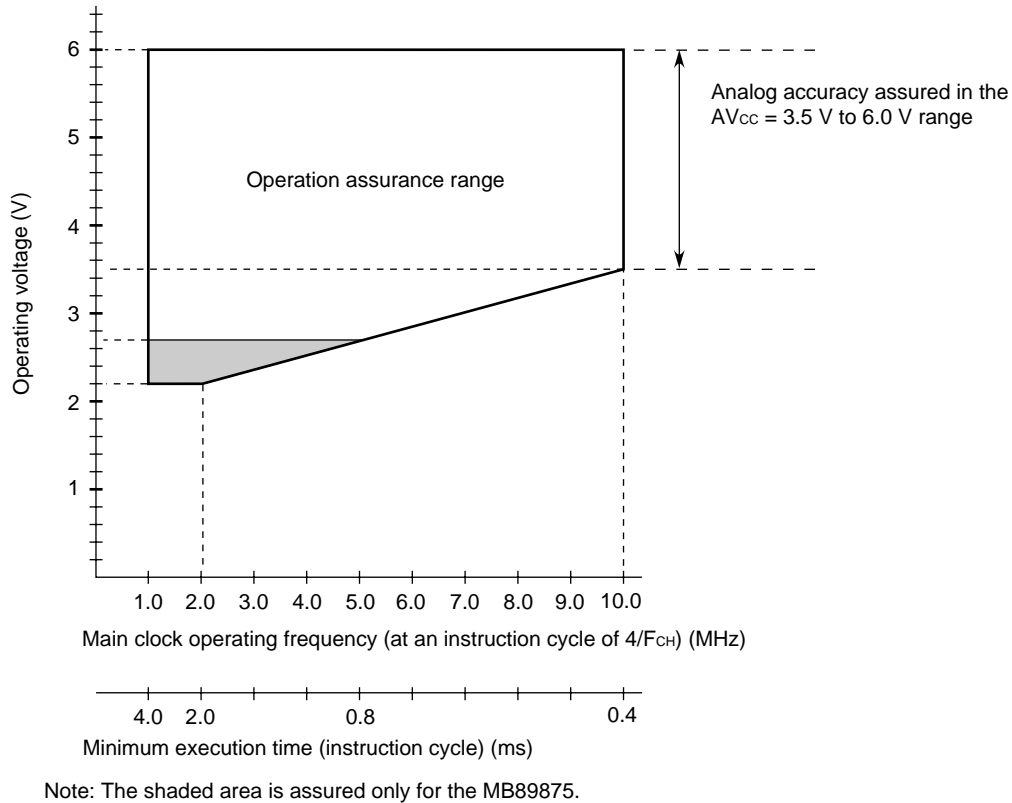


Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

MB89870 Series

3. DC Characteristics

($V_{CC} = V_{CC} = 5.0\text{ V}$, $V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|------------|--|-------------------------------|----------------|------|----------------|------------------|-----------------------|
| | | | | Min. | Typ. | Max. | | |
| “H” level input voltage | V_{IH} | P20 to P24, P30 to P37, P40 to P47, P50 to P52, P54, P56 | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| | V_{IHS} | P00 to P07, P10 to P17, MOD0, MOD1, \overline{RST} , P53, P55, P57 | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| “L” level input voltage | V_{IL} | P20 to P24, P30 to P37, P40 to P47, P50 to P52, P54, P56 | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | |
| | V_{ILS} | P00 to P07, P10 to P17, MOD0, MOD1, \overline{RST} , P53, P55, P57 | — | $V_{SS} - 0.3$ | — | $0.2 V_{CC}$ | V | |
| Open-drain output pin application voltage | V_D | P50 to P57 | — | $V_{SS} - 0.3$ | — | $V_{CC} - 0.3$ | V | N-ch open-drain |
| “H” level output voltage | V_{OH} | P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P57 | $I_{OH} = -2.0\text{ mA}$ | 4.0 | — | — | V | |
| “L” level output voltage | V_{OL} | P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P57 | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | |
| Input leakage current (Hi-Z output leakage current) | I_{LI} | P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P57 MOD0, MOD1, \overline{RST} | $0.0\text{ V} < V_I < V_{CC}$ | — | — | ± 5 | μA | With pull-up resistor |
| Pull-up resistance | R_{PULL} | P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P57 | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | $\text{k}\Omega$ | With pull-up resistor |

(Continued)

MB89870 Series

($AV_{CC} = V_{CC} = 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks | |
|-----------------------------------|------------|---|--|--|------|---------------|------|-------------------|-------------------|
| | | | | Min. | Typ. | Max. | | | |
| Power supply current ¹ | I_{CC1} | V_{CC} | $F_{CH} = 10\text{ MHz}$ $V_{CC} = 5.0\text{ V}$ $t_{inst}^* = 0.4\ \mu\text{s}$ | — | 12 | 20 | mA | | |
| | I_{CC2} | | $F_{CH} = 10\text{ MHz}$ $V_{CC} = 3.0\text{ V}$ $t_{inst}^* = 6.4\ \mu\text{s}$ | — | 1.0 | 2 | mA | MB89875/ PV870 | |
| | | | | | — | 1.5 | 2.5 | mA | MB89P875 |
| | I_{CCS1} | | Sleep mode | $F_{CH} = 10\text{ MHz}$ $V_{CC} = 5.0\text{ V}$ $t_{inst}^* = 0.4\ \mu\text{s}$ | — | 3 | 7 | mA | |
| | | | | $F_{CH} = 10\text{ MHz}$ $V_{CC} = 3.0\text{ V}$ $t_{inst}^* = 6.4\ \mu\text{s}$ | — | 0.5 | 1.5 | mA | |
| | I_{CCL} | | Subclock mode | $F_{CL} = 32.768\text{ kHz}$, $V_{CC} = 3.0\text{ V}$ | — | 50 | 100 | μA | MB89875/ PV870 |
| | | | | | — | 500 | 700 | μA | MB89P875 |
| | I_{CCLS} | | Subclock sleep mode | $F_{CL} = 32.768\text{ kHz}$, $V_{CC} = 3.0\text{ V}$ | — | 15 | 50 | μA | |
| | I_{CCT} | | | $F_{CL} = 32.768\text{ kHz}$, $V_{CC} = 3.0\text{ V}$ • Watch mode • Main clock stop mode at dual-clock system | — | 3 | 15 | μA | |
| | I_{CCH} | | | $T_A = +25^\circ\text{C}$ • Subclock stop mode • Main clock stop mode at single-clock system | — | — | 1 | μA | |
| I_A | AV_{CC} | $F_{CH} = 10\text{ MHz}$, when A/D conversion is activated | — | 1.5 | 3 | mA | | | |
| I_{AH} | | $F_{CH} = 10\text{ MHz}$, $T_A = +25^\circ\text{C}$, when A/D conversion is stopped | — | — | 1 | μA | | | |

(Continued)

MB89870 Series

(Continued)

($AV_{CC} = V_{CC} = 5.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---------------------------------------|------------|---|---|-------|------|---------|---------------|---------|
| | | | | Min. | Typ. | Max. | | |
| LCD divided resistance | R_{LCD} | — | Between V_{CC} and V_0 at $V_{CC} = 5.0\text{ V}$ | 300 | 500 | 750 | $k\Omega$ | |
| COM0 to 3 output impedance | R_{VCOM} | COM0 to 3 | V_1 to $V_3 = 5.0\text{ V}$ | — | — | 2.5 | $k\Omega$ | |
| SEG0 to 24 output impedance | R_{VSEG} | SEG0 to 24 | | — | — | 15 | $k\Omega$ | |
| LCD controller/driver leakage current | I_{LCDL} | V_0 to V_3 , COM0 to 3 SEG0 to SEG24 | — | — | — | ± 1 | μA | |
| Input capacitance | C_{IN} | Other than AV_{CC} , AV_{SS} , V_{CC} , and V_{SS} | $f = 1\text{ MHz}$ | — | 10 | — | pF | |

*1: The power supply current is measured at the external clock.

*2: For information on t_{inst} , see “(4) Instruction Cycle” in “4. AC Characteristics.”

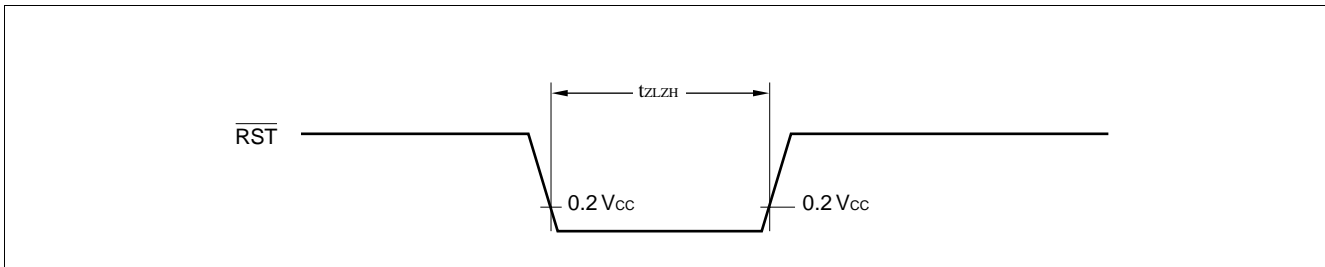
Note: For pins which serve as the LCD and ports (P23, P24 and P40 to P47), see the port parameter when these pins are used as ports and the LCD parameter when they are used as LCD pins.

4. AC Characteristics

(1) Reset Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|------------------|-----------|----------------------|------|------|---------|
| | | | Min. | Max. | | |
| $\overline{\text{RST}}$ "L" pulse width | t_{LZH} | — | 48 t_{HCYL} | — | ns | |



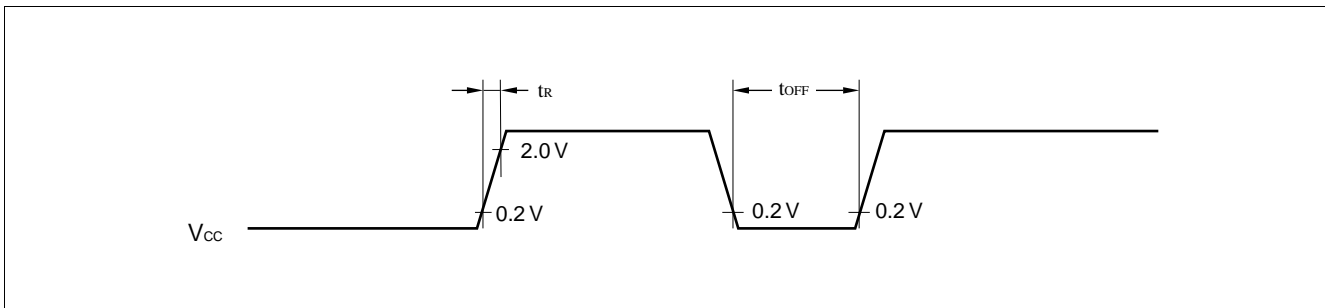
(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|--------------------------|------------------|-----------|-------|------|------|------------------------------|
| | | | Min. | Max. | | |
| Power supply rising time | t_{r} | — | — | 50 | ms | Power-on reset function only |
| Power supply cutoff time | t_{OFF} | | 1 | — | | |

Note: Make sure that power supply rises within the selected oscillation stabilization time.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



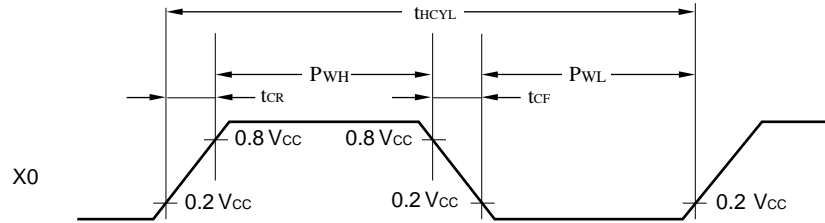
MB89870 Series

(3) Clock Timing

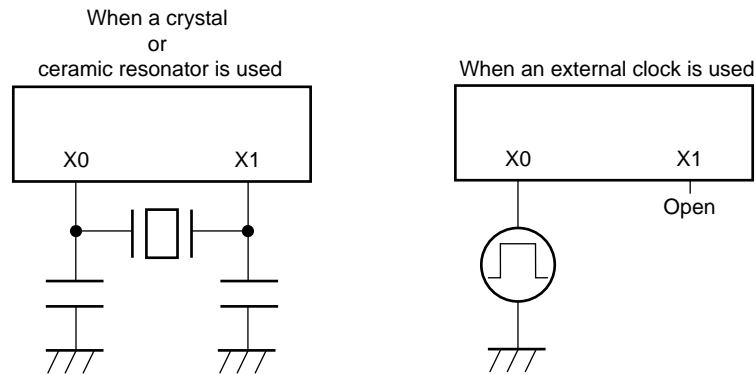
($V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-------------------------|------------------------------------|----------|-----------|-------|--------|------|------|----------------|
| | | | | Min. | Typ. | Max. | | |
| Clock frequency | F _{CH} | X0, X1 | — | 1 | — | 10 | MHz | |
| | F _{CL} | X0A, X1A | | — | 32.768 | — | kHz | |
| Clock cycle time | t _{H CYL} | X0, X1 | | 100 | — | 1000 | ns | |
| | t _{L CYL} | X0A, X1A | | — | 30.5 | — | μs | |
| Input clock pulse width | P _{WH} P _{WL} | X0 | | 20 | — | — | ns | External clock |
| | t _{CR} t _{CF} | X0 | | — | — | 10 | ns | External clock |

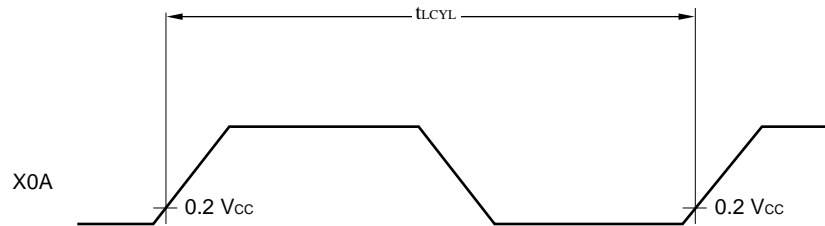
X0 and X1 Timing and Conditions



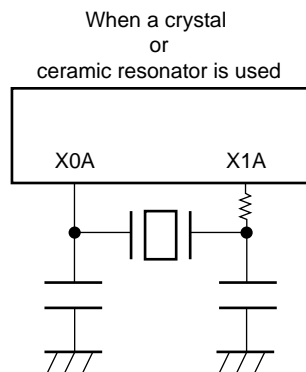
Main Clock Conditions



X0A and X1A Timing and Conditions



Subclock Conditions



MB89870 Series

(4) Instruction Cycle

| Parameter | Symbol | Value (typical) | Unit | Remarks |
|---|------------|---|---------------|---|
| Instruction cycle (minimum execution time) | t_{inst} | $4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$ | μs | $(4/F_{CH}) t_{inst} = 0.4 \mu\text{s}$ when operating at $F_{CH} = 10 \text{ MHz}$ |
| | | $2/F_{CL}$ | μs | $t_{inst} = 61.036 \mu\text{s}$ when operating at $F_{CL} = 32.768 \text{ kHz}$ |

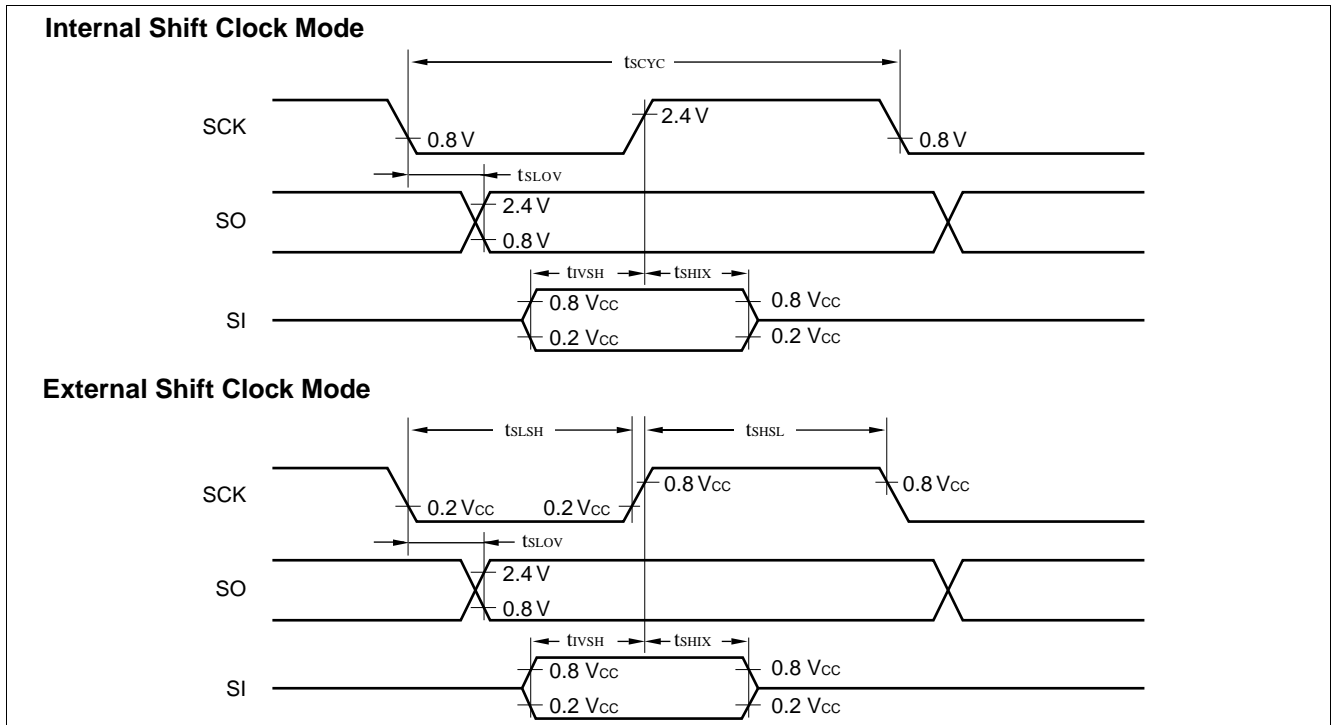
Note: When operating at 10 MHz, the cycle varies with the set execution time.

(5) Serial I/O Timing

($V_{CC} = +5.0 \text{ V} \pm 10\%$, $A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|------------|----------|---------------------------|------------------|------|---------------|---------|
| | | | | Min. | Max. | | |
| Serial clock cycle time | t_{SCYC} | SCK | Internal shift clock mode | $2 t_{inst}^*$ | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK, SO | | -200 | 200 | ns | |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI, SCK | | $1/2 t_{inst}^*$ | — | μs | |
| SCK $\uparrow \rightarrow$ valid SI hold time | t_{SHIX} | SCK, SI | | $1/2 t_{inst}^*$ | — | μs | |
| Serial clock "H" pulse width | t_{SHSL} | SCK | External shift clock mode | $1 t_{inst}^*$ | — | μs | |
| Serial clock "L" pulse width | t_{SLSH} | | | $1 t_{inst}^*$ | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK, SO | | 0 | 200 | ns | |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SI, SCK | | $1/2 t_{inst}^*$ | — | μs | |
| SCK $\uparrow \rightarrow$ valid SI hold time | t_{SHIX} | SCK, SI | | $1/2 t_{inst}^*$ | — | μs | |

* : For information on t_{inst} , see "(4) Instruction Cycle."

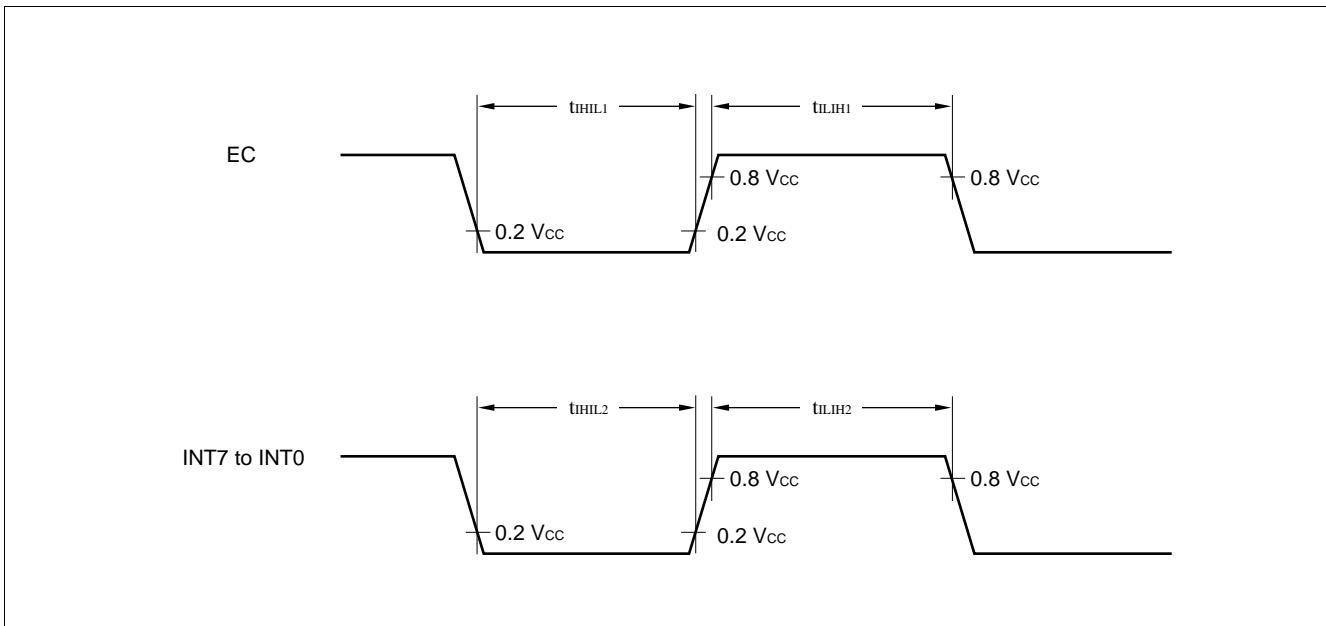


(6) Peripheral Input Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|------------------------------------|-----------|--------------|----------------|------|---------------|---------|
| | | | Min. | Max. | | |
| Peripheral input "H" pulse width 1 | t_{LH1} | EC | 1 t_{inst}^* | — | μs | |
| Peripheral input "L" pulse width 1 | t_{HL1} | | 1 t_{inst}^* | — | μs | |
| Peripheral input "H" pulse width 2 | t_{LH2} | INT7 to INT0 | 2 t_{inst}^* | — | μs | |
| Peripheral input "L" pulse width 2 | t_{HL2} | | 2 t_{inst}^* | — | μs | |

* : For information on t_{inst} , see "(4) Instruction Cycle."



MB89870 Series

5. A/D Converter Electrical Characteristics

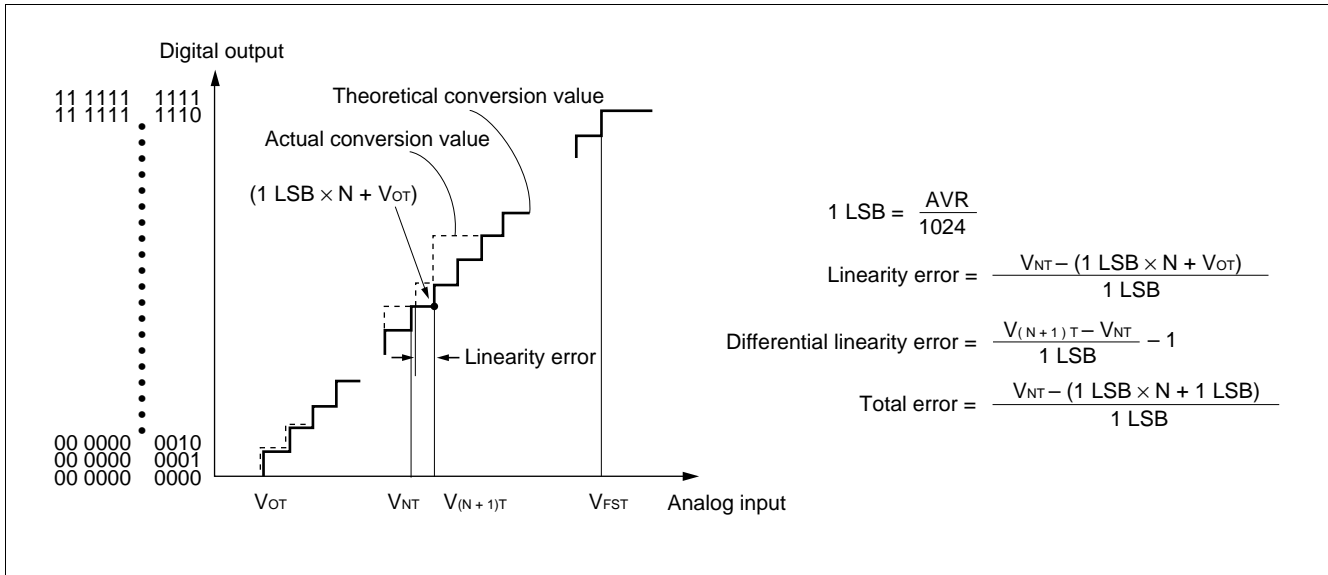
($AV_{CC} = V_{CC} = +3.5\text{ V to }+6.0\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|----------------------------------|-----------|------------|---|----------------------------|----------------------------|----------------------------|---------------|---------|
| | | | | Min. | Typ. | Max. | | |
| Resolution | — | — | — | — | — | 10 | bit | |
| Total error | | | — | — | ± 3.0 | LSB | | |
| Linearity error | | | — | — | ± 2.0 | LSB | | |
| Differential linearity error | | | — | — | ± 1.5 | LSB | | |
| Zero transition voltage | V_{OT} | — | $AVR = AV_{CC}$ | $AV_{SS} - 1.5\text{ LSB}$ | $AV_{SS} + 0.5\text{ LSB}$ | $AV_{SS} + 2.5\text{ LSB}$ | mV | |
| Full-scale transition voltage | V_{FST} | | | $AVR - 3.5\text{ LSB}$ | $AVR - 1.5\text{ LSB}$ | $AVR + 0.5\text{ LSB}$ | mV | |
| Interchannel disparity | — | | | — | — | 4.0 | LSB | |
| A/D mode conversion time | — | — | — | — | $33\ t_{inst}^*$ | — | μs | |
| Sense mode conversion time | — | | | — | $18\ t_{inst}^*$ | — | μs | |
| Analog port input current | I_{AIN} | AN0 to AN7 | — | — | — | 10 | μA | |
| Analog input voltage | — | — | — | 0.0 | — | AVR | V | |
| Reference voltage | — | — | — | 0.0 | — | AV_{CC} | V | |
| Reference voltage supply current | I_R | AVR | AVR = 5.0 V, when A/D conversion is activated | — | 200 | — | μA | |
| | I_{RH} | | AVR = 5.0 V, when A/D conversion is stopped | — | — | 1 | μA | |

* : For information on t_{inst} , see “(4) Instruction Cycle” in “4. AC Characteristics.”

6. A/D Converter Glossary

- Resolution
Analog changes that are identifiable with the A/D converter
When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit: LSB)
The deviation of the straight line connecting the zero transition point (“00 0000 0000” \leftrightarrow “00 0000 0001”) with the full-scale transition point (“11 1111 1111” \leftrightarrow “11 1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
The difference between theoretical and actual conversion values



7. Notes on Using A/D Converter

- **Input impedance of the analog input pins**

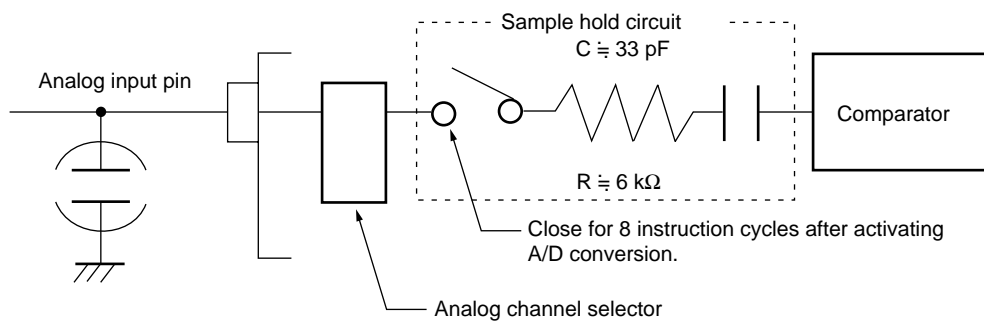
The A/D converter used for the MB89870 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.

- **Analog Input Equivalent Circuit**

If the analog input impedance is higher than 10 kΩ, it is recommended to connect an external capacitor of approx. 0.1 μF.



- **Error**

The smaller the $|AVR - AV_{SS}|$, the greater the error would become relatively.

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8. OP Amp Electrical Characteristics

(1) $AV_{CC} = 5.0\text{ V}$

($AV_{CC} = V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---------------------------|--------|--------------|-----------|---------------------|--------------|---------------------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| I/O voltage range | — | IN0± to IN3± | — | $0.5 V_{CC} - 1.25$ | $0.5 V_{CC}$ | $0.5 V_{CC} + 1.25$ | V | |
| Minimum load resistance | — | — | — | 100 | — | — | kΩ | |
| Maximum load resistance | — | — | — | — | — | 100 | pF | |
| Offset voltage | — | — | — | -10 | 0 | +10 | mV | |
| Gain-bandwidth production | — | — | — | — | 1.8 | — | MHz | |
| DC gain | — | — | — | — | 75 | — | dB | |
| Slew rate | — | — | — | — | 0.9 | — | V/μs | |

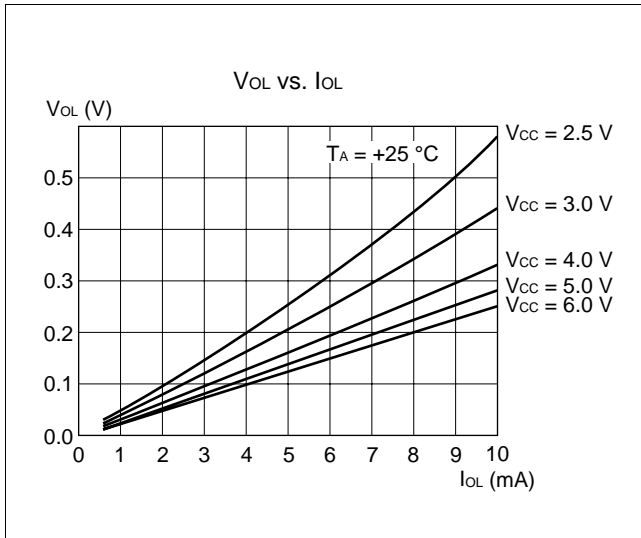
(2) $AV_{CC} = 3.0\text{ V}$

($AV_{CC} = V_{CC} = 2.7\text{ V to } 3.3\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

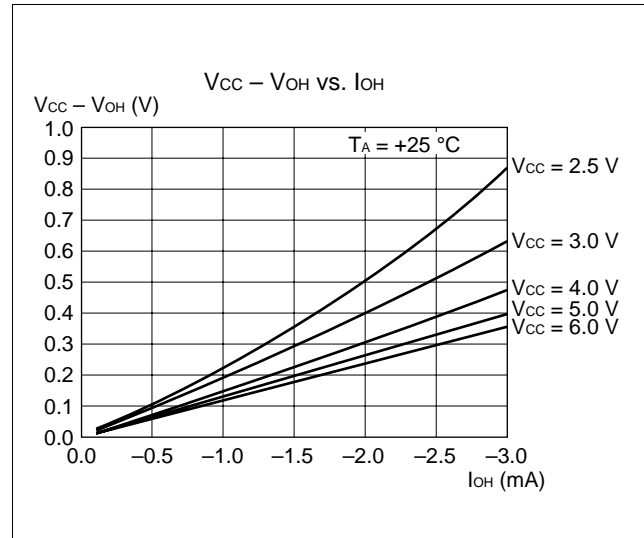
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---------------------------|--------|--------------|-----------|-------|---------------------|-----------------|------|---------|
| | | | | Min. | Typ. | Max. | | |
| I/O voltage range | — | IN0± to IN3± | — | 0.5 | $0.5 V_{CC} - 0.35$ | $V_{CC} - 1.20$ | V | |
| Minimum load resistance | — | — | — | 250 | — | — | kΩ | |
| Maximum load resistance | — | — | — | — | — | 100 | μA | |
| Offset voltage | — | — | — | -10 | 0 | +10 | mV | |
| Gain-bandwidth production | — | — | — | — | 0.5 | — | MHz | |
| DC gain | — | — | — | — | 75 | — | dB | |
| Slew rate | — | — | — | — | 0.1 | — | V/μs | |

EXAMPLE CHARACTERISTICS

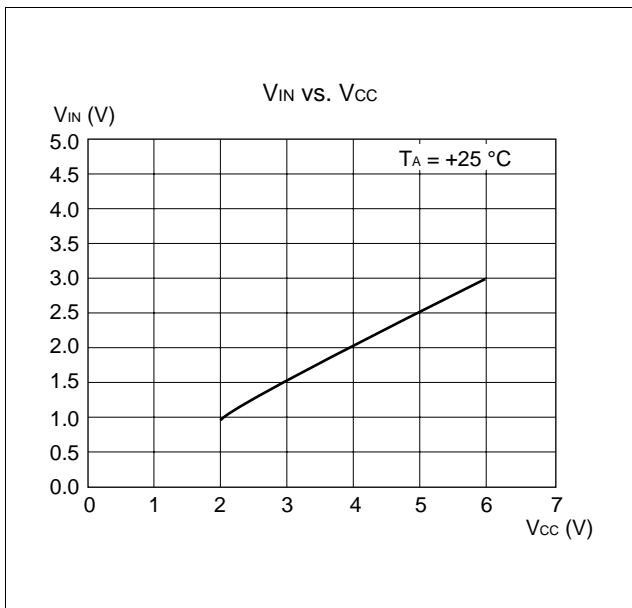
(1) "L" Level Output Voltage



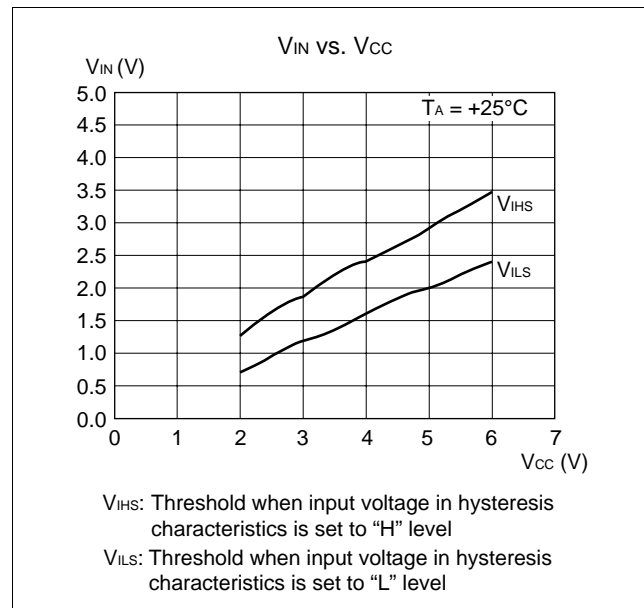
(2) "H" Level Output Voltage



(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)

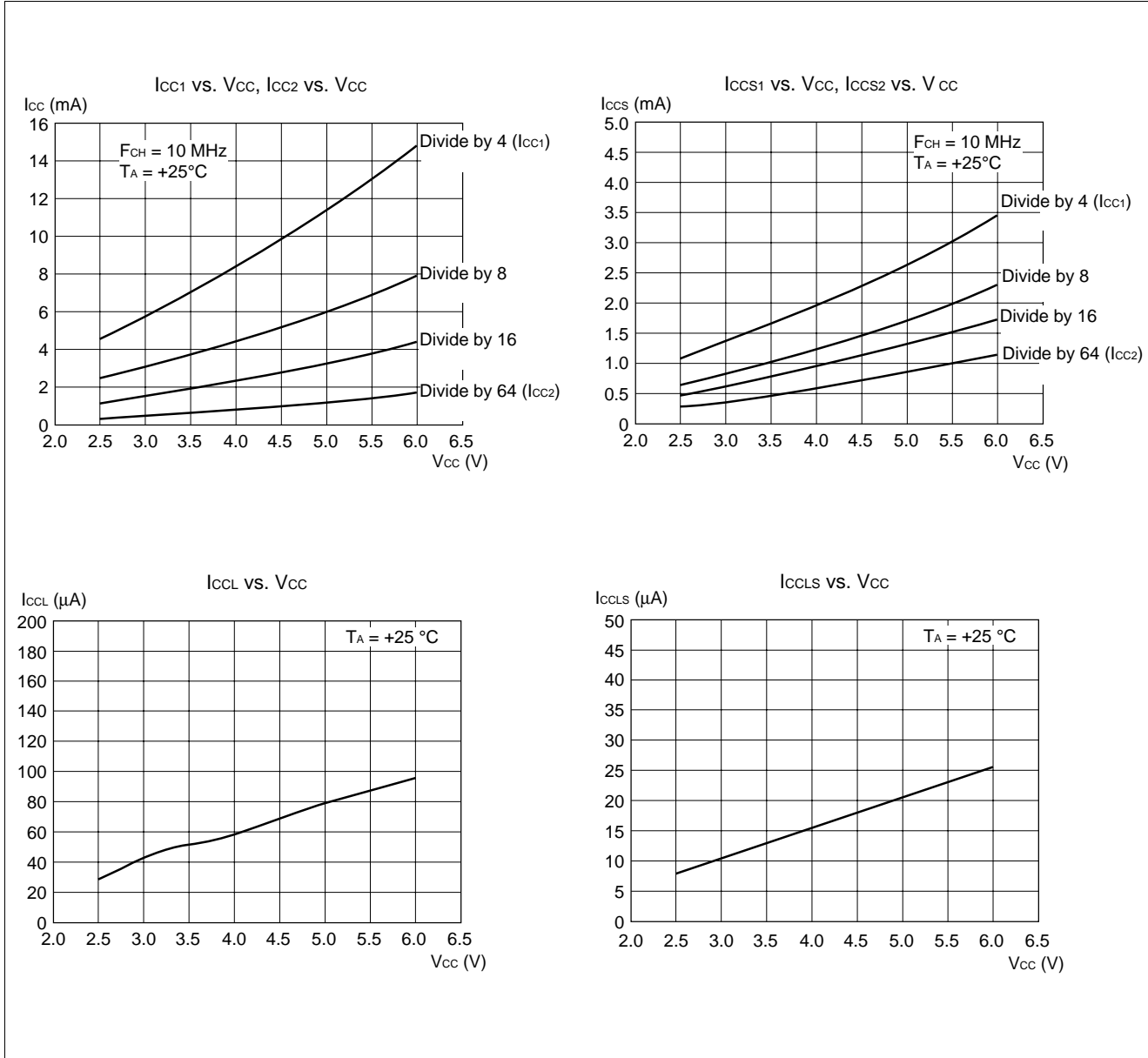


(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



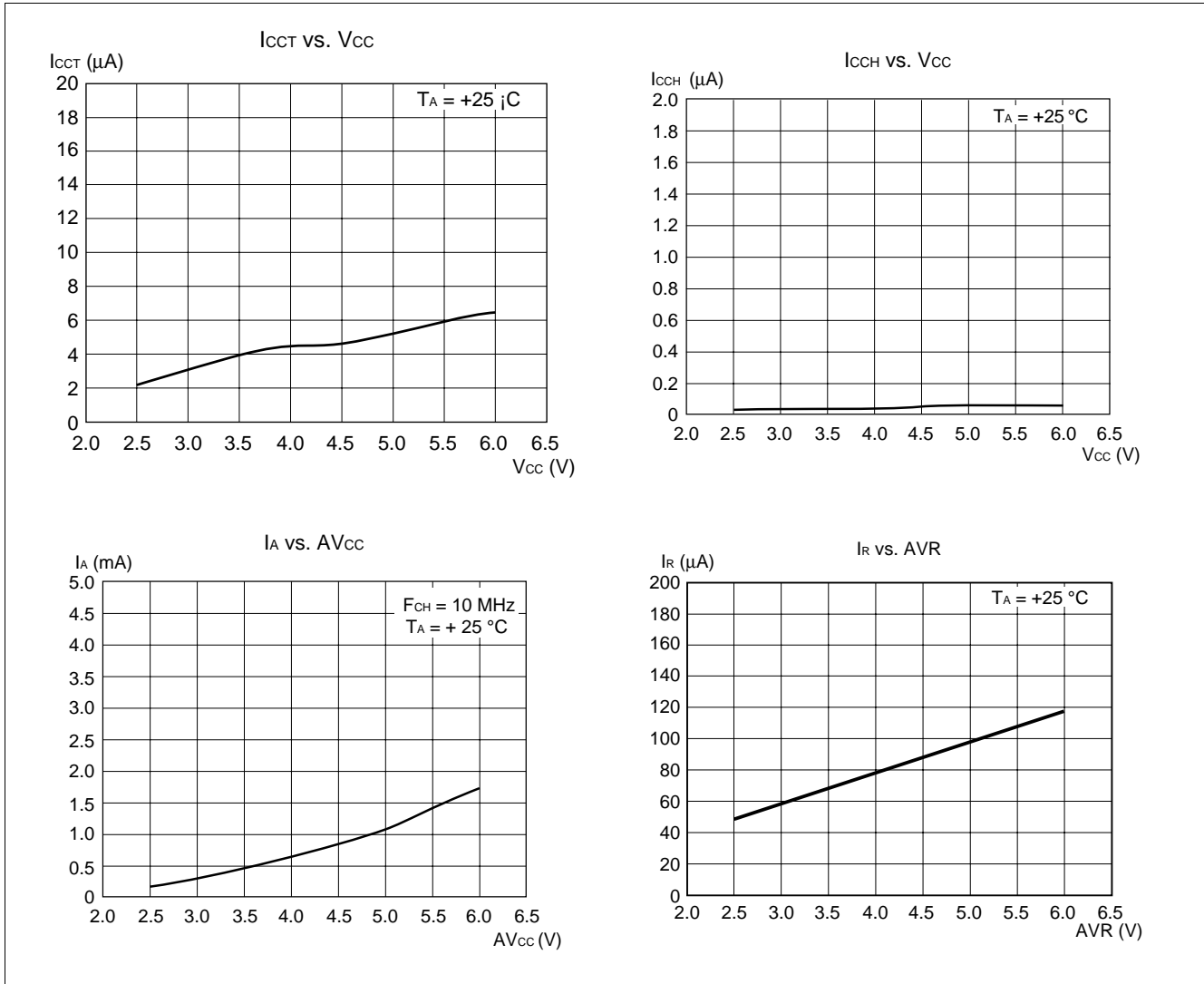
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(5) Power Supply Current (External Clock)

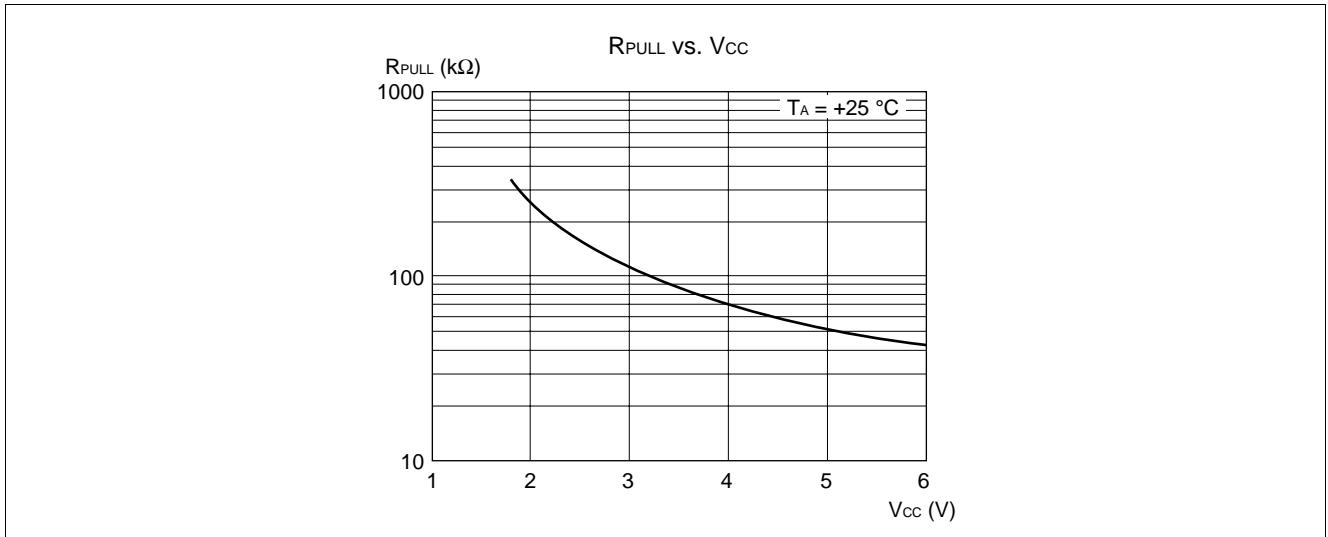


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(6) Pull-up Resistance



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■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

| Symbol | Meaning |
|--------|---|
| dir | Direct address (8 bits) |
| off | Offset (8 bits) |
| ext | Extended address (16 bits) |
| #vct | Vector table number (3 bits) |
| #d8 | Immediate data (8 bits) |
| #d16 | Immediate data (16 bits) |
| dir: b | Bit direct address (8:3 bits) |
| rel | Branch relative address (8 bits) |
| @ | Register indirect (Example: @A, @IX, @EP) |
| A | Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| AH | Upper 8 bits of accumulator A (8 bits) |
| AL | Lower 8 bits of accumulator A (8 bits) |
| T | Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| TH | Upper 8 bits of temporary accumulator T (8 bits) |
| TL | Lower 8 bits of temporary accumulator T (8 bits) |
| IX | Index register IX (16 bits) |
| EP | Extra pointer EP (16 bits) |
| PC | Program counter PC (16 bits) |
| SP | Stack pointer SP (16 bits) |
| PS | Program status PS (16 bits) |
| dr | Accumulator A or index register IX (16 bits) |
| CCR | Condition code register CCR (8 bits) |
| RP | Register bank pointer RP (5 bits) |
| Ri | General-purpose register Ri (8 bits, i = 0 to 7) |
| × | Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| (×) | Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.) |
| ((×)) | The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.) |

Columns indicate the following:

| | |
|-------------|---|
| Mnemonic: | Assembler notation of an instruction |
| ~: | The number of instructions |
| #: | The number of bytes |
| Operation: | Operation of an instruction |
| TL, TH, AH: | A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following: <ul style="list-style-type: none">• “-” indicates no change.• dH is the 8 upper bits of operation description data.• AL and AH must become the contents of AL and AH prior to the instruction executed.• 00 becomes 00. |
| N, Z, V, C: | An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag. |
| OP code: | Code of an instruction. If an instruction is more than one code, it is written according to the following rule: Example: 48 to 4F ← This indicates 48, 49, ... 4F. |

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Table 2 Transfer Instructions (48 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|------------------|---|---|---|----|----|----|------|----------|
| MOV dir,A | 3 | 2 | (dir) ← (A) | - | - | - | ---- | 45 |
| MOV @IX +off,A | 4 | 2 | ((IX) +off) ← (A) | - | - | - | ---- | 46 |
| MOV ext,A | 4 | 3 | (ext) ← (A) | - | - | - | ---- | 61 |
| MOV @EP,A | 3 | 1 | ((EP)) ← (A) | - | - | - | ---- | 47 |
| MOV Ri,A | 3 | 1 | (Ri) ← (A) | - | - | - | ---- | 48 to 4F |
| MOV A,#d8 | 2 | 2 | (A) ← d8 | AL | - | - | ++-- | 04 |
| MOV A,dir | 3 | 2 | (A) ← (dir) | AL | - | - | ++-- | 05 |
| MOV A,@IX +off | 4 | 2 | (A) ← ((IX) +off) | AL | - | - | ++-- | 06 |
| MOV A,ext | 4 | 3 | (A) ← (ext) | AL | - | - | ++-- | 60 |
| MOV A,@A | 3 | 1 | (A) ← ((A)) | AL | - | - | ++-- | 92 |
| MOV A,@EP | 3 | 1 | (A) ← ((EP)) | AL | - | - | ++-- | 07 |
| MOV A,Ri | 3 | 1 | (A) ← (Ri) | AL | - | - | ++-- | 08 to 0F |
| MOV dir,#d8 | 4 | 3 | (dir) ← d8 | - | - | - | ---- | 85 |
| MOV @IX +off,#d8 | 5 | 3 | ((IX) +off) ← d8 | - | - | - | ---- | 86 |
| MOV @EP,#d8 | 4 | 2 | ((EP)) ← d8 | - | - | - | ---- | 87 |
| MOV Ri,#d8 | 4 | 2 | (Ri) ← d8 | - | - | - | ---- | 88 to 8F |
| MOVW dir,A | 4 | 2 | (dir) ← (AH),(dir + 1) ← (AL) | - | - | - | ---- | D5 |
| MOVW @IX +off,A | 5 | 2 | ((IX) +off) ← (AH), ((IX) +off + 1) ← (AL) | - | - | - | ---- | D6 |
| MOVW ext,A | 5 | 3 | (ext) ← (AH), (ext + 1) ← (AL) | - | - | - | ---- | D4 |
| MOVW @EP,A | 4 | 1 | ((EP)) ← (AH),(EP + 1) ← (AL) | - | - | - | ---- | D7 |
| MOVW EP,A | 2 | 1 | (EP) ← (A) | - | - | - | ---- | E3 |
| MOVW A,#d16 | 3 | 3 | (A) ← d16 | AL | AH | dH | ++-- | E4 |
| MOVW A,dir | 4 | 2 | (AH) ← (dir), (AL) ← (dir + 1) | AL | AH | dH | ++-- | C5 |
| MOVW A,@IX +off | 5 | 2 | (AH) ← ((IX) +off), (AL) ← ((IX) +off + 1) | AL | AH | dH | ++-- | C6 |
| MOVW A,ext | 5 | 3 | (AH) ← (ext), (AL) ← (ext + 1) | AL | AH | dH | ++-- | C4 |
| MOVW A,@A | 4 | 1 | (AH) ← ((A)), (AL) ← ((A) + 1) | AL | AH | dH | ++-- | 93 |
| MOVW A,@EP | 4 | 1 | (AH) ← ((EP)), (AL) ← ((EP) + 1) | AL | AH | dH | ++-- | C7 |
| MOVW A,EP | 2 | 1 | (A) ← (EP) | - | - | dH | ---- | F3 |
| MOVW EP,#d16 | 3 | 3 | (EP) ← d16 | - | - | - | ---- | E7 |
| MOVW IX,A | 2 | 1 | (IX) ← (A) | - | - | - | ---- | E2 |
| MOVW A,IX | 2 | 1 | (A) ← (IX) | - | - | dH | ---- | F2 |
| MOVW SP,A | 2 | 1 | (SP) ← (A) | - | - | - | ---- | E1 |
| MOVW A,SP | 2 | 1 | (A) ← (SP) | - | - | dH | ---- | F1 |
| MOV @A,T | 3 | 1 | ((A)) ← (T) | - | - | - | ---- | 82 |
| MOVW @A,T | 4 | 1 | ((A)) ← (TH),(A + 1) ← (TL) | - | - | - | ---- | 83 |
| MOVW IX,#d16 | 3 | 3 | (IX) ← d16 | - | - | - | ---- | E6 |
| MOVW A,PS | 2 | 1 | (A) ← (PS) | - | - | dH | ---- | 70 |
| MOVW PS,A | 2 | 1 | (PS) ← (A) | - | - | - | ++++ | 71 |
| MOVW SP,#d16 | 3 | 3 | (SP) ← d16 | - | - | - | ---- | E5 |
| SWAP | 2 | 1 | (AH) ↔ (AL) | - | - | AL | ---- | 10 |
| SETB dir: b | 4 | 2 | (dir): b ← 1 | - | - | - | ---- | A8 to AF |
| CLRB dir: b | 4 | 2 | (dir): b ← 0 | - | - | - | ---- | A0 to A7 |
| XCH A,T | 2 | 1 | (AL) ↔ (TL) | AL | - | - | ---- | 42 |
| XCHW A,T | 3 | 1 | (A) ↔ (T) | AL | AH | dH | ---- | 43 |
| XCHW A,EP | 3 | 1 | (A) ↔ (EP) | - | - | dH | ---- | F7 |
| XCHW A,IX | 3 | 1 | (A) ↔ (IX) | - | - | dH | ---- | F6 |
| XCHW A,SP | 3 | 1 | (A) ↔ (SP) | - | - | dH | ---- | F5 |
| MOVW A,PC | 2 | 1 | (A) ← (PC) | - | - | dH | ---- | F0 |

- Notes:
- During byte transfer to A, T ← A is restricted to low bytes.
 - Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|-----------------|----|---|--|----|----|----|--------|----------|
| ADDC A,Ri | 3 | 1 | $(A) \leftarrow (A) + (Ri) + C$ | - | - | - | ++++ | 28 to 2F |
| ADDC A,#d8 | 2 | 2 | $(A) \leftarrow (A) + d8 + C$ | - | - | - | ++++ | 24 |
| ADDC A,dir | 3 | 2 | $(A) \leftarrow (A) + (dir) + C$ | - | - | - | ++++ | 25 |
| ADDC A,@IX +off | 4 | 2 | $(A) \leftarrow (A) + ((IX) + off) + C$ | - | - | - | ++++ | 26 |
| ADDC A,@EP | 3 | 1 | $(A) \leftarrow (A) + ((EP)) + C$ | - | - | - | ++++ | 27 |
| ADDCW A | 3 | 1 | $(A) \leftarrow (A) + (T) + C$ | - | - | dH | ++++ | 23 |
| ADDC A | 2 | 1 | $(AL) \leftarrow (AL) + (TL) + C$ | - | - | - | ++++ | 22 |
| SUBC A,Ri | 3 | 1 | $(A) \leftarrow (A) - (Ri) - C$ | - | - | - | ++++ | 38 to 3F |
| SUBC A,#d8 | 2 | 2 | $(A) \leftarrow (A) - d8 - C$ | - | - | - | ++++ | 34 |
| SUBC A,dir | 3 | 2 | $(A) \leftarrow (A) - (dir) - C$ | - | - | - | ++++ | 35 |
| SUBC A,@IX +off | 4 | 2 | $(A) \leftarrow (A) - ((IX) + off) - C$ | - | - | - | ++++ | 36 |
| SUBC A,@EP | 3 | 1 | $(A) \leftarrow (A) - ((EP)) - C$ | - | - | - | ++++ | 37 |
| SUBCW A | 3 | 1 | $(A) \leftarrow (T) - (A) - C$ | - | - | dH | ++++ | 33 |
| SUBC A | 2 | 1 | $(AL) \leftarrow (TL) - (AL) - C$ | - | - | - | ++++ | 32 |
| INC Ri | 4 | 1 | $(Ri) \leftarrow (Ri) + 1$ | - | - | - | +++- | C8 to CF |
| INCW EP | 3 | 1 | $(EP) \leftarrow (EP) + 1$ | - | - | - | ---- | C3 |
| INCW IX | 3 | 1 | $(IX) \leftarrow (IX) + 1$ | - | - | - | ---- | C2 |
| INCW A | 3 | 1 | $(A) \leftarrow (A) + 1$ | - | - | dH | +- - - | C0 |
| DEC Ri | 4 | 1 | $(Ri) \leftarrow (Ri) - 1$ | - | - | - | +++- | D8 to DF |
| DECW EP | 3 | 1 | $(EP) \leftarrow (EP) - 1$ | - | - | - | ---- | D3 |
| DECW IX | 3 | 1 | $(IX) \leftarrow (IX) - 1$ | - | - | - | ---- | D2 |
| DECW A | 3 | 1 | $(A) \leftarrow (A) - 1$ | - | - | dH | +- - - | D0 |
| MULU A | 19 | 1 | $(A) \leftarrow (AL) \times (TL)$ | - | - | dH | ---- | 01 |
| DIVU A | 21 | 1 | $(A) \leftarrow (T) / (AL), MOD \rightarrow (T)$ | dL | 00 | 00 | ---- | 11 |
| ANDW A | 3 | 1 | $(A) \leftarrow (A) \wedge (T)$ | - | - | dH | ++ R - | 63 |
| ORW A | 3 | 1 | $(A) \leftarrow (A) \vee (T)$ | - | - | dH | ++ R - | 73 |
| XORW A | 3 | 1 | $(A) \leftarrow (A) \nabla (T)$ | - | - | dH | ++ R - | 53 |
| CMP A | 2 | 1 | $(TL) - (AL)$ | - | - | - | ++++ | 12 |
| CMPW A | 3 | 1 | $(T) - (A)$ | - | - | - | ++++ | 13 |
| RORC A | 2 | 1 | $\rightarrow C \rightarrow A$ | - | - | - | ++ - + | 03 |
| ROLC A | 2 | 1 | $C \leftarrow A$ | - | - | - | ++ - + | 02 |
| CMP A,#d8 | 2 | 2 | $(A) - d8$ | - | - | - | ++++ | 14 |
| CMP A,dir | 3 | 2 | $(A) - (dir)$ | - | - | - | ++++ | 15 |
| CMP A,@EP | 3 | 1 | $(A) - ((EP))$ | - | - | - | ++++ | 17 |
| CMP A,@IX +off | 4 | 2 | $(A) - ((IX) + off)$ | - | - | - | ++++ | 16 |
| CMP A,Ri | 3 | 1 | $(A) - (Ri)$ | - | - | - | ++++ | 18 to 1F |
| DAA | 2 | 1 | Decimal adjust for addition | - | - | - | ++++ | 84 |
| DAS | 2 | 1 | Decimal adjust for subtraction | - | - | - | ++++ | 94 |
| XOR A | 2 | 1 | $(A) \leftarrow (AL) \nabla (TL)$ | - | - | - | ++ R - | 52 |
| XOR A,#d8 | 2 | 2 | $(A) \leftarrow (AL) \nabla d8$ | - | - | - | ++ R - | 54 |
| XOR A,dir | 3 | 2 | $(A) \leftarrow (AL) \nabla (dir)$ | - | - | - | ++ R - | 55 |
| XOR A,@EP | 3 | 1 | $(A) \leftarrow (AL) \nabla ((EP))$ | - | - | - | ++ R - | 57 |
| XOR A,@IX +off | 4 | 2 | $(A) \leftarrow (AL) \nabla ((IX) + off)$ | - | - | - | ++ R - | 56 |
| XOR A,Ri | 3 | 1 | $(A) \leftarrow (AL) \nabla (Ri)$ | - | - | - | ++ R - | 58 to 5F |
| AND A | 2 | 1 | $(A) \leftarrow (AL) \wedge (TL)$ | - | - | - | ++ R - | 62 |
| AND A,#d8 | 2 | 2 | $(A) \leftarrow (AL) \wedge d8$ | - | - | - | ++ R - | 64 |
| AND A,dir | 3 | 2 | $(A) \leftarrow (AL) \wedge (dir)$ | - | - | - | ++ R - | 65 |

(Continued)

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(Continued)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|------------------|---|---|--|----|----|----|------|----------|
| AND A,@EP | 3 | 1 | $(A) \leftarrow (AL) \wedge ((EP))$ | - | - | - | ++R- | 67 |
| AND A,@IX +off | 4 | 2 | $(A) \leftarrow (AL) \wedge ((IX) +off)$ | - | - | - | ++R- | 66 |
| AND A,Ri | 3 | 1 | $(A) \leftarrow (AL) \wedge (Ri)$ | - | - | - | ++R- | 68 to 6F |
| OR A | 2 | 1 | $(A) \leftarrow (AL) \vee (TL)$ | - | - | - | ++R- | 72 |
| OR A,#d8 | 2 | 2 | $(A) \leftarrow (AL) \vee d8$ | - | - | - | ++R- | 74 |
| OR A,dir | 3 | 2 | $(A) \leftarrow (AL) \vee (dir)$ | - | - | - | ++R- | 75 |
| OR A,@EP | 3 | 1 | $(A) \leftarrow (AL) \vee ((EP))$ | - | - | - | ++R- | 77 |
| OR A,@IX +off | 4 | 2 | $(A) \leftarrow (AL) \vee ((IX) +off)$ | - | - | - | ++R- | 76 |
| OR A,Ri | 3 | 1 | $(A) \leftarrow (AL) \vee (Ri)$ | - | - | - | ++R- | 78 to 7F |
| CMP dir,#d8 | 5 | 3 | $(dir) - d8$ | - | - | - | ++++ | 95 |
| CMP @EP,#d8 | 4 | 2 | $((EP)) - d8$ | - | - | - | ++++ | 97 |
| CMP @IX +off,#d8 | 5 | 3 | $((IX) +off) - d8$ | - | - | - | ++++ | 96 |
| CMP Ri,#d8 | 4 | 2 | $(Ri) - d8$ | - | - | - | ++++ | 98 to 9F |
| INCW SP | 3 | 1 | $(SP) \leftarrow (SP) + 1$ | - | - | - | ---- | C1 |
| DECW SP | 3 | 1 | $(SP) \leftarrow (SP) - 1$ | - | - | - | ---- | D1 |

Table 4 Branch Instructions (17 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|----------------|---|---|---|----|----|----|---------|----------|
| BZ/BEQ rel | 3 | 2 | If $Z = 1$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | FD |
| BNZ/BNE rel | 3 | 2 | If $Z = 0$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | FC |
| BC/BLO rel | 3 | 2 | If $C = 1$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | F9 |
| BNC/BHS rel | 3 | 2 | If $C = 0$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | F8 |
| BN rel | 3 | 2 | If $N = 1$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | FB |
| BP rel | 3 | 2 | If $N = 0$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | FA |
| BLT rel | 3 | 2 | If $V \vee N = 1$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | FF |
| BGE rel | 3 | 2 | If $V \vee N = 0$ then $PC \leftarrow PC + rel$ | - | - | - | ---- | FE |
| BBC dir: b,rel | 5 | 3 | If $(dir: b) = 0$ then $PC \leftarrow PC + rel$ | - | - | - | --+-- | B0 to B7 |
| BBS dir: b,rel | 5 | 3 | If $(dir: b) = 1$ then $PC \leftarrow PC + rel$ | - | - | - | --+-- | B8 to BF |
| JMP @A | 2 | 1 | $(PC) \leftarrow (A)$ | - | - | - | ---- | E0 |
| JMP ext | 3 | 3 | $(PC) \leftarrow ext$ | - | - | - | ---- | 21 |
| CALLV #vct | 6 | 1 | Vector call | - | - | - | ---- | E8 to EF |
| CALL ext | 6 | 3 | Subroutine call | - | - | - | ---- | 31 |
| XCHW A,PC | 3 | 1 | $(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$ | - | - | dH | ---- | F4 |
| RET | 4 | 1 | Return from subroutine | - | - | - | ---- | 20 |
| RETI | 6 | 1 | Return form interrupt | - | - | - | Restore | 30 |

Table 5 Other Instructions (9 instructions)

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC | OP code |
|----------|---|---|-----------|----|----|----|-------|---------|
| PUSHW A | 4 | 1 | | - | - | - | ---- | 40 |
| POPW A | 4 | 1 | | - | - | dH | ---- | 50 |
| PUSHW IX | 4 | 1 | | - | - | - | ---- | 41 |
| POPW IX | 4 | 1 | | - | - | - | ---- | 51 |
| NOP | 1 | 1 | | - | - | - | ---- | 00 |
| CLRC | 1 | 1 | | - | - | - | ----R | 81 |
| SETC | 1 | 1 | | - | - | - | ----S | 91 |
| CLRI | 1 | 1 | | - | - | - | ---- | 80 |
| SETI | 1 | 1 | | - | - | - | ---- | 90 |

INSTRUCTION MAP

| L | H | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|--------------|--------------|---------------|---------------|--------------|--------------|--------------|--------------|-------------|----------------|----------------|-------------|----------------|---------------|---------------|--------------|-----------|
| 0 | NOP | SWAP A | RET | RETI | PUSHW A | PUSHW A | POPW A | MOV A,ext | MOVW A,PS | CLRI | SETI | CLRB dir: 0 | BBC dir: 0,rel | INCW A | DECW A | JMP @A | MOVW A,PC |
| 1 | MULU A | DIVU A | JMP addr16 | CALL addr16 | PUSHW IX | PUSHW IX | POPW PS,A | MOV ext,A | MOVW PS,A | CLRC | SETC | CLRB dir: 1 | BBC dir: 1,rel | INCW SP | DECW SP | MOVW SP,A | MOVW A,SP |
| 2 | ROLC A | CMP A | ADDC A | SUBC A | XCH A,T | XCH A,T | XOR A | AND A | OR A | MOV @A,T | MOV A,@A | CLRB dir: 2 | BBC dir: 2,rel | INCW IX | DECW IX | MOVW IX,A | MOVW A,IX |
| 3 | RORC A | CMPW A | ADDCW A | SUBCW A | XCHW A,T | XCHW A,T | XORW A | ANDW A | ORW A | MOVW @A,T | MOVW A,@A | CLRB dir: 3 | BBC dir: 3,rel | INCW EP | DECW EP | MOVW EP,A | MOVW A,EP |
| 4 | MOV A,#d8 | CMP A,#d8 | ADDC A,#d8 | SUBC A,#d8 | XOR A,#d8 | XOR A,#d8 | XOR A,#d8 | AND A,#d8 | OR A,#d8 | DAA | DAS | CLRB dir: 4 | BBC dir: 4,rel | MOVW A,ext | MOVW ext,A | MOVW A,#d16 | XCHW A,PC |
| 5 | MOV A,dir | CMP A,dir | ADDC A,dir | SUBC A,dir | XOR A,dir | MOV dir,A | XOR A,dir | AND A,dir | OR A,dir | MOV dir,#d8 | CMP dir,#d8 | CLRB dir: 5 | BBC dir: 5,rel | MOVW A,dir | MOVW dir,A | MOVW SP,#d16 | XCHW A,SP |
| 6 | MOV A,@IX +d | CMP A,@IX +d | ADDC A,@IX +d | SUBC A,@IX +d | XOR A,@IX +d | MOV @IX +d,A | XOR A,@IX +d | AND A,@IX +d | OR A,@IX +d | MOV @IX +d,#d8 | CMP @IX +d,#d8 | CLRB dir: 6 | BBC dir: 6,rel | MOVW A,@IX +d | MOVW @IX +d,A | MOVW IX,#d16 | XCHW A,IX |
| 7 | MOV A,@EP | CMP A,@EP | ADDC A,@EP | SUBC A,@EP | XOR A,@EP | MOV @EP,A | XOR A,@EP | AND A,@EP | OR A,@EP | MOV @EP,#d8 | CMP @EP,#d8 | CLRB dir: 7 | BBC dir: 7,rel | MOVW A,@EP | MOVW @EP,A | MOVW EP,#d16 | XCHW A,EP |
| 8 | MOV A,R0 | CMP A,R0 | ADDC A,R0 | SUBC A,R0 | MOV R0,A | MOV R0,A | XOR A,R0 | AND A,R0 | OR A,R0 | MOV R0,#d8 | CMP R0,#d8 | SETB dir: 0 | BBS dir: 0,rel | INC R0 | DEC R0 | CALLV #0 | BNC rel |
| 9 | MOV A,R1 | CMP A,R1 | ADDC A,R1 | SUBC A,R1 | MOV R1,A | MOV R1,A | XOR A,R1 | AND A,R1 | OR A,R1 | MOV R1,#d8 | CMP R1,#d8 | SETB dir: 1 | BBS dir: 1,rel | INC R1 | DEC R1 | CALLV #1 | BC rel |
| A | MOV A,R2 | CMP A,R2 | ADDC A,R2 | SUBC A,R2 | MOV R2,A | MOV R2,A | XOR A,R2 | AND A,R2 | OR A,R2 | MOV R2,#d8 | CMP R2,#d8 | SETB dir: 2 | BBS dir: 2,rel | INC R2 | DEC R2 | CALLV #2 | BP rel |
| B | MOV A,R3 | CMP A,R3 | ADDC A,R3 | SUBC A,R3 | MOV R3,A | MOV R3,A | XOR A,R3 | AND A,R3 | OR A,R3 | MOV R3,#d8 | CMP R3,#d8 | SETB dir: 3 | BBS dir: 3,rel | INC R3 | DEC R3 | CALLV #3 | BN rel |
| C | MOV A,R4 | CMP A,R4 | ADDC A,R4 | SUBC A,R4 | MOV R4,A | MOV R4,A | XOR A,R4 | AND A,R4 | OR A,R4 | MOV R4,#d8 | CMP R4,#d8 | SETB dir: 4 | BBS dir: 4,rel | INC R4 | DEC R4 | CALLV #4 | BNZ rel |
| D | MOV A,R5 | CMP A,R5 | ADDC A,R5 | SUBC A,R5 | MOV R5,A | MOV R5,A | XOR A,R5 | AND A,R5 | OR A,R5 | MOV R5,#d8 | CMP R5,#d8 | SETB dir: 5 | BBS dir: 5,rel | INC R5 | DEC R5 | CALLV #5 | BZ rel |
| E | MOV A,R6 | CMP A,R6 | ADDC A,R6 | SUBC A,R6 | MOV R6,A | MOV R6,A | XOR A,R6 | AND A,R6 | OR A,R6 | MOV R6,#d8 | CMP R6,#d8 | SETB dir: 6 | BBS dir: 6,rel | INC R6 | DEC R6 | CALLV #6 | BGE rel |
| F | MOV A,R7 | CMP A,R7 | ADDC A,R7 | SUBC A,R7 | MOV R7,A | MOV R7,A | XOR A,R7 | AND A,R7 | OR A,R7 | MOV R7,#d8 | CMP R7,#d8 | SETB dir: 7 | BBS dir: 7,rel | INC R7 | DEC R7 | CALLV #7 | BLT rel |

MB89870 Series

■ MASK OPTIONS

| No. | Part number | MB89875 | MB89P875 | MB89PV870 |
|-----|--|--|--|--|
| | Specifying procedure | Specify when ordering masking | Set with EPROM programmer | Setting not possible |
| 1 | Pull-up resistors P00 to P07, P10 to P17, P20 to P24, P30 to P37, P40 to P47, P50 to P57 | Specify by pin (in 2-pin unit for P10 to P17, and in 4-pin unit for P40 to P47) | Specify by pin (in 2-pin unit for P10 to P17, and in 4-pin unit for P40 to P47) | Fixed to without pull-up resistor |
| 2 | Power-on reset selection With power-on reset Without power-on reset | Selectable | Selectable | Fixed to with power-on reset |
| 3 | Selection of the oscillation stabilization time initial value $2^{18}/F_{CH}$ (Approx. 26.2 ms) $2^{17}/F_{CH}$ (Approx. 13.1 ms) $2^{13}/F_{CH}$ (Approx. 0.8 ms) $2^4/F_{CH}$ (Approx. 0 ms) | Selectable | Selectable | Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms) |
| 4 | Selection either single- or dual-clock system Single clock Dual Clock | Selectable | Selectable | Fixed to dual-clock system |
| 5 | Reset pin output With reset output Without reset output | Selectable | Selectable | Fixed to with reset output |

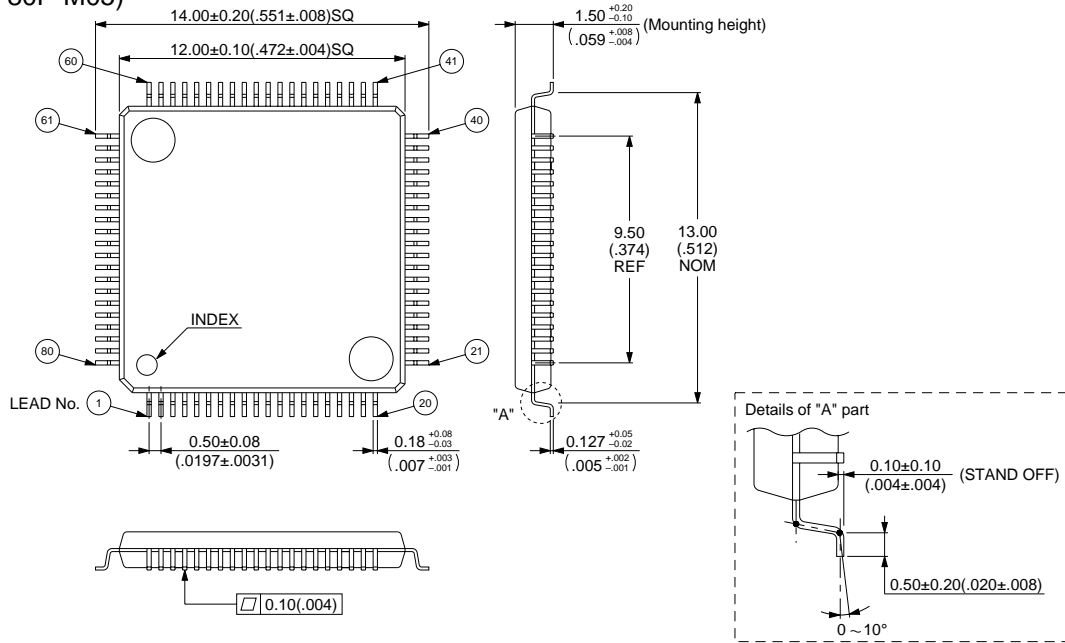
- Notes:
- Reset is input asynchronized with the internal clock whether with or without power-on reset.
 - P30 to P37 should be set to without pull-up resistor when an A/D converter is used.
 - P10 to P17, P34 to P37 should be set to without pull-up resistor when an OP amp is used.
 - P40 to P47 and P23 and P24 should be set to without pull-up resistor when an LCD controller/driver is used.

■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---------------------------|--------------------------------------|---------|
| MB89875PFV MB89P875PFV | 80-pin Plastic LQFP (FPT-80P-M05) | |
| MB89875PF MB89P875PF | 80-pin Plastic QFP (FPT-80P-M06) | |
| MB89PV870CF | 80-pin Ceramic MQFP (MQP-80C-P01) | |

PACKAGE DIMENSIONS

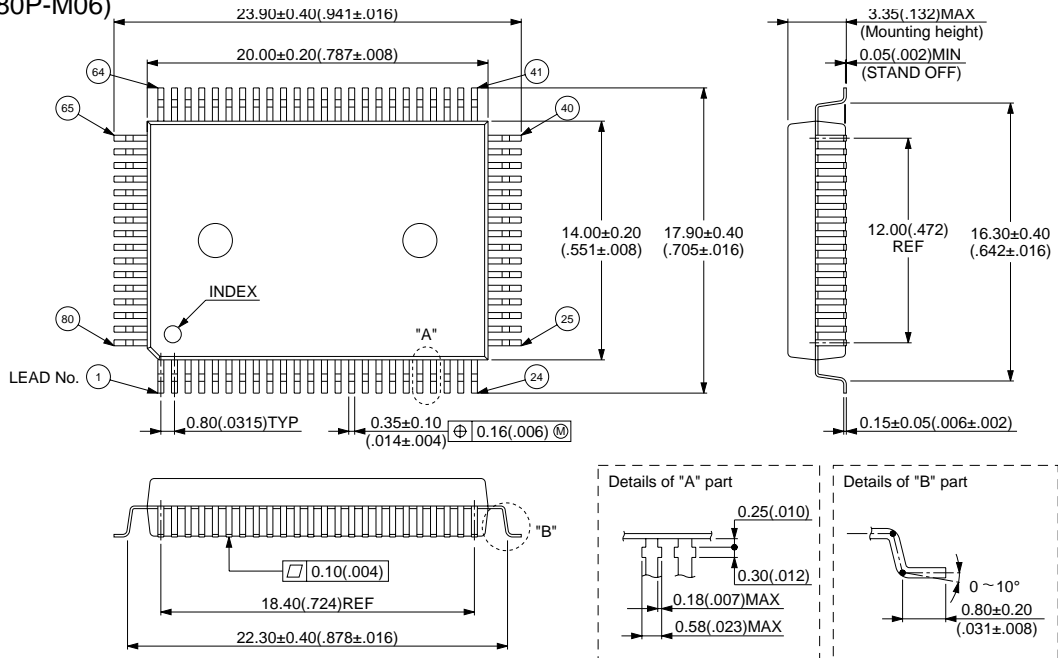
80-pin Plastic LQFP (FPT-80P-M05)



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Dimensions in mm (inches)

80-pin Plastic QFP (FPT-80P-M06)

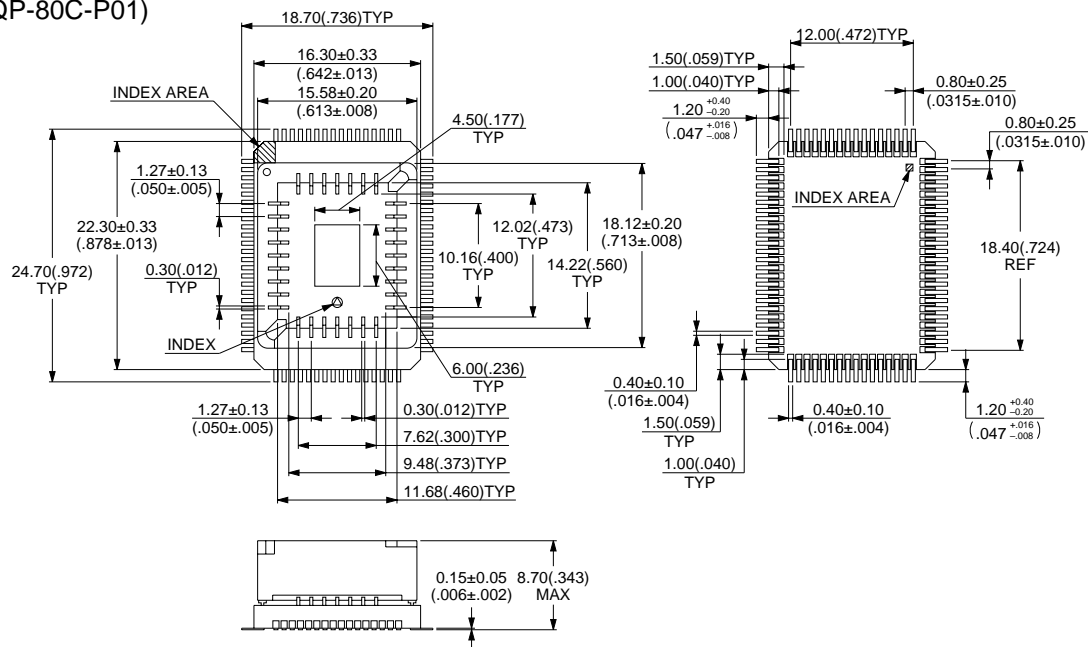


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Dimensions in mm (inches)

MB89870 Series

80-pin Ceramic MQFP
(MQP-80C-P01)



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Dimensions in mm (inches)

FUJITSU LIMITED

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