5-CH High-Efficiency PMIC

Features

- Wide 3.5V to 18V Operating Input Range
- High Efficient DC/DC Converter: 92~96%
- Low Power Consumption (Sleep Mode) < 10μA
- Built-in Power On Reset
- Built-in soft start
- Over Voltage Lock Out (OVLO)
- Under Voltage Lock Out (UVLO)
- Over current protection (OCP)
- Short circuit protection (SCP)
- Over thermal protection (OTP)
- Available in in QFN28-4×4 Package
- -40°C to +85°C Temperature Range
- Buck DC/DC Converter (3-CH)
  BUCK1-BUCK2: Input 3.5V~18.0V, output 0.6V ~ VIN adjustable, load current up to 2A
  BUCK3: Input 2.5V~5.5V, output 0.6V~ VIN adjustable, load current up to 2A
- High PSRR LDO (2-CH)
  LDO1: Output 0.6V~5.0V fixed, load current up to 500mA
  LDO2: Output 0.6V~5.0V adjustable, load current up to 500mA
- Power On Reset (1-CH)
- Support reset function

Applications

- Mobile Internet Devices
- Tablet Personal Computer (Pad)
- Personal Navigation Devices
- Entertaining and Education Machine
- Portable Media Player (PMP)
- Digital Photo Frame

General Description

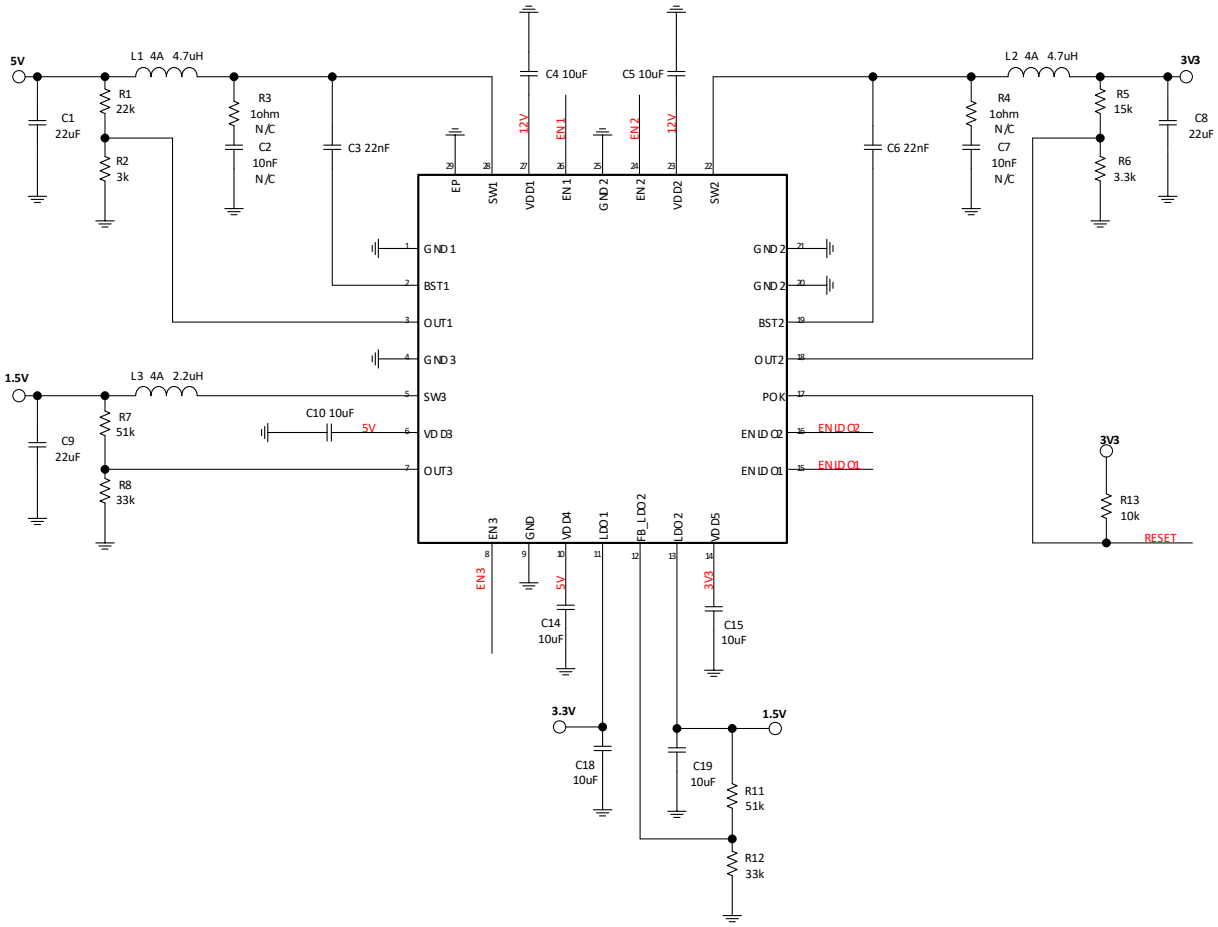
RY1505 is a highly integrated power management IC (PMIC) designed to minimize power consumption in consumer and multimedia applications. It provides a complete system power management solution, the RY1505 integrates 3-ch synchronous buck converter, 2-ch LDO,1-ch power on reset. The converters are optimized for high efficiency (greater than 92%) and feature integrated low impedance FETs. The RY1505 is available in a 28 pins QFN 4×4 package.

Product Options

Block	Input voltage	Output voltage	Capability
BUCK1/BUCK2	3.5~18.0V	Adjustable	Up to 2A
BUCK3	2.5~5.5V	Adjustable	Up to 2A
LDO1	2.5V~5.5V	Fixed (Customized)	Up to 0.5A
LDO2	2.5V~5.5V	Adjustable	Up to 0.5A
Power On Reset	3.3V		50mS delay

5-CH High-Efficiency PMIC

Typical Application Circuit



Basic Application Circuit

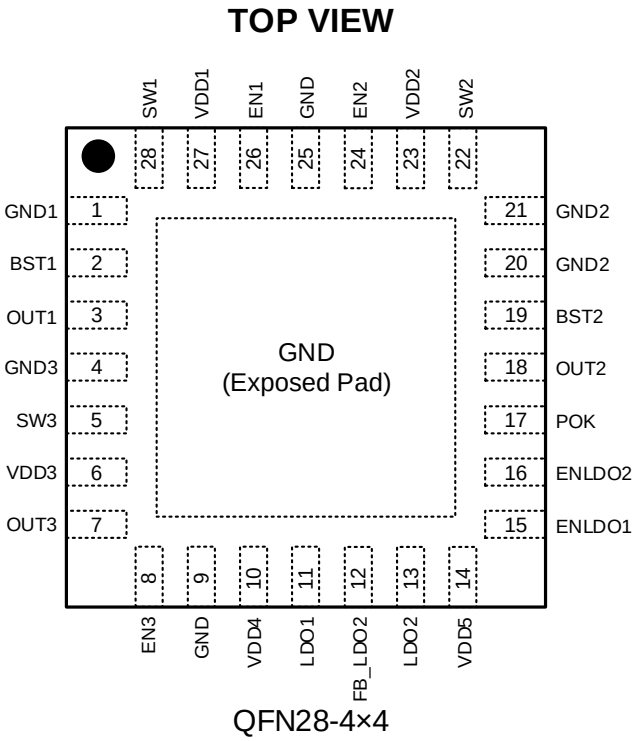
Order Information

Marking	Part No.	Model	Description	Package	Shipment
RY1505 YYLL	70305001	RY1505	RY1505 5-CH PMU, 2×Buck: V_{IN} 3.5-18V, 2A, 600KHz, V_{FB} 0.6V; 1×Buck: V_{IN} 2.5-5.5V, 2A, 1.2MHz, V_{FB} 0.6V; 1×ADJ LDO: V_{IN} 2.5-5.5V, 500mA, V_{FB} 0.6V; 1×Fixed LDO: V_{IN} 2.5-5.5V, 500mA; Power On Reset, QFN28-4×4	QFN28-4×4	T/R 5000

5-CH High-Efficiency PMIC

Pin Description

Pin Configuration



QFN28-4×4

Top Marking: RY1505YYLL (device code: 1505, Y=year code, LL= lot number code)

Pin Description

Pin	Name	Function
1	GND1	Ground
2	BST1	Bootstrap. A capacitor connected between SW1 and BST1 pins is required to form a floating supply across the high-side switch driver. Use a 22nF capacitor.
3	OUT1	BUCK1 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
4	GND3	Ground
5	SW3	BUCK3 Switching Pin, Connect this Pin to inductor, Minimize the track area to reduce EMI.
6	VDD3	BUCK3 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
7	OUT3	BUCK3 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
8	EN3	BUCK3 Enable (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
9	GND	Ground
10	VDD4	LDO1 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.

11	LDO1	LDO1 Output pin, Bypass 10μF capacitor to GND.
12	FB_LDO2	LDO2 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
13	LDO2	LDO2 Output pin, Bypass 10μF capacitor to GND
14	VDD5	LDO2 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
15	ENLDO1	LDO1 Enable (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
16	ENLDO2	LDO2 Enable (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
17	POK	Power On Reset
18	OUT2	BUCK2 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
19	BST2	Bootstrap. A capacitor connected between SW2 and BST2 pins is required to form a floating supply across the high-side switch driver. Use a 22nF capacitor.
20	GND2	Ground
21	GND2	Ground
22	SW2	BUCK2 Switching Pin, Connect this Pin to inductor, Minimize the track area to reduce EMI.
23	VDD2	BUCK2 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
24	EN2	BUCK2 Enable (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
25	GND	Ground
26	EN1	BUCK1 Enable (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
27	VDD1	BUCK1 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
28	SW1	BUCK1 Switching Pin, Connect this Pin to inductor, Minimize the track area to reduce EMI.
29	EP	Thermal PAD, connect to Ground.

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
VDD1, SW1, BST1	-0.3	28	V
VDD2, SW2, BST2	-0.3	28	V
Other pin Voltage	-0.3	6.0	V
Pink Current limit		3	A
Junction Temperature		125	°C
Operating Temperature	-40	125	°C
Storage Temperature Range	-55	150	°C
Lead Temperature		300	°C
Junction to Ambient Temperature		21	°C /W

Note1: Exceeding these ratings may damage the device.

Note2: The device is not guaranteed to function outside of its operating conditions.

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Electrical Characteristics

BUCK1 & BUCK2 Electrical Characteristics

(V_{IN} = 12V, T_A= 25°C unless otherwise specified)

Parameter	Symbol	Test conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}		3.5		18	V
Input UVLO Threshold		Input Voltage Rising			3	V
Standby Supply Current		V_{FB} = 103%, I_{OUT} = 0		400	600	μA
Shutdown Supply Current		EN1/EN2 = 0, V_{IN} = 12V		3		μA
Feedback Voltage	V_{FB}		0.588	0.6	0.612	V
Output Voltage Line Regulation				0.04	0.4	%/V
Output Voltage Load Regulation				0.5		%
Current Limit	I_{LIM}	Duty = 30%		3		A
Oscillator Frequency	F_{SW}			0.6		MHz
NMOS On Resistance	R_{ONN}	I_{SW}=100mA		0.07		Ω

BUCK3 Electrical Characteristics

(V_{IN} = 3.6V, T_A= 25°C unless otherwise specified)

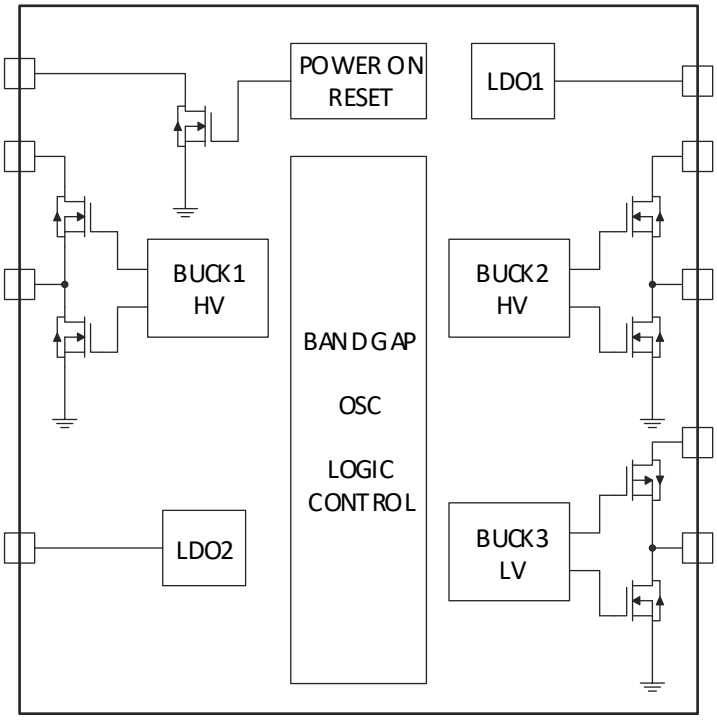
Parameter	Symbol	Test conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold		Input Voltage Rising		2.4		V
Operating Supply Current		V_{FB} = 60%, I_{OUT} = 0		150	200	μA
Standby Supply Current		V_{FB} = 103%, I_{OUT} = 0		40	80	μA
Shutdown Supply Current		EN3 = 0, V_{IN} = 4.2V		0.1	1	μA
Output Voltage Regulation Accuracy	V_{FB}		-1.5	1	1.5	%
Feedback Voltage			0.588	0.6	0.612	V
Output Voltage Line Regulation				0.04	0.4	%/V
Output Voltage Load Regulation				0.5		%
Current Limit	I_{LIM}	Duty = 30%		3		A
Oscillator Frequency	F_{SW}			1.2		MHz
PMOS On Resistance	R_{ONP}	I_{SW}=100mA		0.1		Ω
NMOS On Resistance	R_{ONN}	I_{SW}=100mA		0.07		Ω

LDO1 & LDO2 Electrical Characteristics

(V_{IN} = 3.6V, T_A= 25°C unless otherwise specified)

Parameter	Symbol	Test conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold		Input Voltage Rising		2.4	3	V
Output Voltage Accuracy			-3	1.5	3	%
Output Voltage (LDO1)				Fixed		V
Feedback Voltage (LDO2)	V_{FB}		0.588	0.6	0.612	V

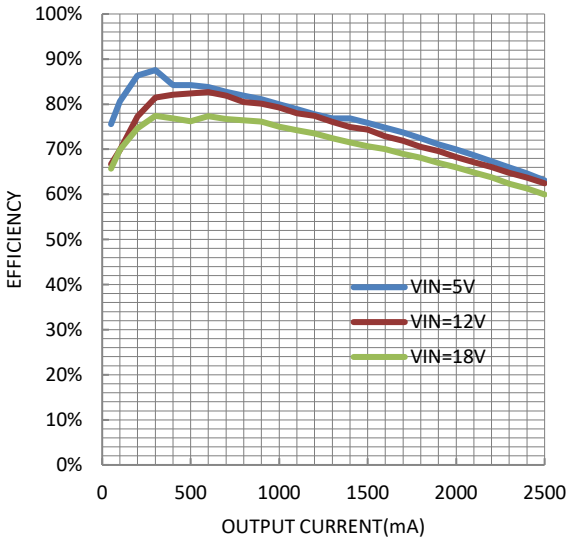
Functional Block Diagram



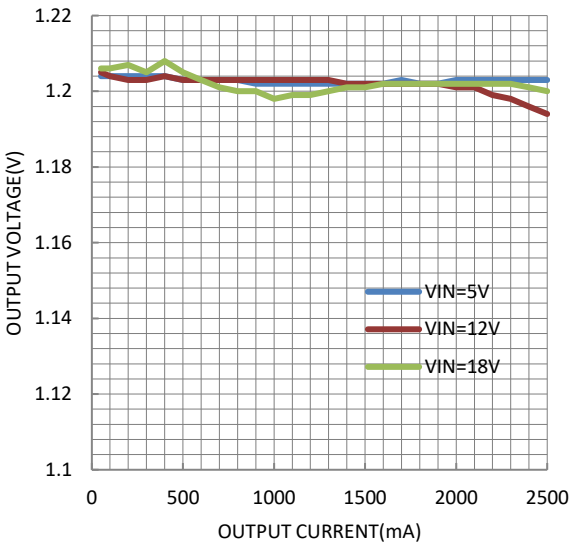
RY1505 Block Diagram

Typical Performance Characteristics

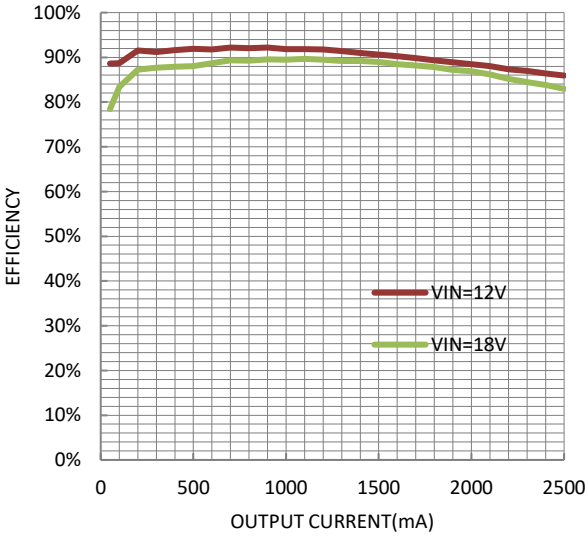
HV BUCK1:EFFICIENCY VS OUTPUT CURRENT
(VOUT=1.2V)



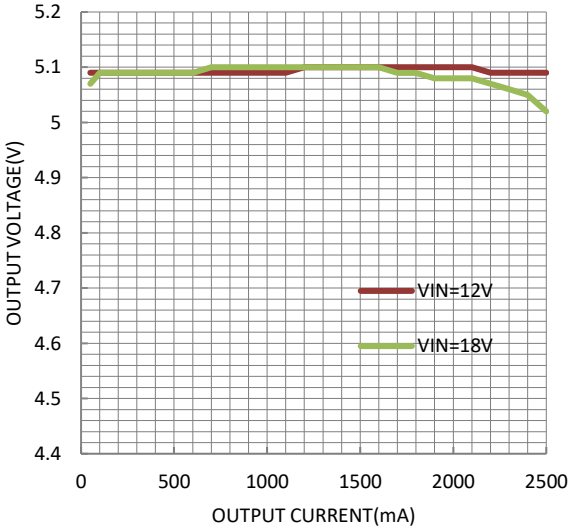
HV BUCK1:OUTPUT VOLTAGE VS OUTPUT CURRENT
(VOUT=1.2V)



HV BUCK1:EFFICIENCY VS OUTPUT CURRENT
(VOUT=5V)



HV BUCK1:OUTPUT VOLTAGE VS OUTPUT CURRENT
(VOUT=5V)



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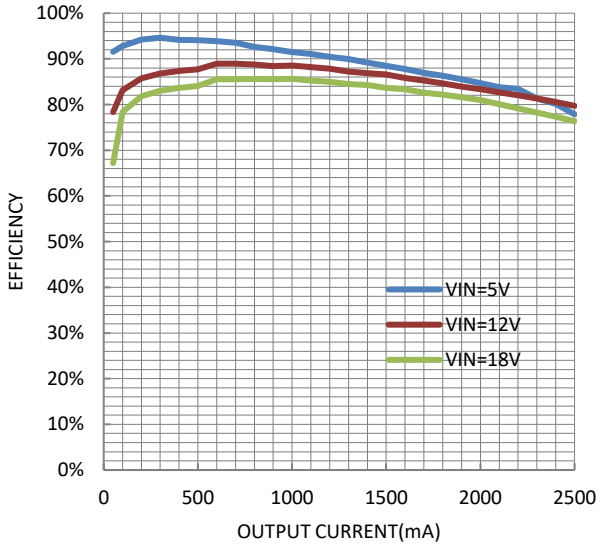
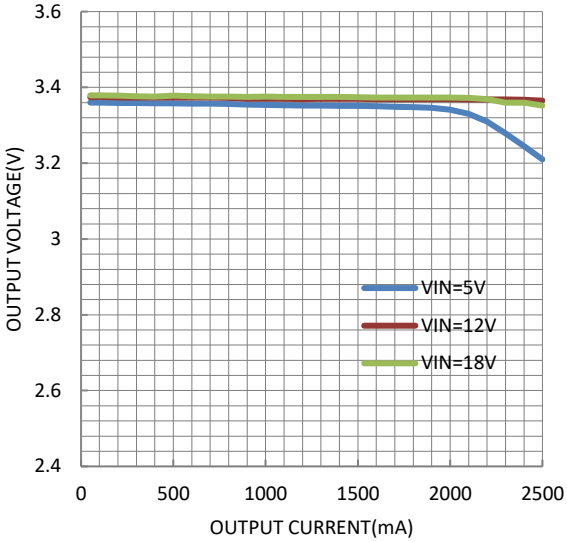
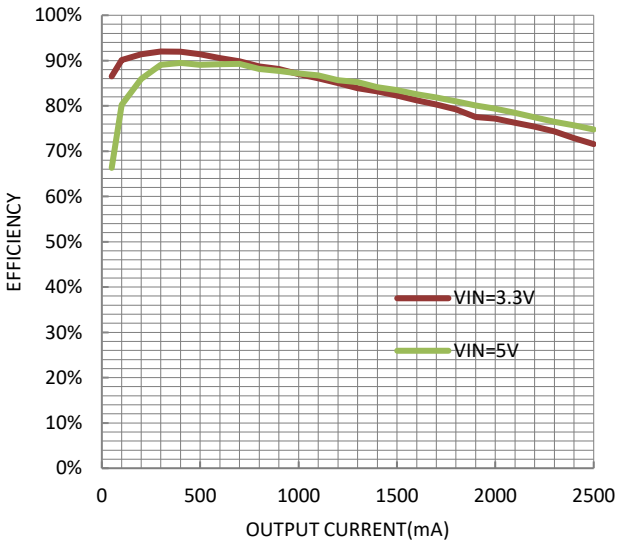
HV BUCK2:EFFICIENCY VS OUTPUT CURRENT
(VOUT=3.3V)



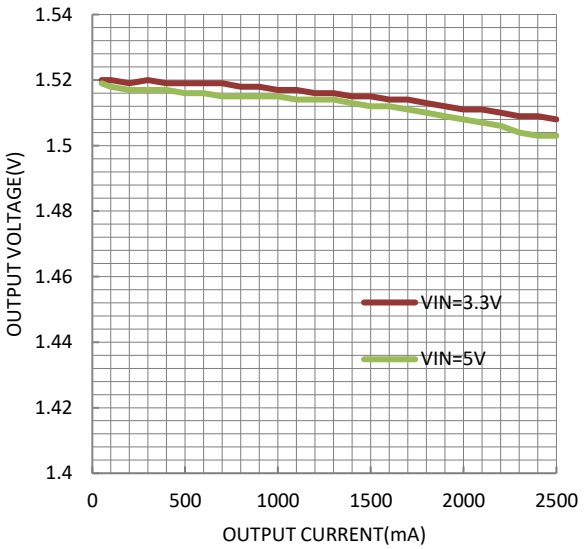
HV BUCK2:OUTPUT VOLTAGE VS OUTPUT CURRENT
(VOUT=3.3V)



LV BUCK1:EFFICIENCY VS OUTPUT CURRENT
(VOUT=1.5V)

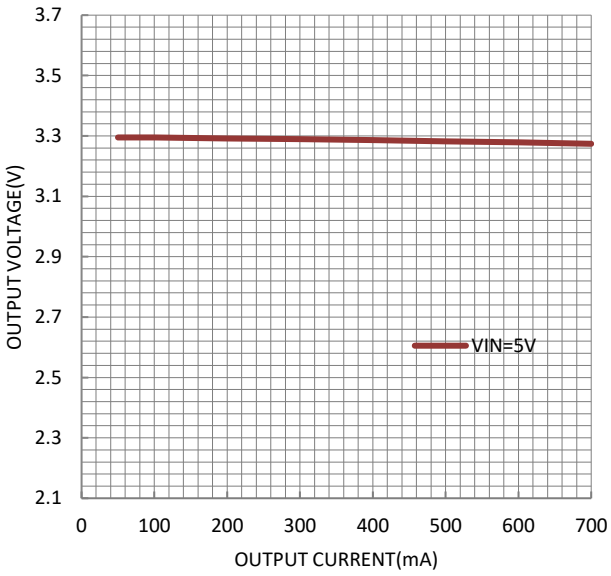


LV BUCK1:OUTPUT VOLTAGE VS OUTPUT CURRENT
(VOUT=1.5V)

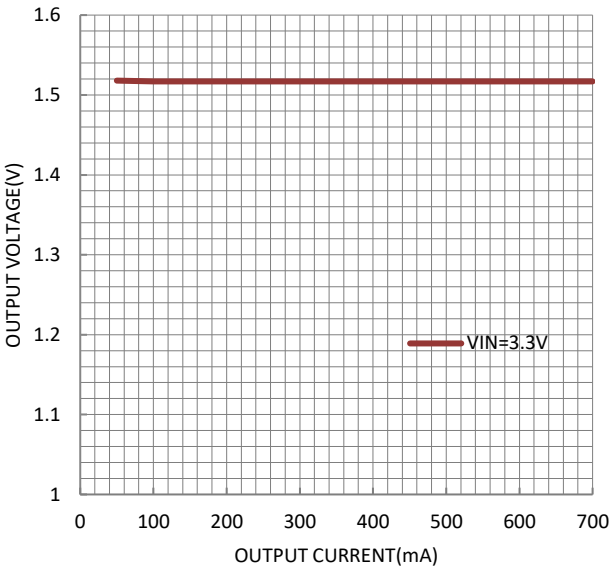


5-CH High-Efficiency PMIC

LDO1:OUTPUT VOLTAGE VS OUTPUT CURRENT
(VIN=5V,VOUT=3.3V)

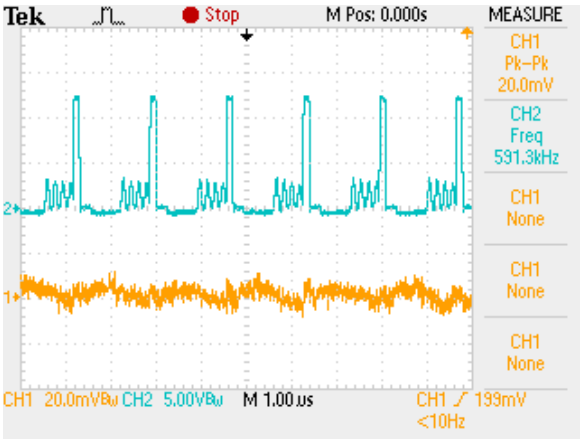


LDO2:OUTPUT VOLTAGE VS OUTPUT CURRENT
(VIN=3.3V,VOUT=1.5V)

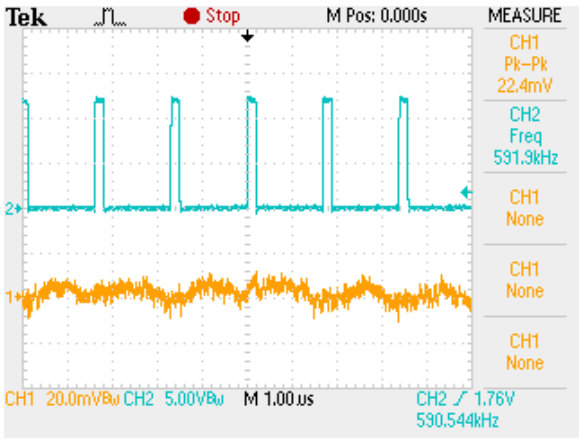


5-CH High-Efficiency PMIC

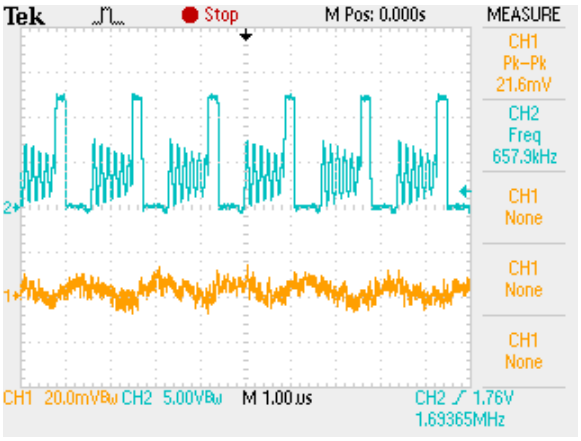
STEADY STATE OPERATION
HV BUCK1(VIN=12V,VOUT=1.2V,IOUT=100mA)



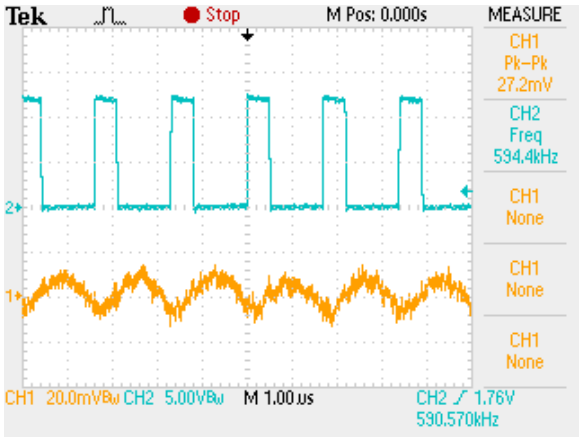
STEADY STATE OPERATION
HV BUCK1(VIN=12V,VOUT=1.2V,IOUT=1000mA)



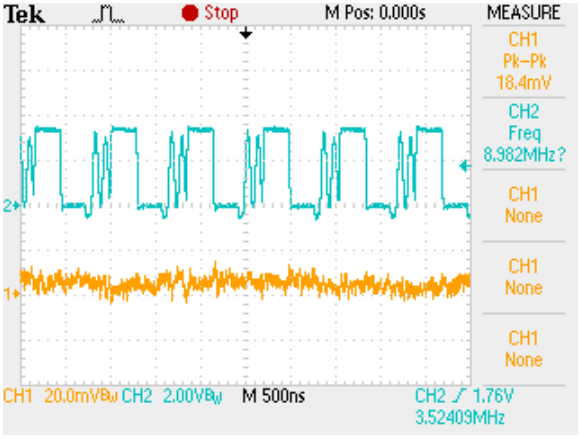
STEADY STATE OPERATION
HV BUCK2(VIN=12V,VOUT=3.3V,IOUT=100mA)



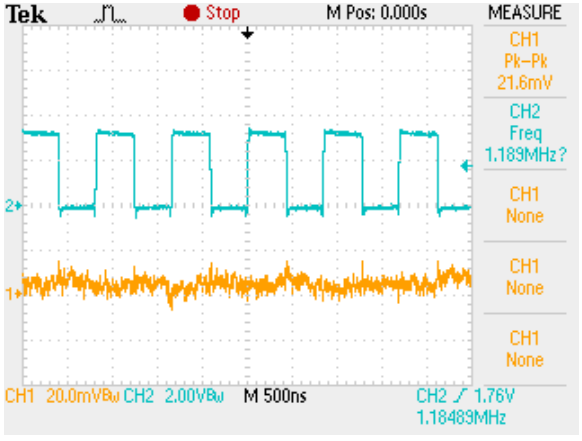
STEADY STATE OPERATION
HV BUCK2(VIN=12V,VOUT=3.3V,IOUT=1000mA)



STEADY STATE OPERATION
LV BUCK1(VIN=3.3V,VOUT=1.5V,IOUT=100mA)

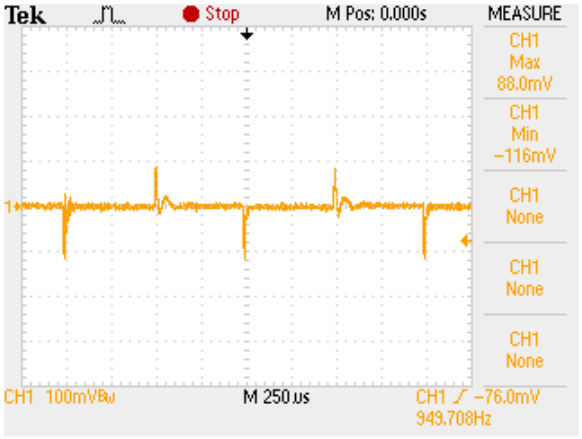


STEADY STATE OPERATION
LV BUCK1(VIN=3.3V,VOUT=1.5V,IOUT=1000mA)

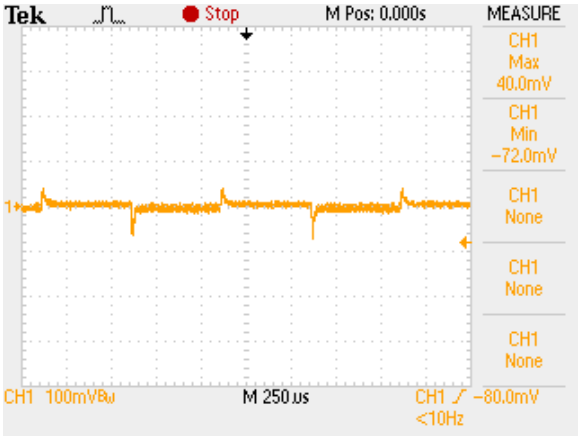


5-CH High-Efficiency PMIC

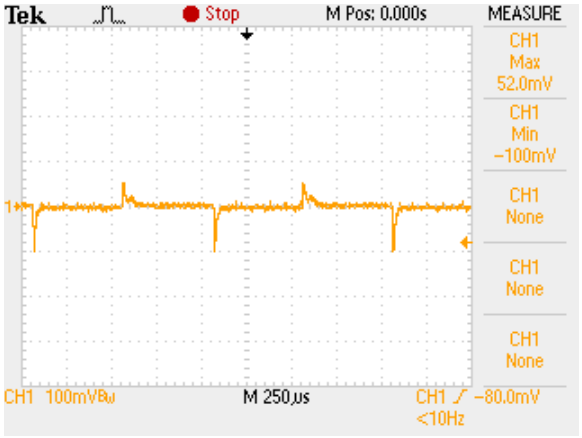
LOAD TRANSIENT RESPONSE
HV BUCK1
(VIN=12V,VOUT=1.2V,IOUT=100-1000mA,1A/uS)



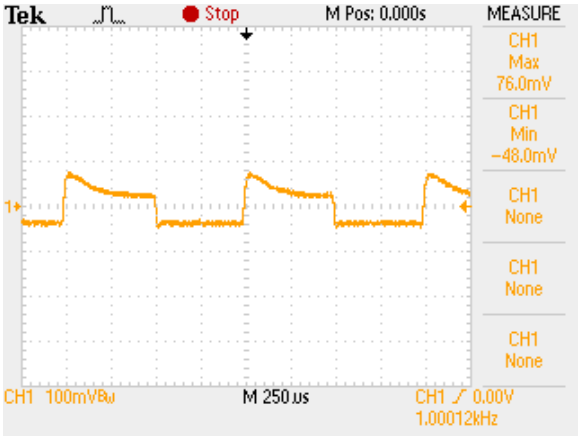
LOAD TRANSIENT RESPONSE
HV BUCK2
(VIN=12V,VOUT=3.3V,IOUT=100-1000mA,1A/uS)



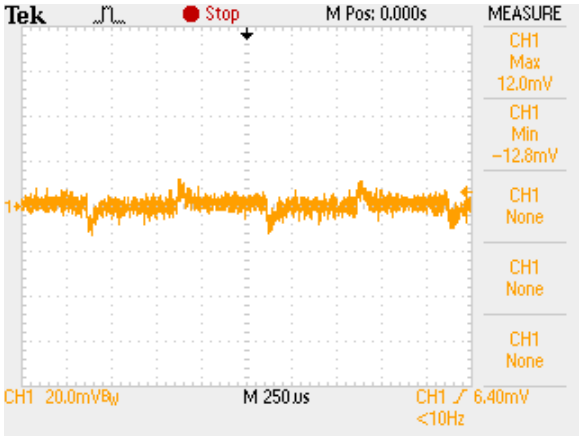
LOAD TRANSIENT RESPONSE
LV BUCK1
(VIN=3.3V,VOUT=1.5V,IOUT=100-1000mA,1A/uS)



LOAD TRANSIENT RESPONSE
LDO1
(VIN=5V,VOUT=3.3V,IOUT=50-300mA,1A/uS)

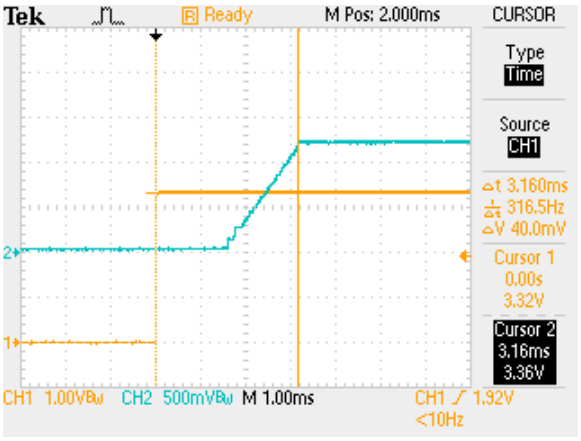


LOAD TRANSIENT RESPONSE
LDO2
(VIN=3.3V,VOUT=1.5V,IOUT=50-300mA,1A/uS)

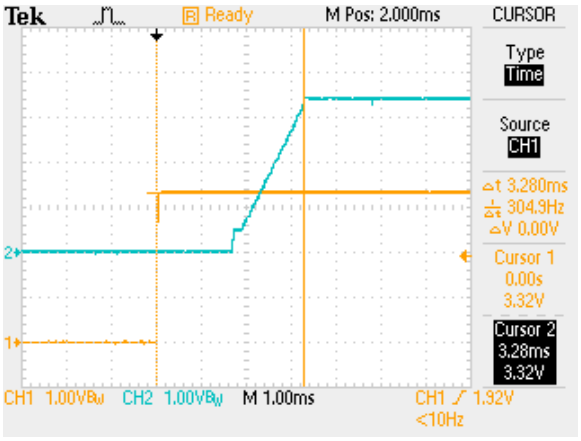


5-CH High-Efficiency PMIC

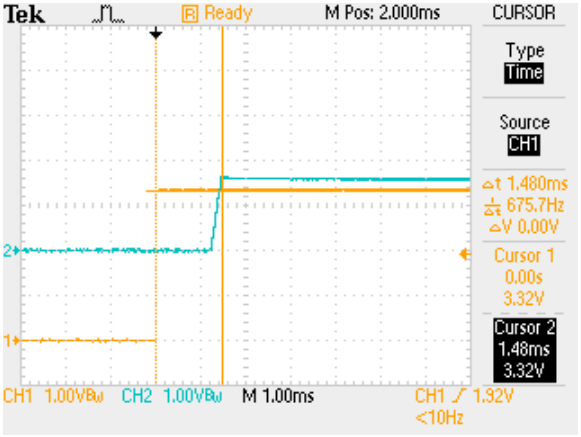
STRAT UP
HV BUCK1
(VIN=12V,VOUT=1.2V)



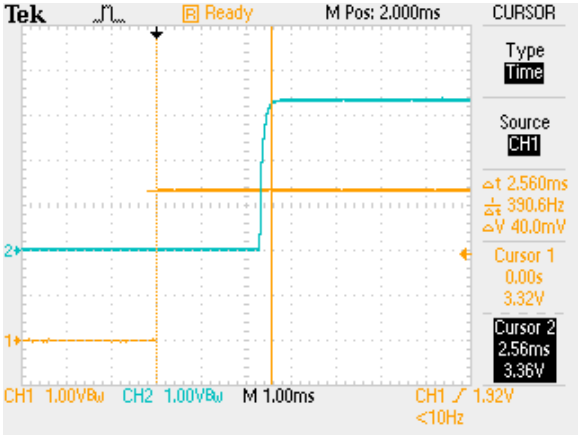
STRAT UP
HV BUCK2
(VIN=12V,VOUT=3.3V)



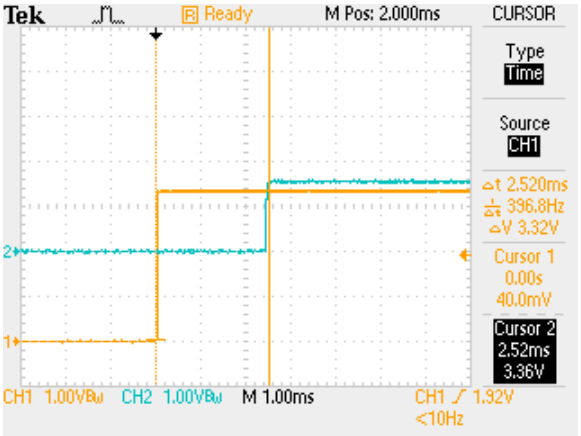
STRAT UP
LV BUCK1
(VIN=3.3V,VOUT=1.5V)



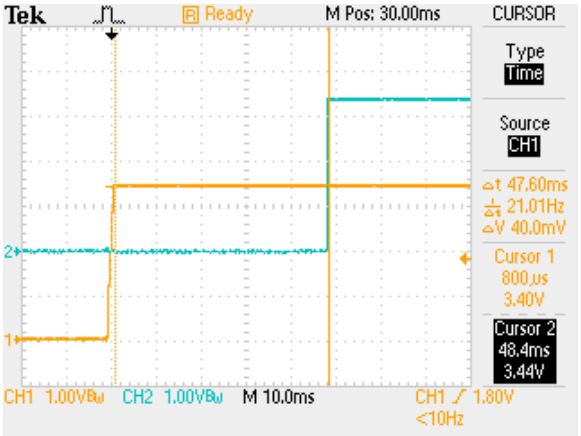
STRAT UP
LDO1
(VIN=5V,VOUT=3.3V)



STRAT UP
LDO2
(VIN=3.3V,VOUT=1.5V)



POK SIGNAL RISE FOLLOW HV BUCK2 START UP



Functions Description

Feature Description

RY1505 is a highly efficient and integrated Power Management IC for Systems-on-a-Chip (SoCs), ASICs, and processors. The device incorporates 3 high-efficiency synchronous buck regulators, and 2 LDOs that deliver 5 output voltages from a single power source. The device also includes a power on reset Block that provides a reset output signal.

Each of the buck regulators is specially designed for high-efficiency operation throughout the load range. With 600kHz (BUCK1, BUCK2) and 1.2MHz (BUCK3) typical switching frequency, the external L- C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.

BUCK3 can operate up to a 100% duty cycle allowing for the lowest possible input voltage that still maintains the regulation of the output. The lowest input to output dropout voltage is achieved by keeping the PMOS switch on. Additional features include soft-start, under-voltage lockout, bypass, and current and thermal overload protection. To reduce the input current ripple, the device employs a control circuit that operates the BUCK1 and BUCK2 at 90° phase. BUCKs are nearly identical in performance and mode of operation. They can operate in automatic mode (PWM/PFM). At very light loads, BUCKs enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Soft start

Each of converters has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady-state operating point, thus reducing startup stresses and surges. During startup, the switch current limit is increased in steps.

For BUCKs the soft start is implemented by increasing the switch current limit in steps that are gradually set higher. The startup time depends on the output capacitor size, load current and output voltage.

Current Limiting

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

Low Dropout Operation

BUCK3 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage:

$V_{IN\_MIN} = V_{OUT} + I_{LOAD} \times (R_{DSON\_HSFET} + R_{IND})$ where

- I_{LOAD} : Load Current
- R_{DSON_HSFET} : Drain to source resistance of MOSFET (high side)

- R_{IND} : Inductor resistance

Startup Sequence

Once V_{IN} reaches the UVLO threshold and the ENABLE pin= High BUCK1 and BUCK2 will start up. But *only when VDD4 be supplied*, BUCK3 and LDOs can start up.

POR

The RY1505 has POR pin to signal that BUCK2 output rails are valid. POR is Low if BUCK2 is disabled. If power OK condition is detected, then the POR pin will be set immediately.
1 condition is must be fulfilled:

- BUCK2 output is over flag level (90% when rising,85% when falling).

Under Voltage Lock Out (UVLO)

The V_{IN} voltage is monitored for a supply under voltage condition, for which the operation of the device cannot be guaranteed. The part will automatically disable PMIC. To prevent unstable operation, the UVLO has a hysteresis window. An under voltage lockout (UVLO) will disable BUCKs outputs, Once the supply voltage is above the UVLO hysteresis, the device will initiate a power-up sequence and then enter the active state.

Over Voltage Lock Out (OVLO)

The V_{IN} voltage is monitored for a supply over voltage condition, for which the operation of the device cannot be guaranteed. The purpose of OVLO is to protect the part and all other components connected to the PMIC outputs from any damage and malfunction. Once V_{IN} rises over about 20V BUCK1/BUCK2 will be disabled automatically. To prevent unstable operation, the OVLO has a hysteresis window. An over voltage lockout (OVLO) will force the device into the reset state, Once the supply voltage goes below the OVLO lower threshold, the device will initiate a power-up sequence and then enter the active state. BUCK1/BUCK2 operating maximum input voltage at which parameters are guaranteed is 20V. Absolute maximum of the device is 28V.

Thermal Shutdown (OTP)

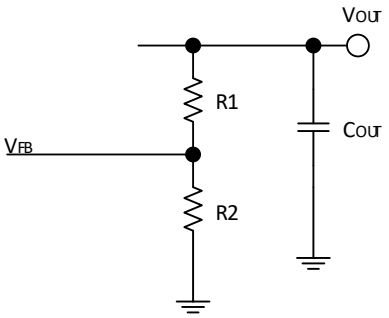
The temperature of the silicon die is monitored for an over-temperature condition, for which the operation of the device cannot be guaranteed. The part will automatically be disabled if the temperature is too high. The thermal shutdown (OTP) will force the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the OTP has a hysteresis window of about °02C. Once the temperature has decreased below the OTP hysteresis, the device will initiate a power-up sequence and then enter the active state. In the active state, the part will start up as if for the first time.

Detailed Design Procedure

External Components Selection

All 3 BUCKs require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. All 3 BUCKs are internally compensated and do not require external components to achieve stable operation. The output voltage of the 3 BUCKs and LDO2 can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$



Select $R1$ value around 50K Ω

$$R_2 = R_1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$$

Where V_{FB}

BUCKs: 0.6V

LDO2： 0.6V

Output Inductors and Capacitors Selection

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Over current ruggedness

The device has been optimized for use with nominal LC values as shown in the Application Diagram.

BUCK Power Supply Recommendations

The devices are designed to operate from BUCK1/BUCK2 input voltage supply range between 3.5 V and 18 V. This input supply must be well regulated. If the input supply is located more than a few inches, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47uF is a typical choice. VDD1,VDD2 and VDD3 must all be connected to input capacitors as close as possible.

BUCK Inductor Selection

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$I_{L(MAX)} = I_{LOAD(MAX)} + I_{RIPPLE}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

$D = \frac{V_{OUT}}{V_{IN}}$, F_S= 600kHz/1.2MHz, L = 4.7uH/2.2uH

where

- $I_{L(MAX)}$: Max inductor Current
- $I_{LOAD(MAX)}$: Max load current
- I_{RIPPLE}: Peak-to-Peak inductor current
- D: Estimated duty factor
- V_{IN}: Input voltage
- V_{OUT}: Output voltage
- F_S: Switching frequency, Hertz

Recommended Method for BUCK Inductor Selection

The best way to guarantee the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum device current limit, as specified in the Electrical Characteristics. In this case the device will prevent inductor saturation by going into current limit before the saturation level is reached.

Alternate Method for BUCK Inductor Selection

If the recommended approach cannot be used care must be taken to guarantee that the saturation current is greater than the peak inductor current:

$I_{SAT} > IL_{PEAK}$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

where

- I_{SAT}: Inductor saturation current at operating temperature
- I_{LPEAK}: Peak inductor current during worst case conditions
- I_{OUTMAX}: Maximum average inductor current
- I_{RIPPLE}: Peak-to-Peak inductor current
- V_{OUT}: Output voltage
- V_{IN}: Input voltage (HVVP1,HVVP2, LVVP1,LVVP2)
- L: Inductor value in Henries at I_{OUTMAX}
- F_S: Switching frequency, Hertz
- D: Estimated duty factor
- EFF: Estimated power supply efficiency

I_{SAT} may not be exceeded during any operation, including transients, startup, high temperature, worst case conditions, etc.

Output and Input Capacitors Characteristics

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table. The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a

temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47uF to 44uF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

BUCK Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can be usually neglected at the frequency ranges the switcher operates.

The output-filter capacitor smoothes out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

Note that the output voltage ripple increases with the inductor current ripple and the Equivalent Series Resistance of the output capacitor (ESR_{COUT}).Also note that the actual value of the capacitor's ESR_{COUT} is frequency and temperature dependent, as specified by its manufacturer. The ESR should be calculated at the applicable switching frequency and ambient temperature.

$$V_{OUT-RIPPLE-PP} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

Where

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output voltage ripple
- I_{RIPPLE}: estimated current ripple
- D: Estimated duty factor

Output ripple can be estimated from the vector sum of the reactive (capacitance) voltage component and the real (ESR) voltage component of the output capacitor:

$$V_{OUT-RIPPLE-PP} = \sqrt{{V_{ROUT}}^2 + {V_{COUT}}^2}$$

Where

$$V_{ROUT} = I_{RIPPLE} \times ESR_{OUT}$$

$$V_{OUT} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

where

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output ripple
- V_{ROUT}: estimated real output ripple
- V_{COUT}: estimated reactive output ripple

The device is designed to be used with ceramic capacitors on the outputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The recommended value for the output capacitors is 22µF, 6.3V with an ESR of 2mΩ or less. The output capacitors need to be mounted as close as possible to the output/ground terminals of the device.

BUCK Input Capacitor Selection

There are 3 buck regulators in the RY1505 device. Each of these buck regulators has its own input capacitor which should be located as close as possible to their corresponding V_{IN} and GND terminals, tantalum capacitor can also be located in the proximity of the device.

The input capacitor supplies the AC switching current drawn from the switching action of the internal power MOSFETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power. The input capacitor must be rated to handle this current:

$$V_{RMS\_CIN} = I_{OUT} \frac{\sqrt{{V_{ROUT}}^2 + {V_{COUT}}^2}}{V_{OUT}}$$

The power dissipated in the input capacitor is given by:

$$P_{D\_CIN} = {I_{RMS\_CIN}}^2 \times ESR_{CIN}$$

The device is designed to be used with ceramic capacitors on the inputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The minimum recommended value for the input capacitor is 10µF with an ESR of 10mΩ or less. The input capacitors need to be mounted as close as possible to the power/ground input terminals of the device.

The input power source supplies the average current continuously. During the high side MOSFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified “worst case” assumption is that all of the high side MOSFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current. Input ripple voltage is estimated as follows:

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F_S} + I_{OUT} \times \frac{\sqrt{{V_{ROUT}}^2 + {V_{COUT}}^2}}{V_{OUT}}$$

where

- V_{PPIN}: Estimated peak-to-peak input ripple voltage

- I_{OUT}: Output current
- C_{IN}: Input capacitor value
- ESR_{CIN}: *Input capacitor ESR*

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMS\_CIN} = \sqrt{D \times ({I_{OUT}}^2 + \frac{{I_{RIPPLE}}^2}{12})}$$

Where

- I_{RMSCIN}: Estimated input capacitor RMS current

LDO Output Capacitor Selection

The LDO is designed to be stable with a minimum 4.7μF output capacitor. No series resistor is required when using low ESR capacitors. For most applications, a 10μF ceramic capacitor is recommended. Larger values will improve transient response, and raise the power supply rejection ratio (PSRR) of the LDO. Refer to the Typical Performance Characteristics for the allowable range of output capacitor to ensure loop stability.

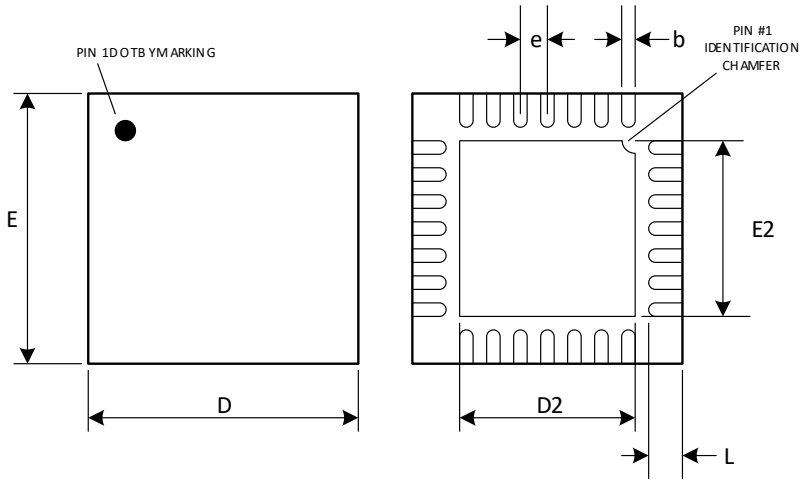
Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

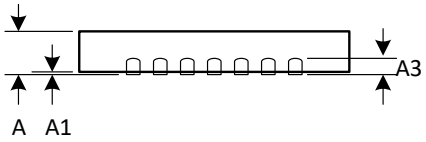
1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

Package Description

QFN28-4×4



TOP VIEW BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	W:VERY VERY THIN		
REF.	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.035	0.05
A3	0.203 REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
b	0.15	0.20	0.25
L	0.25	0.35	0.45
D2	2.70	2.80	2.90
E2	2.70	2.80	2.90
e	0.40 BSC		