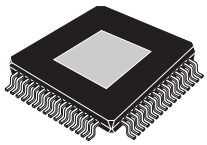
L5964

Automotive monolithic dual step-down switching regulator with LDO

Data brief



LQFP64
(exposed pad up)

Features

- AEC-Q100 qualified
- Two step-down synchronous switching voltage regulators with internal power switches:
  - Output voltage selectable by external divider (feedback voltage at 0.9 V)
  - Minimum and maximum output is limited by minimum and maximum duty cycle
  - Internal high-side/ low-side NDMOS
  - 270 kHz and 2.2 MHz selectable free-run frequencies
  - 125 kHz < f < 2.3 MHz synchronization range at SYNCIN pin
  - Programmable current limits at 2 A and 3.5A (> 2 A requires the addition of external schottky diodes)
  - Independent hardware enabling pins
  - Independent supply inputs
  - 180° phase shift between outputs
  - Synch out 90° phase shift vs DC-DC1
  - Programmable switching frequency divider by 1, 2, 4, 8 between the two regulators
  - The two buck converters can be connected in parallel (for evaluation purposes only)
- Independent voltage supervisors/power-goods with selectable thresholds through external pin:
  - two available thresholds for UV/OV/PG signals: 90-120-95% or 80-110-85% (output voltage percentage)
- Soft-start, thermal protection
- One standby/linear regulator:
  - Output selectable with external resistor divider till 10 V
  - Soft start, hardware enable pin
  - 250 mA maximum current capability
  - Standby operative mode
  - Programmable power good thresholds (85% or 95% output voltage percentage)
  - Thermal protection
- Microcontroller reset with programmable duration, activated by output under voltage or watchdog fault
- External High Side Driver enable pin
- One integrated window watchdog (5 ms ≤ window ≤ 50 ms, with ± 20% tolerance)
- Short circuit protected outputs
- Low external components number
- Thermal shutdown junction temperature 150°C

Table 1. Device summary

Order code	Package	Packing
L5964L-VYY	LQFP64 exp. pad up	Tray

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1 Description

L5964 is a dual step-down switching regulator with internal power switches and a low drop-out linear/standby regulator. All the regulators have independent supply voltages, enables, power goods and thermal protections.

The switching regulators have selectable voltage supervisors and power goods, and selectable current limits. The LDO has power good and fixed current limitation.

The two DC-DC converters can work in free-run condition, with frequency selectable between two values, 270 kHz or 2.2 MHz, or synchronize themselves to an external clock (SYNCIN pin). They are 180° out of phase, while the synchronization output signal (SYNCOUT pin) is 90° out of phase with the first regulator. The phase shift simplifies the use of two ICs in the same application (4 DC/DCs regulators).

DC-DC1 and DC-DC2 current limits can be independently set through the pins OCPSET1 and OCPSET2 respectively. Two current limits are available, 2 A (1.7 A min) and 3.5 A (3.7 A min). For operation > 2 A, 20 V, with less than 0.5 V forward voltage and 2 A at room temperature, Schottky diodes placed as close to the PHASE1/2 pins as possible, to ground are required.

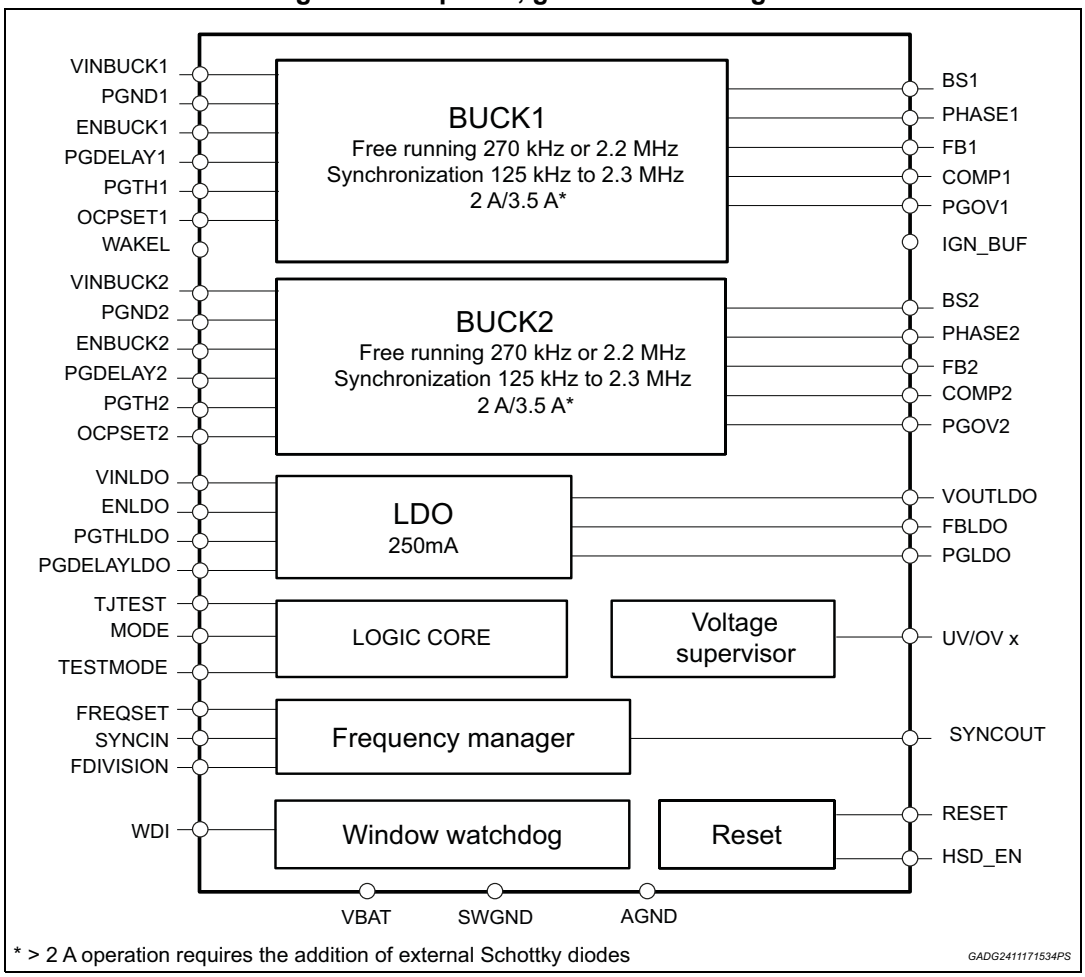
The high operating frequency allowed by the synchronization input helps to reduce AM and FM interferences and grants the use of small and low cost inductors and capacitors.

The L5964 can manage the microcontroller supply. A configurable reset output and a configurable watchdog input are available.

This IC finds application in the automotive segment, where load dump protection and wide input voltage range are mandatory. L5964 has been qualified for car passenger cars, with a standard 14 V battery. The total quiescent current, when both DC/DCs and LDO are disabled, is less than 10 µA.

The product is available in LQFP64 exposed pad up package. The slug, whenever possible, has to be connected to the ground plane.

Figure 1. Simplified, general block diagram



2 Pins description

2.1 LQFP64 pins description

Figure 2. LQFP64 pinout (bottom view)

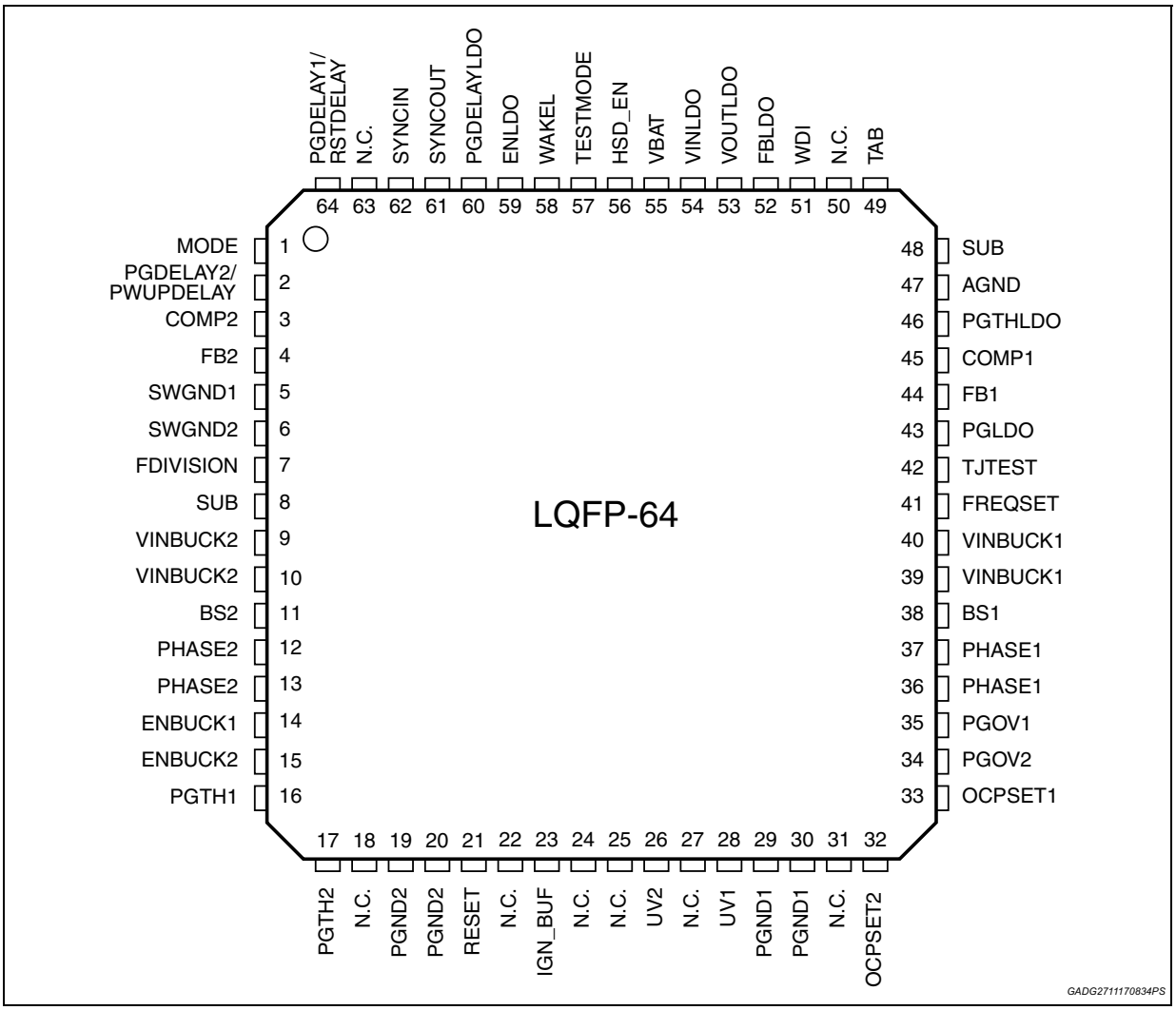


Table 2. LQFP64 pin list

N#	Pin name	Pin type	Pin description
1	MODE	IN	Working mode: Pin floating sets the working Mode to Normal; shorted to AGND sets the Microcontroller Mode.
2	PGDELAY2/ PWUPDELAY	IN	DC/DC2 Power good output delay time adjustable by connecting a capacitor from PGDELAY2 to AGND. In Microcontroller Mode, a capacitor sets the power up delay, from reset to watchdog input.
3	COMP2	IN/OUT	DC/DC2 Error amplifier output for compensation network connection.
4	FB2	IN/OUT	DC/DC2 Output feedback. Connected to an error amplifier that compares the feedback voltage to the internal reference voltage.

Table 2. LQFP64 pin list (continued)

N#	Pin name	Pin type	Pin description
5	SWGND1	GROUND	DC/DC analog blocks ground (Switching ground).
6	SWGND2	GROUND	DC/DC analog blocks ground (Switching ground).
7	FDIVISION	IN	Frequency divider setting to make DC/DC2 working at a frequency that is 1/1, 1/2, 1/4 or 1/8 of DC/DC1 one. If connected to ground, puts the device in parallel mode (for evaluation purposes only).
8	SUB	GROUND	Device substrate ground.
9	VINBUCK2	SUPPLY	DC/DC2 power supply connection.
10	VINBUCK2	SUPPLY	DC/DC2 power supply connection.
11	BS2	OUT	Boot-strap capacitor connection for DC/DC2.
12	PHASE2	OUT	DC/DC2 power stage output (for external inductor and boot-strap capacitor connection).
13	PHASE2	OUT	DC/DC2 power stage output (for external inductor and boot-strap capacitor connection).
14	ENBUCK1	IN	DC/DC1 enable (active high).
15	ENBUCK2	IN	DC/DC2 enable (active high).
16	PGTH1	IN	Power good threshold setting for DC/DC1. Pin floating sets the threshold to 95% of Vout; shorted to AGND sets the threshold to 85% of Vout.
17	PGTH2	IN	Power good threshold setting for DC/DC2. Pin floating sets the threshold to 95% of Vout; shorted to AGND sets the threshold to 85% of Vout.
18	N.C.	-	Not Connected.
19	PGND2	GROUND	Power ground of DC/DC2. Connected to internal low-side source.
20	PGND2	GROUND	Power ground of DC/DC2. Connected to internal low-side source.
21	RESET	OUT	Reset signal to Microprocessor in Microcontroller Mode: in Normal mode is kept in high impedance state. Open-drain output.
22	N.C.	-	Not Connected.
23	IGN_BUF	OUT	DC/DC1 status (ON/OFF) echo to Microprocessor in Microcontroller Mode: in Normal Mode is kept in high impedance. Open-drain output.
24	N.C.	-	Not Connected.
25	N.C.	-	Not Connected.
26	UV2	OUT	Under-voltage DC/DC2 signal. Open-drain output.
27	N.C.	-	Not Connected.
28	UV1	OUT	Under-voltage DC/DC1 signal. Open-drain output.
29	PGND1	GROUND	Power ground of DC/DC1. Connected to internal low-side source.
30	PGND1	GROUND	Power ground of DC/DC1. Connected to internal low-side source.
31	N.C.	-	Not Connected.
32	OCPSET2	IN	Programmable OCP setting for DC/DC2. Pin floating sets the overcurrent threshold to 4A; shorted to AGND sets the threshold to 2 A.

Table 2. LQFP64 pin list (continued)

N#	Pin name	Pin type	Pin description
33	OCPSET1	IN	Programmable OCP setting for DC/DC1. Pin floating sets the overcurrent threshold to 4A; shorted to AGND sets the threshold to 2 A.
34	PGOV2	OUT	Over-voltage DC/DC2 signal. Open-drain output.
35	PGOV1	OUT	Over-voltage DC/DC1 signal. Open-drain output.
36	PHASE1	OUT	DC/DC1 power stage output (for external inductor and boot-strap capacitor connection).
37	PHASE1	OUT	DC/DC1 power stage output (for external inductor and boot-strap capacitor connection).
38	BS1	OUT	Boot-strap capacitor connection for DC/DC1.
39	VINBUCK1	SUPPLY	DC/DC1 power supply connection.
40	VINBUCK1	SUPPLY	DC/DC1 power supply connection.
41	FREQSET	IN	Programmable internal PWM frequency for DC/DC. Pin floating sets the frequency to 2M Hz; shorted to AGND sets the frequency to 250 kHz and inhibits FDIVISION.
42	TJTEST	OUT	Device junction temperature information.
43	PGLDO	OUT	LDO regulator Power good output. Open-drain output.
44	FB1	IN/OUT	DC/DC1 Output feedback. Connected to error amplifier that compares the feedback voltage to the internal reference voltage.
45	COMP1	IN/OUT	DC/DC1 Error amplifier output for compensation network connection.
46	PGTHLDO	IN	Power good threshold setting for LDO. Pin floating sets the threshold to 95% of VOUTLDO; shorted to AGND sets the threshold to 85% of VOUTLDO.
47	AGND	GROUND	Device analog ground.
48	SUB	GROUND	Device substrate ground.
49	TAB	-	Device slug connection.
50	N.C.	-	Not Connected.
51	WDI	IN	Watchdog input from Microcontroller. Internal Pull Down.
52	FBLDO	IN/OUT	LDO regulator output feedback.
53	VOUTLDO	OUT	LDO regulator output.
54	VINLDO	SUPPLY	LDO regulator power supply.
55	VBAT	SUPPLY	Dedicated high voltage supply for reference blocks.
56	HSD_EN	OUT	Enable signal for external High Side switch (active low). Only active in microcontroller mode, high impedance in normal mode.
57	TESTMODE	IN	TESTMODE pin, reserved use. Connect to ground.
58	WAKEL	IN	Wake-up signal to enable DC/DC1 in OR internally with ENBUCK1 pin (ignored in Normal Mode, active low in Microcontroller Mode).
59	ENLDO	IN	LDO regulator enable (active high).

Table 2. LQFP64 pin list (continued)

N#	Pin name	Pin type	Pin description
60	PGDELAYLDO	IN	LDO Power good output delay time adjustable by connecting a capacitor to AGND.
61	SYNCOUT	OUT	External Switching clock output signal.
62	SYNCIN	IN	External clock input connection. Connect an external clock at SYNCIN for frequency synchronization.
63	N.C.	-	Not Connected.
64	PGDELAY1/ RSTDELAY	IN	DC/DC1 Power good output delay time adjustable by connecting a capacitor from PGDELAY1 to AGND. In Microcontroller Mode, a capacitor sets the power up delay, from reset to watchdog input.

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK is an ST trademark.

3.1 LQFP64 (10x10x1.4 mm exp. pad up) package information

Figure 3. LQFP64 (10x10x1.4 mm exp. pad up) package outline

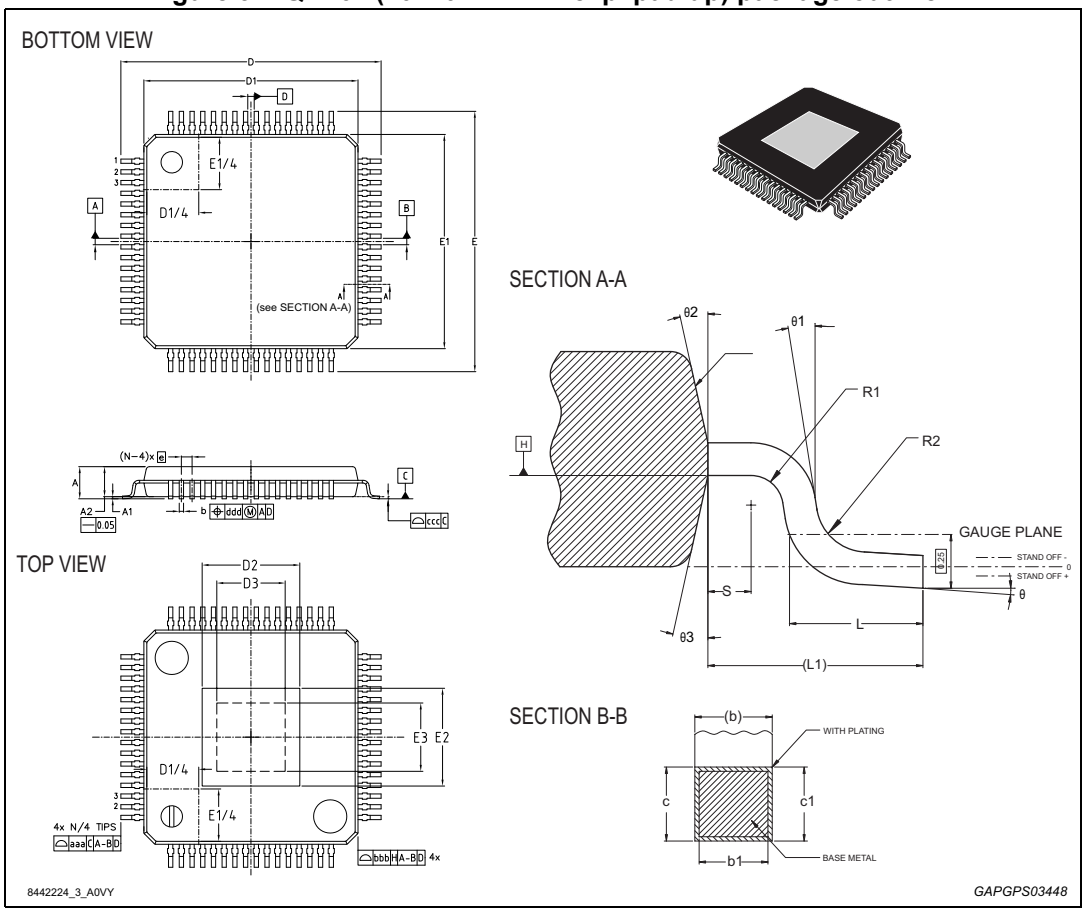


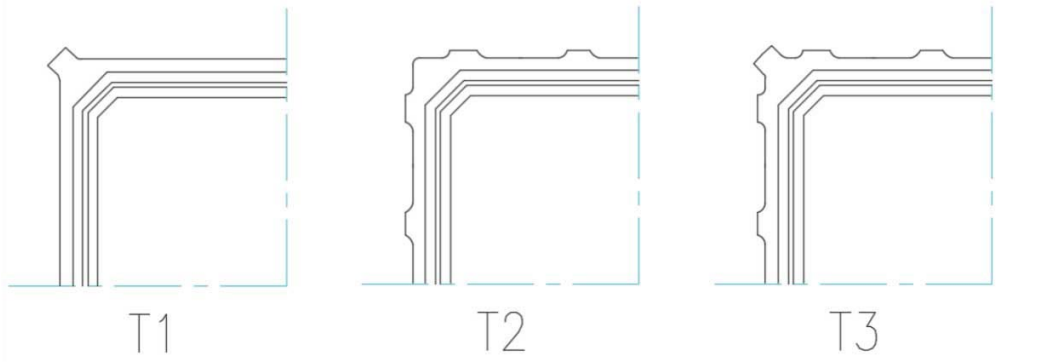
Table 3. LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	6°
Θ1	0°	9°	12°
Θ2	11°	12°	13°
Θ3	11°	12°	13°
A	-	-	1.49
A1	-0.04	-	0.04
A2	1.35	1.4	1.45
b	-	-	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	0.127	0.16
D	12.00 BSC		
D1(1) (2)	10.00 BSC		
D2	**See VARIATIONS**		
e	0.50 BSC		
E	12.00 BSC		
E1(1) (2)	10.00 BSC		
E2	**See VARIATIONS**		
L	0.45	0.60	0.75
L1	1.00 REF		
N	-	64	-
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Tolerance of form and position			
aaa	-	0.20	-
bbb	-	0.20	-
ccc	-	0.08	-
ddd	-	0.08	-

Table 3. LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data (continued)

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
VARIATIONS			
Pad option 6.0x6.0 (T1-T3)(3)			
D2	-	-	6.61
E2	-	-	6.61
D3	4.8	-	-
E3	4.8	-	-

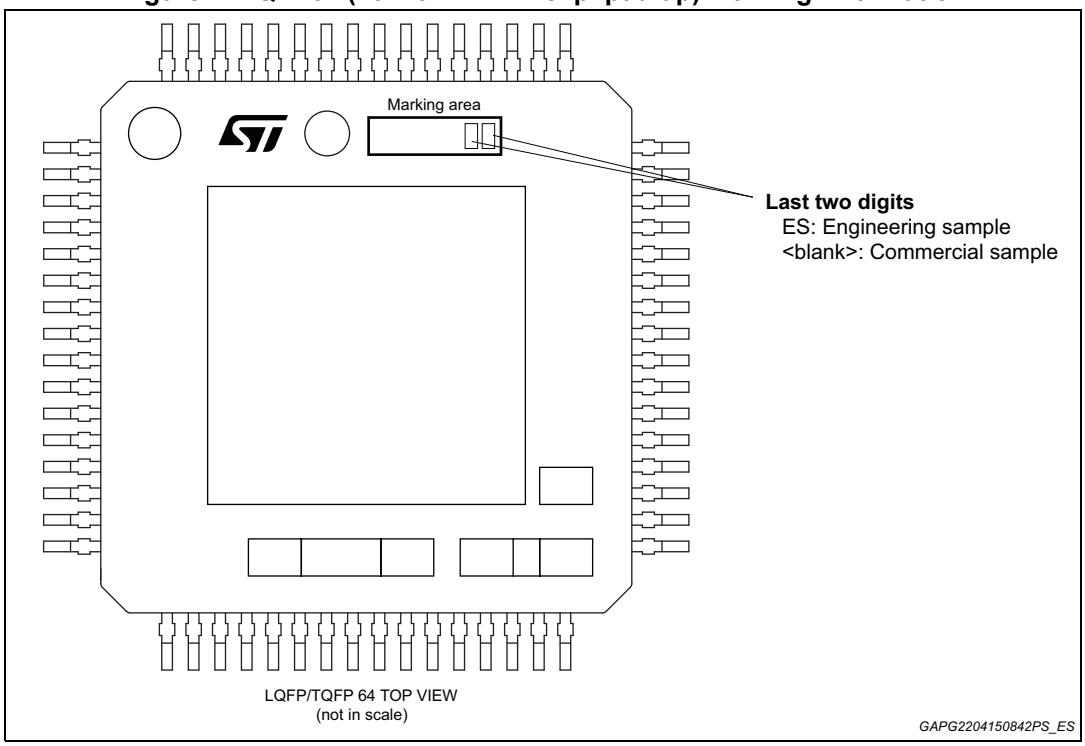
1. Dimensions D1 and E1 do not include mold flash or protrusions.
   Allowable mold flash or protrusion is “0.25 mm” per side.
2. The Top package body size may be smaller than the bottom package size by much as 0.15 mm.
3. Number, dimensions and position of shown groves are for reference only:



GADG2108170827PS

3.2 Package marking information

Figure 4. LQFP64 (10x10x1.4 mm exp. pad up) marking information



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
24-Feb-2022	1	Initial release.