

M5M5V208AKV/KR

PRELIMINARY

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Some parametric limits are subject to change

2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V208A is a family of low voltage 2-Mbit static RAMs organized as 262,144-words by 8-bit, fabricated by Mitsubishi's high-performance 0.25µm CMOS technology.

The M5M5V208A is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The M5M5V208A is packaged in 32-pin 8mm x 13.4mm STSOP packages. Two types of STSOPs are available, M5M5V208AKV (normal-lead-bend STSOP) and M5M5V208AKR (reverse-lead-bend STSOP). These two types STSOPs are suitable for a surface mounting on double-sided printed circuit boards.

From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version". Those are summarized in the part name table below.

FEATURES

- Single 2.7 ~ 3.6V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by $\overline{S1}$ & $\overline{S2}$
- Data retention supply voltage=2.0V
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Small stand-by current 0.3µA(typ.)

PACKAGE

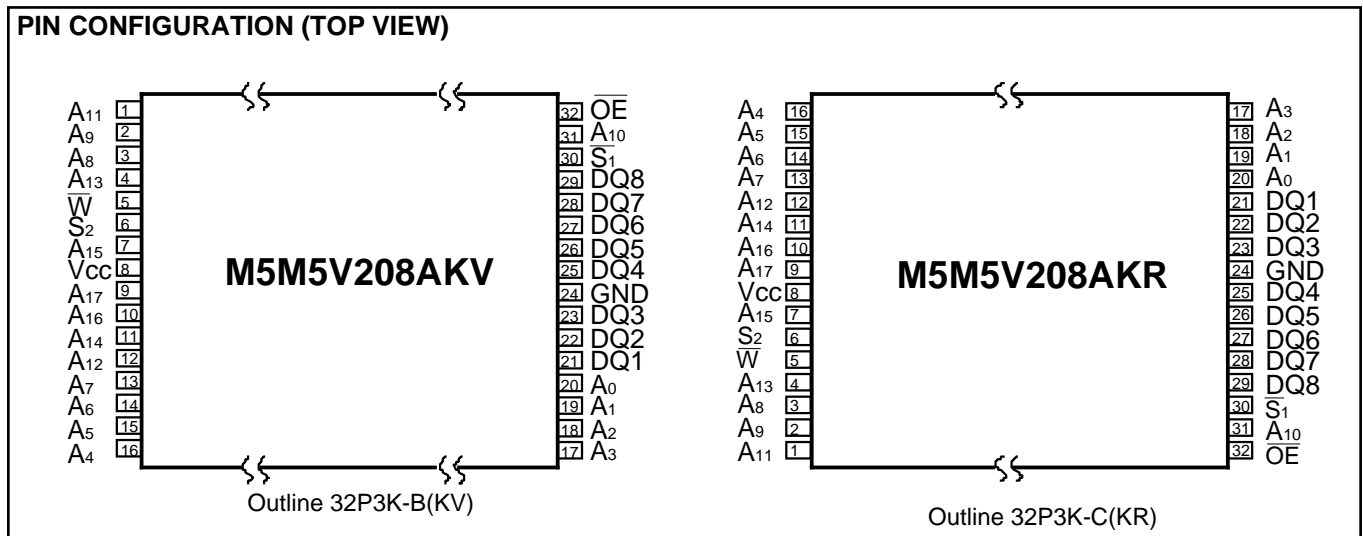
M5M5V208AKV,KR : 32pin 8 X 13.4 mm TSOP

PART NAME TABLE

Version, Operating temperature	Part name (## stands for "KV" or "KR")	Power Supply	Access time max.	Stand-by current I _{cc} (PD), V _{CC} =3.0V						Active current I _{cc} 1 (3.0V, typ.)
				typical *		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5V208A## -55L	2.7 ~ 3.6V	55ns	---	---	---	---	20µA	---	20mA (f=10MHz) 3mA (f=1MHz)
	M5M5V208A## -70L		70ns	---	---	---	---	---		
	M5M5V208A## -55H	2.7 ~ 3.6V	55ns	0.3µA	---	1µA	3µA	8µA	---	
	M5M5V208A## -70H		70ns	---	---	---	---	---		
W-version -20 ~ +85°C	M5M5V208A## -55LW	2.7 ~ 3.6V	55ns	---	---	---	---	20µA	50µA	
	M5M5V208A## -70LW		70ns	---	---	---	---	---		
	M5M5V208A## -55HW	2.7 ~ 3.6V	55ns	0.3µA	---	1µA	3µA	8µA	24µA	
	M5M5V208A## -70HW		70ns	---	---	---	---	---		
I-version -40 ~ +85°C	M5M5V208A## -55LI	2.7 ~ 3.6V	55ns	---	---	---	---	20µA	50µA	
	M5M5V208A## -70LI		70ns	---	---	---	---	---		
	M5M5V208A## -55HI	2.7 ~ 3.6V	55ns	0.3µA	---	1µA	3µA	8µA	24µA	
	M5M5V208A## -70HI		70ns	---	---	---	---	---		

* "typical" parameter is sampled, not 100% tested.

PIN CONFIGURATION (TOP VIEW)



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FUNCTION

The operation mode of the M5M5V208A is determined by a combination of the device control inputs \overline{S}_1 , S_2 , \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write cycle is executed whenever the low level \overline{W} overlaps with the low level \overline{S}_1 and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , \overline{S}_1 or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

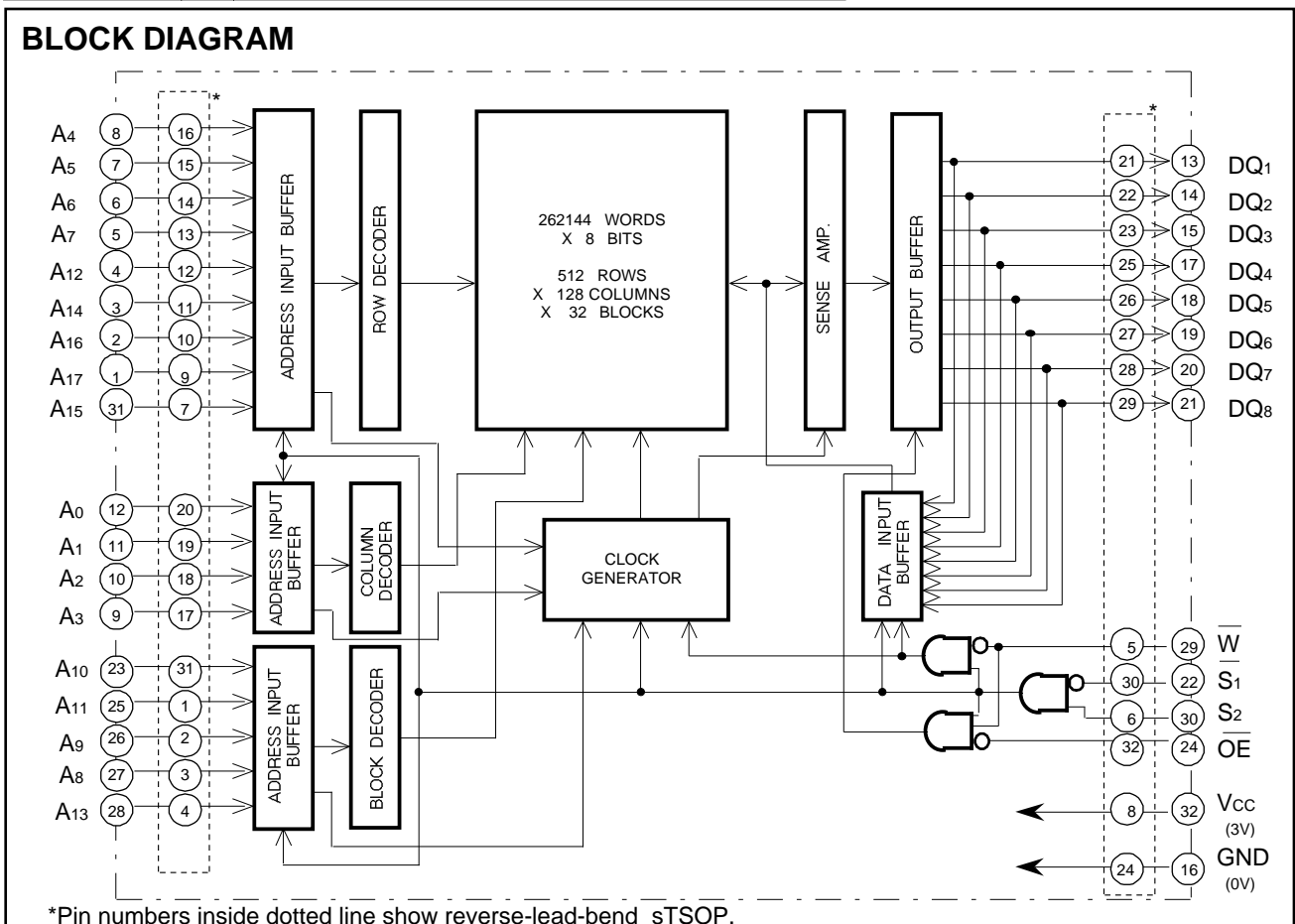
A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while \overline{S}_1 and S_2 are in an active state ($\overline{S}_1 = L, S_2 = H$).

When setting \overline{S}_1 at a high level or S_2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \overline{S}_1 or S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{cc3} or I_{cc4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

\overline{S}_1	S_2	\overline{W}	\overline{OE}	Mode	DQ	I_{cc}
X	L	X	X	Non selection	High-impedance	Standby
H	X	X	X	Non selection	High-impedance	Standby
L	H	L	X	Write	D_{IN}	Active
L	H	H	L	Read	D_{OUT}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



M5M5V208AKV/KR**PRELIMINARY**Notice: This is not a final specification.
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Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	- 0.5*~4.6	V
V _I	Input voltage		- 0.5* ~ V _{CC} + 0.5 (Max 4.6)	V
V _O	Output voltage		0 ~ V _{CC}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature	Standard	0 ~ 70	°C
		W - Version	- 20 ~ 85	°C
		I - Version	- 40 ~ 85	°C
T _{str}	Storage temperature		- 65 ~ 150	°C

* - 3.0V in case of AC (Pulse width 30ns)

DC ELECTRICAL CHARACTERISTICS(V_{CC}= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V _{IH}	High-level input voltage		2.0		V _{CC} +0.3V	V	
V _{IL}	Low-level input voltage		- 0.3*		0.6	V	
V _{OH1}	High-level output voltage 1	I _{OH} = - 0.5mA	2.4			V	
V _{OH2}	High-level output voltage 2	I _{OH} = - 0.05mA	V _{CC} -0.5V			V	
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	V	
I _I	Input current	V _I =0 ~ V _{CC}			±1	µA	
I _O	Output current in off-state	$\overline{S_1}=V_{IH}$ or $S_2=V_{IL}$ or $\overline{OE}=V_{IH}$ V _{I/O} =0 ~ V _{CC}			±1	µA	
I _{CC1}	Active supply current (CMOS-level Input)	$\overline{S_1}$ 0.2V, S ₂ V _{CC} -0.2V, other inputs 0.2V or V _{CC} -0.2V,output-open	f= 10MHz	20	25	mA	
			f= 5MHz	10	13		
			f= 1MHz	3	5		
I _{CC2}	Active supply current (TTL-level Input)	$\overline{S_1}=V_{IL}$, S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} output-open	f= 10MHz	22	27	mA	
			f= 5MHz	12	15		
			f= 1MHz	3	5		
I _{CC3}	Stand-by current	1) S ₂ 0.2V, other inputs=0 ~ V _{CC} or 2) $\overline{S_1}$ V _{CC} -0.2V, S ₂ V _{CC} -0.2V other inputs=0 ~ V _{CC}	-L		60	µA	
			-H	~+25°C	0.3		2
			-HW	~+40°C			5
			-HI	~+70°C			10
			-HW / I	~+85°C			30
I _{CC4}	Stand-by current	$\overline{S_1}=V_{IH}$ or S ₂ =V _{IL} , other inputs=0 ~ V _{CC}			0.33	mA	

* - 3.0V in case of AC (Pulse width 30ns)

CAPACITANCE(V_{CC}= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			8	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is for V_{CC} = 3V, T_a = 25°C

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V_{CC} 2.7 ~ 3.6V
 Input pulse level V_{IH}=2.2V, V_{IL}=0.4V
 Input rise and fall time 5ns
 Reference level V_{OH}=V_{OL}=1.5V
 Output loads Fig.1, CL=30pF

CL=5pF (for t_{en}, t_{dis})

Transition is measured ±500mV from steady
 state voltage. (for t_{en}, t_{dis})

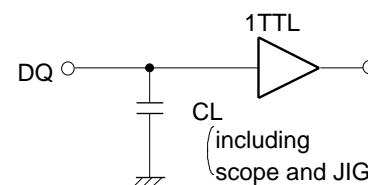


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits				Unit
		-55L,H		-70L,H		
		Min	Max	Min	Max	
t _{CR}	Read cycle time	55		70		ns
t _a (A)	Address access time		55		70	ns
t _a (S ₁)	Chip select 1 access time		55		70	ns
t _a (S ₂)	Chip select 2 access time		55		70	ns
t _a (OE)	Output enable access time		30		35	ns
t _{dis} (S ₁)	Output disable time after S ₁ high		20		25	ns
t _{dis} (S ₂)	Output disable time after S ₂ low		20		25	ns
t _{dis} (OE)	Output disable time after OE high		20		25	ns
t _{en} (S ₁)	Output enable time after S ₁ low	10		10		ns
t _{en} (S ₂)	Output enable time after S ₂ high	10		10		ns
t _{en} (OE)	Output enable time after OE low	5		5		ns
t _v (A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits				Unit
		-55L,H		-55L,H		
		Min	Max	Min	Max	
t _{cw}	Write cycle time	55		70		ns
t _w (W)	Write pulse width	45		55		ns
t _{su} (A)	Address setup time	0		0		ns
t _{su} (A-WH)	Address setup time with respect to \bar{W}	50		65		ns
t _{su} (S ₁)	Chip select 1 setup time	50		65		ns
t _{su} (S ₂)	Chip select 2 setup time	50		65		ns
t _{su} (D)	Data setup time	25		30		ns
t _h (D)	Data hold time	0		0		ns
t _{rec} (W)	Write recovery time	0		0		ns
t _{dis} (W)	Output disable time from \bar{W} low		20		25	ns
t _{dis} (OE)	Output disable time from OE high		20		25	ns
t _{en} (W)	Output enable time from \bar{W} high	5		5		ns
t _{en} (OE)	Output enable time from OE low	5		5		ns

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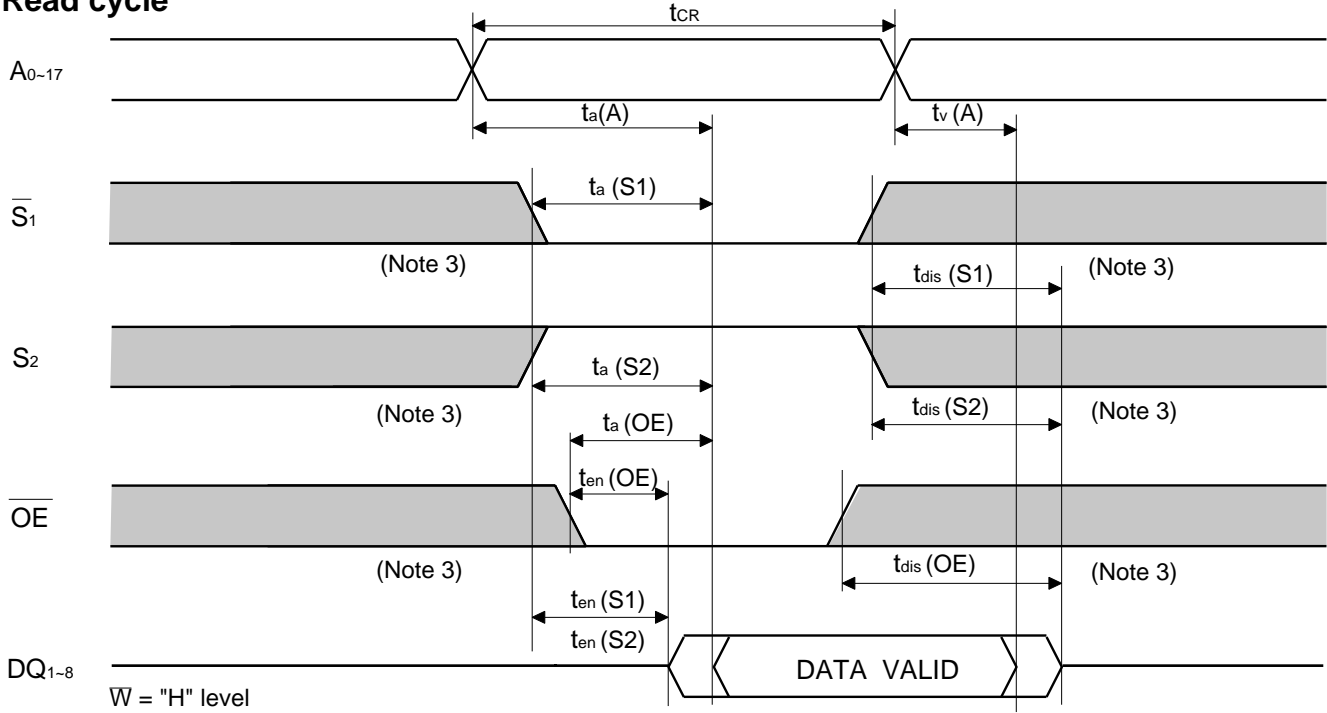
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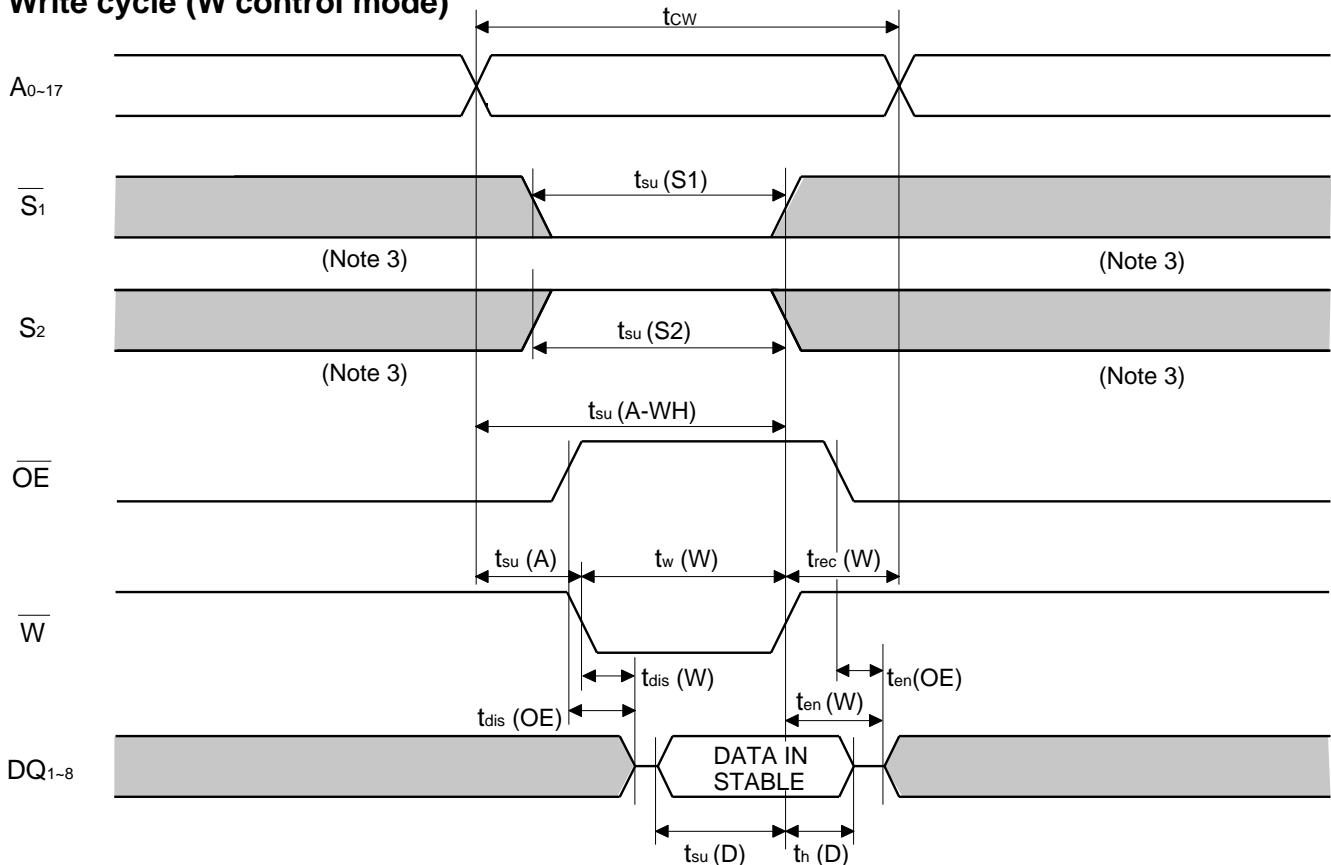
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(4) TIMING DIAGRAMS

Read cycle



Write cycle (\overline{W} control mode)



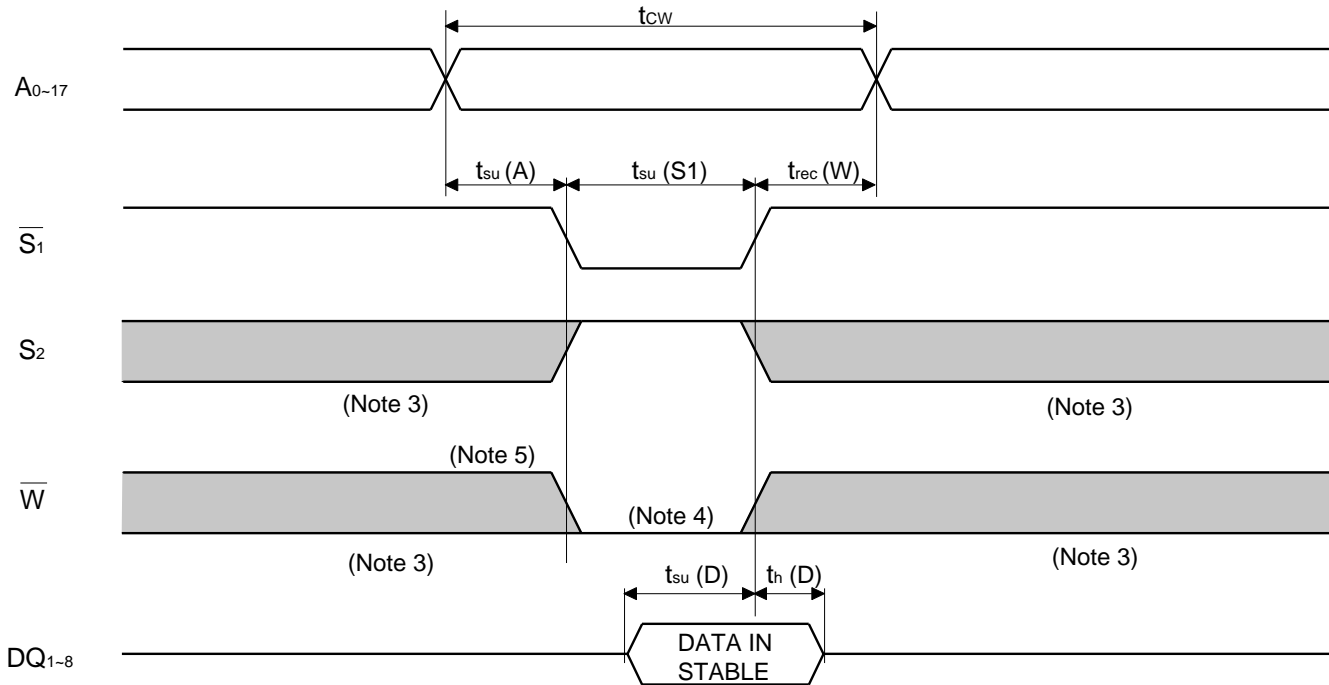
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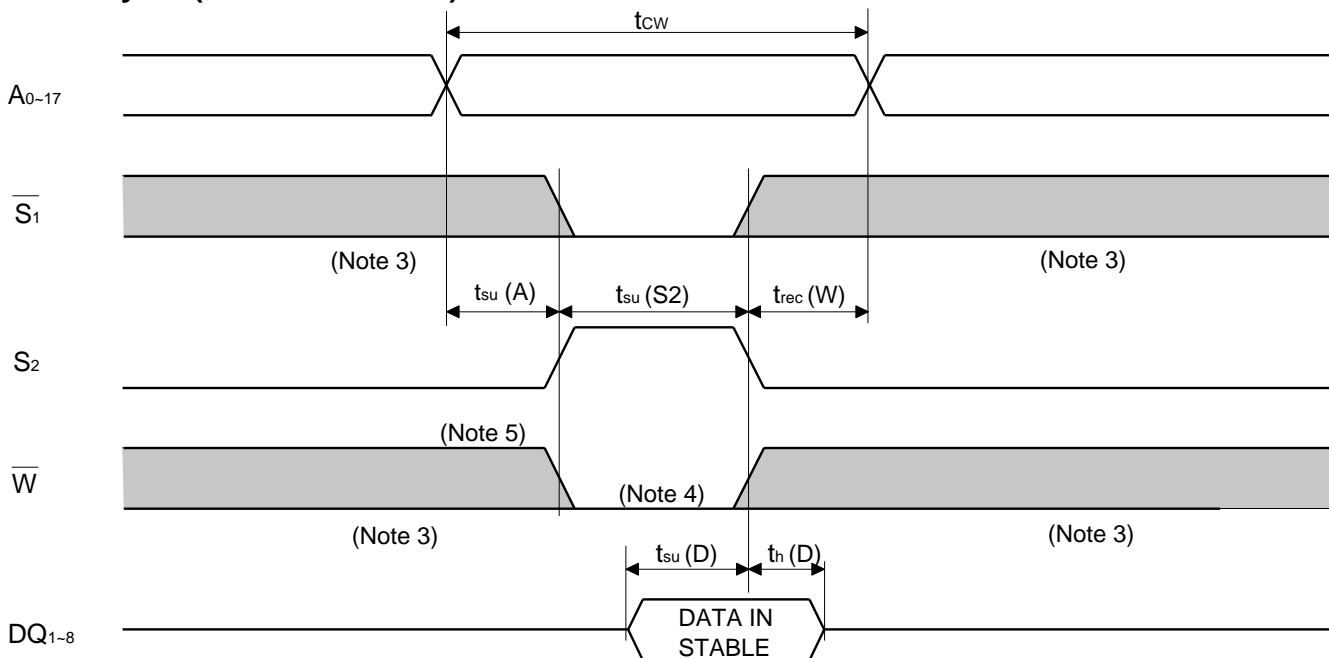
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Write cycle ($\overline{S1}$ control mode)



Write cycle ($S2$ control mode)



Note 3: Hatching indicates the state is "don't care".

4: Writing is executed while $S2$ high overlaps $\overline{S1}$ and \overline{W} low.

5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of $S2$, the outputs are maintained in the high impedance state.

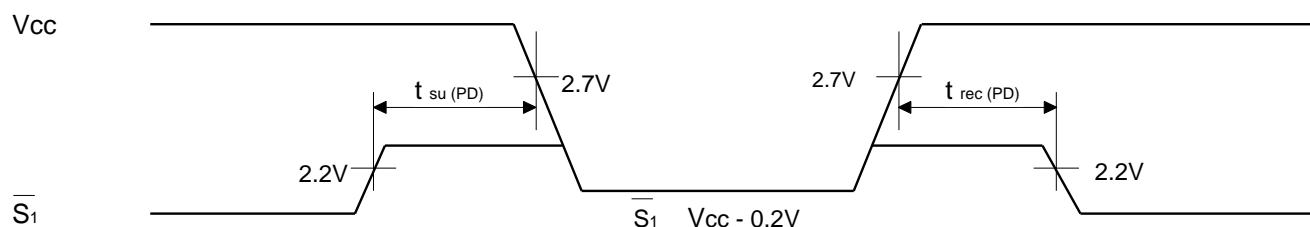
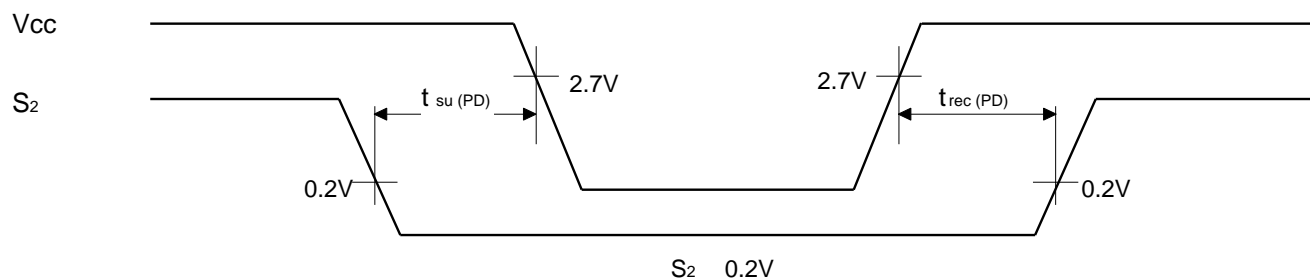
6: Don't apply inverted phase signal externally when DQ pin is output mode.

M5M5V208AKV/KR**PRELIMINARY**Notice: This is not a final specification.
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Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
$V_{CC(PD)}$	Power down supply voltage		2			V	
$V_{I(S1)}$	Chip select input $\overline{S1}$		2.0			V	
$V_{I(S2)}$	Chip select input S_2				0.2	V	
$I_{CC(PD)}$	Power down supply current	$V_{CC}=3.0V$ 1) $S_2 = 0.2V$, other inputs=0 ~ V_{CC} or 2) $\overline{S1} = V_{CC}-0.2V$, $S_2 = V_{CC}-0.2V$ other inputs=0 ~ V_{CC}	-L		50	μA	
			-H	$\sim +25^\circ C$	0.3		1
			-HW	$\sim +40^\circ C$			3
			-HI	$\sim +70^\circ C$			8
			-HW / I	$\sim +85^\circ C$			24

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down set up time		0			ns
$t_{rec(PD)}$	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS **$\overline{S1}$ control mode** **S_2 control mode**

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Revision History

<u>Revision No.</u>	<u>History</u>	<u>Date</u>	
A0.1E	The first edition	09.Nov.'98	Preliminary
A0.2E	The second edition	29.Nov.'99	Preliminary