

# Clock generator IC

## BU2288FV

The BU2288FV is an IC that generates plural clocks required for DVD system from a 2-channel PLL external crystal oscillator. The six kinds of signals for video and audio system are generated with low jitter.

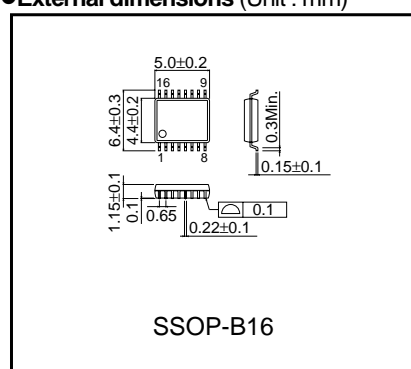
### ●Application

All DVD sets

### ●Features

- 1) All clock signals needed for DVD can be generated by a single chip.
- 2) All output low jitter (No load 30psec)
- 3) No need for additional components.  
(BU2288FV has a PLL loop filter inside.)
- 4) 3.3V single power supply
- 5) Small SSOP-B16 package.

### ●External dimensions (Unit : mm)



### ●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V <sub>DD</sub>	-0.5 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5	V
Storage temperature range	T <sub>stg</sub>	-30 to +125	°C
Power dissipation	P <sub>d</sub>	450	mW

\* An operation is not guaranteed.

\* In case it is used at Ta=25°C or more, 4.5mW is reduced at every1°C.

\* Radiation resistance design is not used.

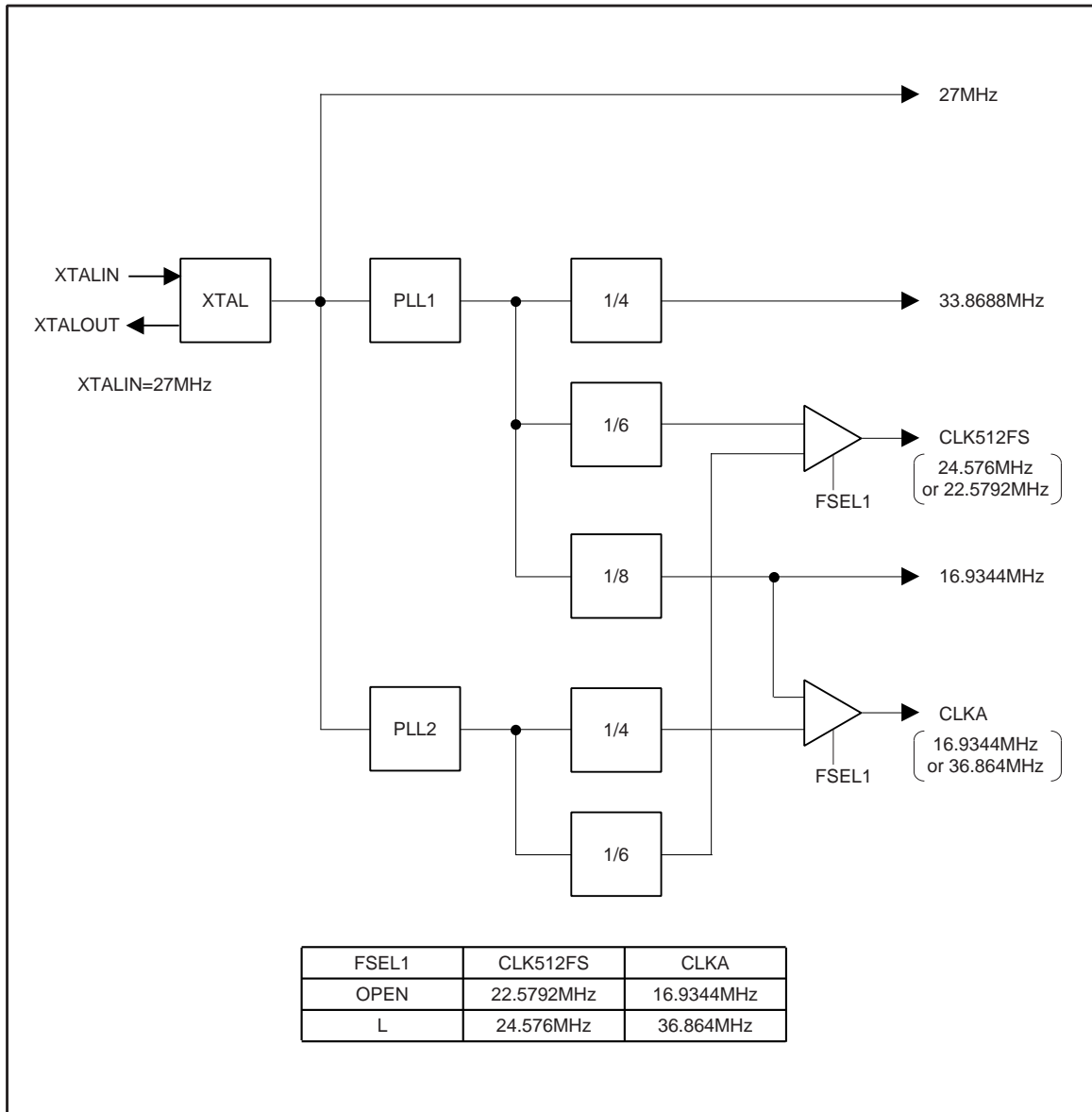
\* Power dissipation is measured when BU2288FV is placed on the board.

### ●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>	3.0	-	3.6	V
Input "H" voltage range	V <sub>IH</sub>	0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V
Input "L" voltage range	V <sub>IL</sub>	0	-	0.2V <sub>DD</sub>	V
Operation temperature range	T <sub>opr</sub>	-5	-	70	°C
Output maximum load	CL	-	-	15	pF

Multimedia ICs

●Block diagram



## Multimedia ICs

## ●Pin descriptions

Pin No.	Pin name	Functions
1	VDD2	Digital VDD for 27MHz clock output
2	VSS2	Digital GND for 27MHz clock output
3	CLK27M	27MHz clock output
4	TEST	Output for test
5	AVDD	Analog VDD
6	AVSS	Analog GND
7	XTALOUT	Standard crystal output
8	XTALIN	Standard crystal input
9	CLKA	Clock output (FSEL1=Open : 16.9344MHz, FSEL1=L : 36.864MHz)
10	CLK512FS	Clock output (FSEL1=Open : 22.5792MHz, FSEL1=L : 24.576MHz)
11	DVSS	Digital GND
12	DVDD	Digital VDD
13	CLK16M	16.9344MHz clock output
14	FSEL1	Output select : with pull-up Open : 16.9344MHz (Pin9), 22.5792MHz (Pin10) L : 36.864MHz (Pin9), 24.576Mhz (Pin10)
15	CLK33M	33.8688MHz clock output
16	OE	Output enable (open : enable, L : disable) : with pull-up

Multimedia ICs

●Input output circuits

Pin No.	Equivalent circuit
Input (schmitt trigger) Pin 14 with pull-up resistance	
Input Pin 16 with pull-up resistance	
Output Pin 3, 9, 10, 13, 15	
Output Pin 4	
Crystal Pin 7, 8	

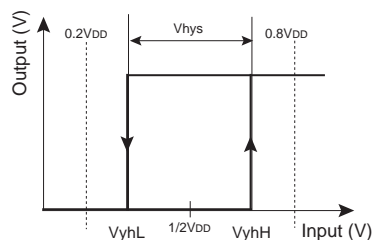
## Multimedia ICs

**●Electrical characteristics** (Unless specified otherwise Ta=25°C, VDD=3.3V, crystal frequency=27MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output "H" voltage	V <sub>OH</sub>	2.4	–	–	V	I <sub>OH</sub> =–4.0mA
Output "L" voltage	V <sub>OL</sub>	–	–	0.4	V	I <sub>OL</sub> =4.0mA
FSEL Input V <sub>thL</sub> *3	V <sub>thL</sub>	0.2V <sub>DD</sub>	–	–	V	*1
FSEL Input V <sub>thH</sub> *3	V <sub>thH</sub>	–	–	0.8V <sub>DD</sub>	V	*1
Hysteresis width *3	V <sub>hys</sub>	0.2	–	–	V	V <sub>hys</sub> =V <sub>thH</sub> –V <sub>thL</sub>
Power supply current	I <sub>DD</sub>	–	27	40.5	mA	no load
CLK512FS	CLK512-A	–	22.5792	–	MHz	FSEL1=OPEN, XTAL *3136/625/6
	CLK512-B	–	24.576	–	MHz	FSEL1=L, XTAL *2048/375/6
CLK33M	CLK33M	–	33.8688	–	MHz	XTAL *3136/625/4
CLK16M	CLK16M	–	16.9344	–	MHz	XTAL *3136/625/8
CLK27M	CLK27M	–	27	–	MHz	XTAL output
CLK A	CLKA-A	–	16.9344	–	MHz	FSEL1=OPEN, XTAL *3136/625/8
	CLKA-B	–	36.864	–	MHz	FSEL1=L, XTAL *2048/375/4
Duty	Duty	45	50	55	%	1/2 V <sub>DD</sub> test
Jitter 1σ	J <sub>sSD</sub>	–	70	–	psec	Jitter 1sigma
Jitter MIN-MAX	J <sub>sABS</sub>	–	420	–	psec	MIN-MAX level
Rise time	t <sub>r</sub>	–	2.5	–	nsec	Time between 0.2V <sub>DD</sub> –0.8V <sub>DD</sub>
Fall time	t <sub>f</sub>	–	2.5	–	nsec	Time between 0.8V <sub>DD</sub> –0.2V <sub>DD</sub>
Output Lock time	t <sub>lock</sub>	–	–	1	msec	*2

Note : JITTER is mean value when using Time Interval Analyzer with 10,000 sampling

\*1) graph

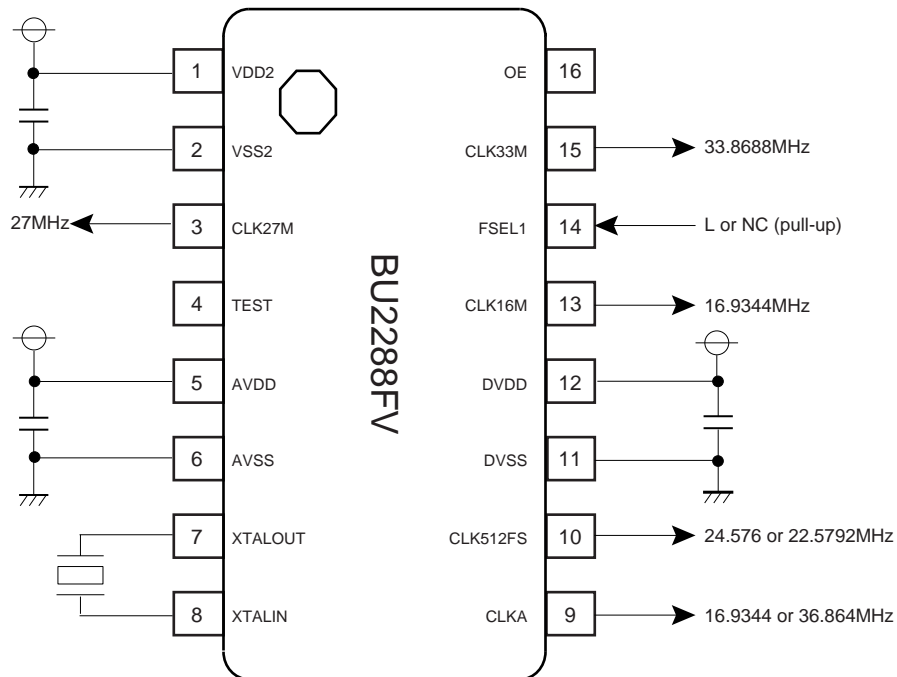


\*2) Time between voltage supply leads to 3.0V and output clock gats stable.

Start up time of power supply sources satisfy this rated value at every time, case

## Multimedia ICs

## ●Application example



Note : The BU2288FV is basically placed on the board

Decoupling capacitance (0.1 $\mu$ F) need to be placed between Pin5 (AVDD) and Pin6 (AVSS).

Also Decoupling capacitance (0.1 $\mu$ F) need to be placed between Pin1 (VDD2) and Pin2 (VSS2), Pin11 (DVSS) and Pin12 (DVDD).

To obtain accurate frequency, capacitance ( pF) need to be placed between Pin8 (XTALIN) and Pin6 (AVSS), Pin7 (XTALOUT) and Pin6 (AVSS).

Tantalum capacitance (10 ~100 $\mu$ F), ferrite beads may need to be placed to prevent power supply drop in certain boards case.

To reduce high frequency noise, selected bypass capacitors ( $\leq 1\Omega$  at problem high frequency) maybe used for power pin as close to BU2288FV as possible.

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