

## Low Supply Current, 50mW Stereo Cap-Free Headphone Driver

### Features

- **Operating Voltage: 2.3V~5.5V**
- **Supply Current**
  - $I_{DD}=1\text{mA}$  at  $V_{DD}=3.6\text{V}$
- **Low Shutdown Current**
  - $I_{DD}=5\text{mA}$  at  $V_{DD}=3.6\text{V}$
- **Ground Reference Output**
  - **No Output Capacitor Required (for DC Blocking)**
  - **Save the PCB Space**
  - **Reduce the BOM Costs**
  - **Improve the Low Frequency Response**
- **Output Power 50mW/Ch into 16Ω at  $V_{DD}=3.6\text{V}$**
- **High PSRR: 80dB at 217Hz**
- **Fast Start-Up Time: 4ms**
- **Integrate the De-pop Circuitry**
- **Thermal Protection**
- **Surface-Mount Packaging**
  - WLCSP1.6x1.6-12**
  - TDFN3x3-12**
- **Lead Free and Green Devices Available (RoHS Compliant)**

### Applications

- **Handsets**
- **PDA's**
- **Portable Multimedia Devices**
- **Notebooks**

### General Description

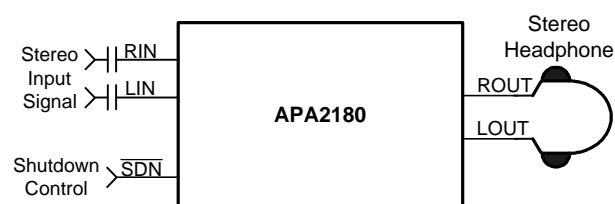
The APA2180 is a stereo, fixed gain, single supply, and cap-free headphone driver, which is available in a WLCSP1.6x1.6-12 and TDFN3x3-12 packages.

The APA2180 is ground-reference output and don't need the output capacitors for DC blocking. The advantages of eliminating the output capacitor are saving the cost, eliminating component height, and improving the low frequency response.

The internal fixed gain setting (-1.5V/V) can minimize the external component counts and save the PCB space. High PSRR provides increased immunity to noise and RF rectification.

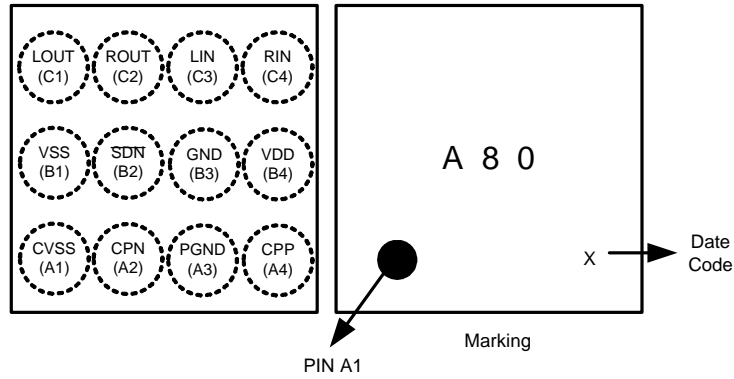
The APA2180 is capable of driving 50mW at 3.6V into 16Ω load and provides thermal protection.

### Simplified Application Circuit

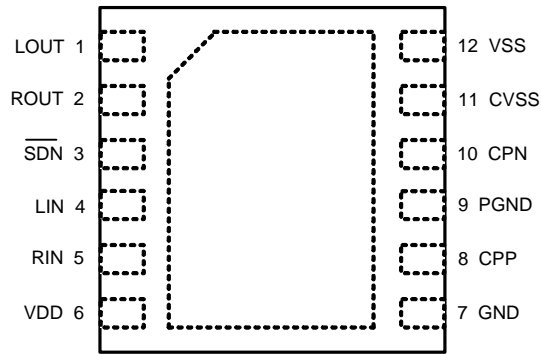


ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration

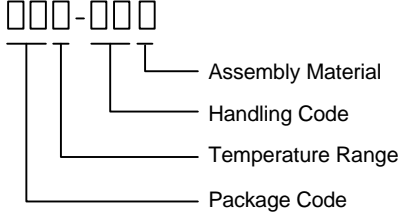


**WLCSP1.6x1.6-12  
(Top View)**



**TDFN3x3-12  
(Top View)**

## Ordering and Marking Information

<p>APA2180    □□□-□□□</p>  <p>Assembly Material Handling Code Temperature Range Package Code</p>	<p>Package Code HA : WLCSP1.6x1.6-12 QB : TDFN3x3-12 Temperature Range I : - 40 to 85 °C Handling Code TR : Tape &amp; Reel Assembly Material G : Halogen and Lead Free Device</p>			
<p>APA2180 HA:    <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>A80</td></tr><tr><td>• X</td></tr></table></p>	A80	• X	<p>X - Date Code</p>	
A80				
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<p>APA2180 QB:    <table border="1" style="display: inline-table; vertical-align: middle;"><tr><td>APA</td></tr><tr><td>2180</td></tr><tr><td>XXXXX</td></tr></table></p>	APA	2180	XXXXX	<p>X - Date Code</p>
APA				
2180				
XXXXX				

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
$V_{PGND\_GND}$	PGND to GND Voltage	-0.3 to 0.3	V
$V_{DD}$	Supply Voltage (VDD to GND and PGND)	-0.3 to 5.5	
$V_{SDN}$	Input Voltage ( $\overline{SDN}$ to GND)	GND-0.3 to $V_{DD}+0.3$	
$V_{SS}$	VSS to GND and PGND Voltage	-5.5 to 0.3	
$V_{OUT}$	ROUT and LOU to GND Voltage	$V_{SS}-0.3$ to $V_{DD}+0.3$	
$V_{CPP}$	CPP to PGND Voltage	PGND-0.3 to $V_{DD}+0.3$	
$V_{CPN}$	CPN to PGND Voltage	$PV_{SS}-0.3$ to PGND+0.3	
$T_J$	Maximum Junction Temperature	150	°C
$T_{STG}$	Storage Temperature Range	-65 to +150	
$T_{SDR}$	Maximum Soldering Temperature Range, 10 Seconds	260	
$P_D$	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
$\theta_{JA}$	Thermal Resistance - Junction to Ambient <sup>(Note 2)</sup> WLCSP1.6x1.6-12 TDFN3x3-12	160 50	$^{\circ}\text{C/W}$

Note 2: Please refer to "Thermal Pad Consideration". 2 layered 5 in2 printed circuit boards with 2oz trace and copper through several thermal vias. The thermal pad is soldered on the PCB.

## Recommended Operating Conditions

Symbol	Parameter	Range	Unit	
$V_{DD}$	Supply Voltage	2.3 ~ 5.5	V	
$V_{IH}$	High Level Threshold Voltage	SDN		1.0 ~ $V_{DD}$
$V_{IL}$	Low Level Threshold Voltage	SDN		0 ~ 0.35
$T_A$	Operating Ambient Temperature Range	-40 ~ 85	$^{\circ}\text{C}$	
$T_J$	Operating Ambient Temperature Range	-40 ~ 125		
$R_L$	Headphone Resistance	16 ~ 100k	$\Omega$	

## Electrical Characteristics

$V_{DD}=3.6\text{V}$ ,  $V_{GND}=V_{PGND}=0\text{V}$ ,  $V_{SDN}=V_{DD}$ ,  $C_{CPF}=C_{CPO}=1\mu\text{F}$ ,  $C_I=1\mu\text{F}$ ,  $T_A=25^{\circ}\text{C}$  (unless otherwise noted).

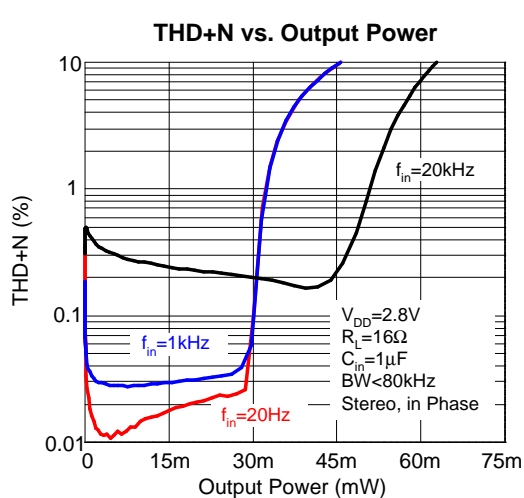
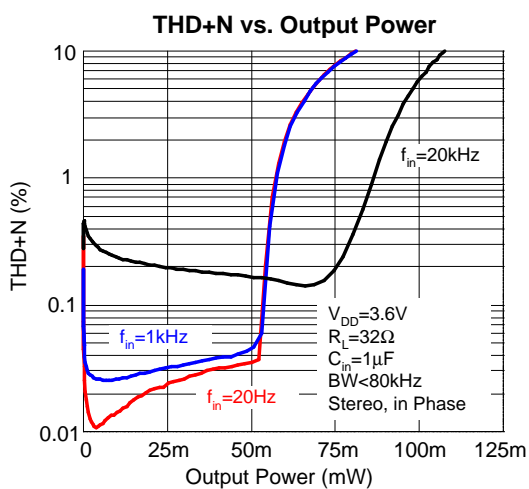
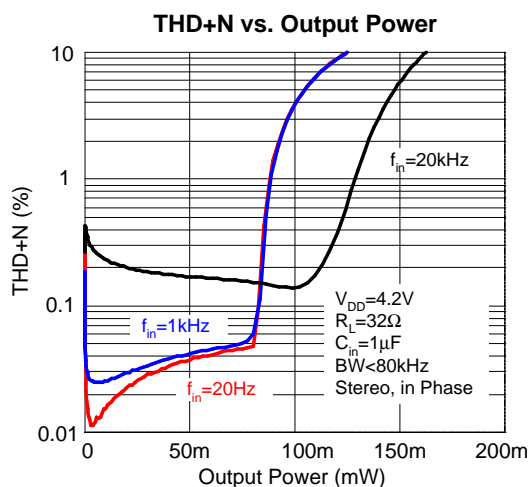
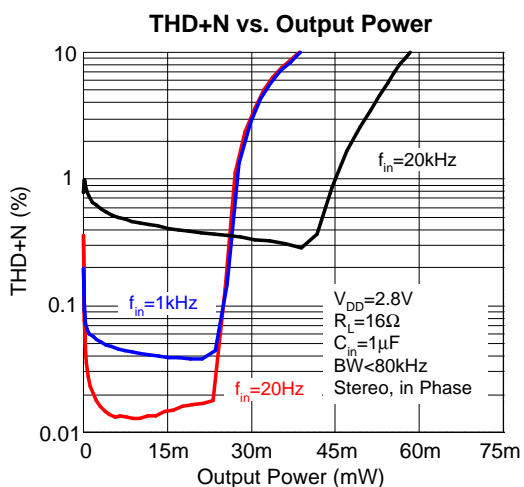
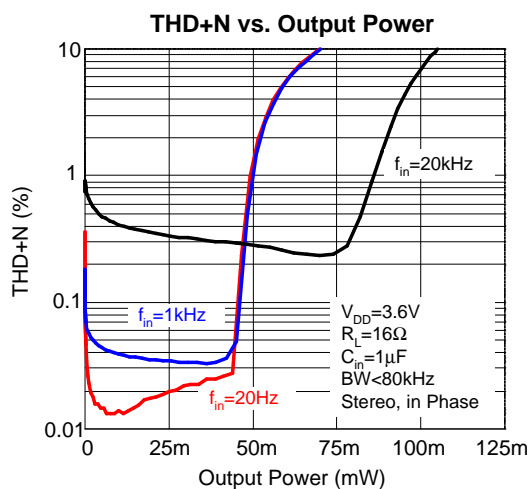
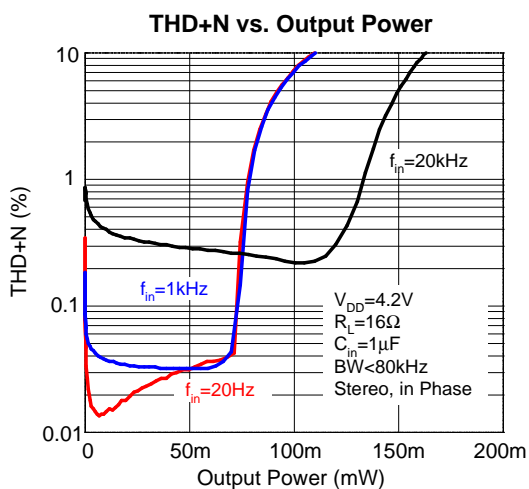
Symbol	Parameter	Test Conditions	APA2180			Unit
			Min.	Typ.	Max.	
$I_{DD}$	$V_{DD}$ Supply Current		-	1	2	mA
$I_{SD}$	$V_{DD}$ Shutdown Current	$V_{SDN}=0\text{V}$	-	5	10	$\mu\text{A}$
$I_I$	Input current	SDN	-	0.1	-	
<b>CHARGE PUMP</b>						
$f_{OSC}$	Switching Frequency		400	500	600	kHz
$R_{eq}$	Equivalent Resistance		-	15	18	$\Omega$
<b>DRIVERS</b>						
$A_V$	Internal Voltage Gain	No Load	-1.55	-1.5	-1.45	V/V
$A_V$	Gain Matching		-	1	2	%
$R_i$	Input Resistance		12	14	16	k $\Omega$
$R_f$	Feedback Resistance		17	21	25	
$V_{SR}$	Slew Rate		-	2.5	-	V/ $\mu\text{s}$
$V_{OS}$	Output Offset Voltage	$V_{DD}=2.3\text{V}$ to $5.5\text{V}$ , $R_L = 16\Omega$	-8	-	8	mV
$V_N$	Output Noise		-	27	-	$\mu\text{Vrms}$
PSRR	Power Supply Rejection Ratio	$V_{DD}=2.3\text{V}$ to $5.5\text{V}$ , $V_{r}=200\text{mVrms}$ $f_{in}= 217\text{Hz}$ $f_{in}= 1\text{kHz}$ $f_{in}= 20\text{kHz}$	-	-80 -80 -40	-60 -60 -35	dB
$C_L$	Maximum Capacitive Load		-	400	-	pF
$T_{start-up}$	Start-up Time		-	4	-	ms
$V_{ESD}$	ESD Protection	OUTR, OUTL	-	8	-	kV

**Electrical Characteristics (Cont.)**

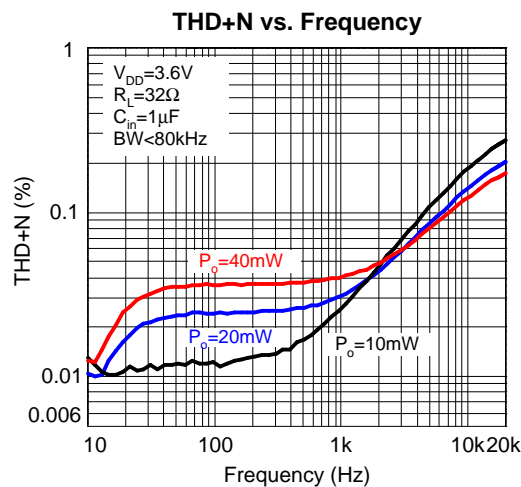
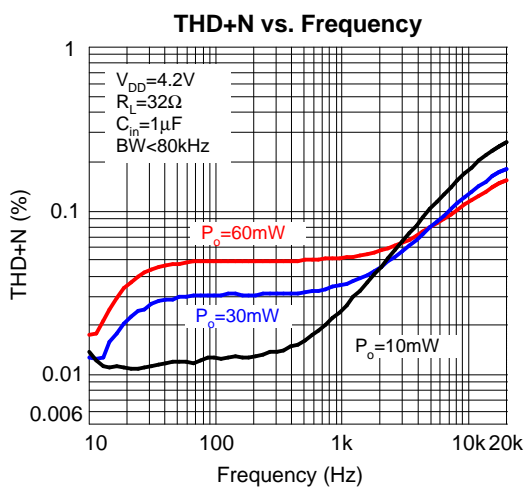
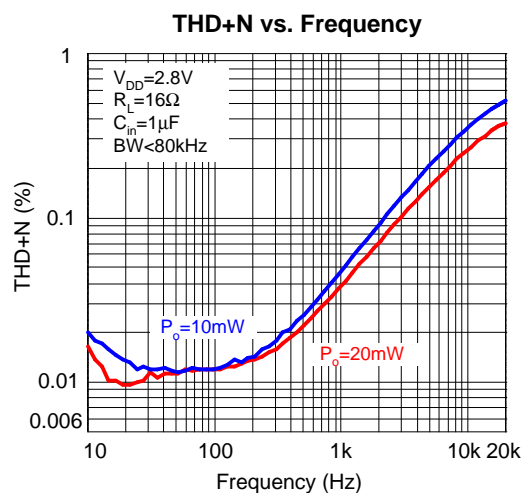
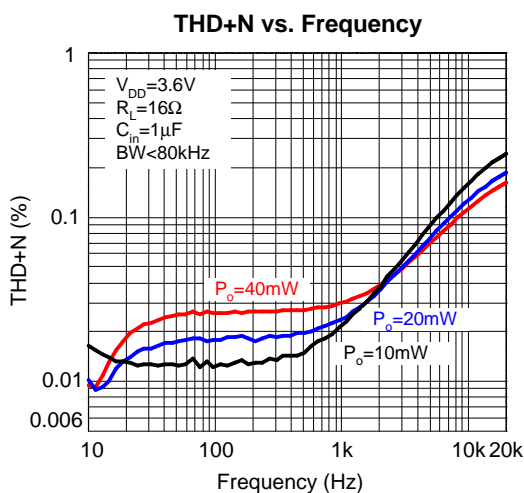
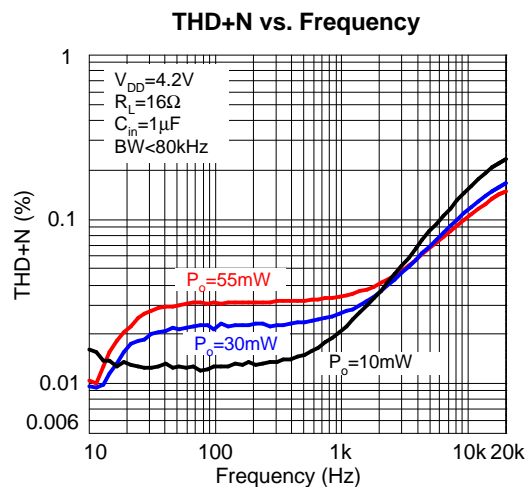
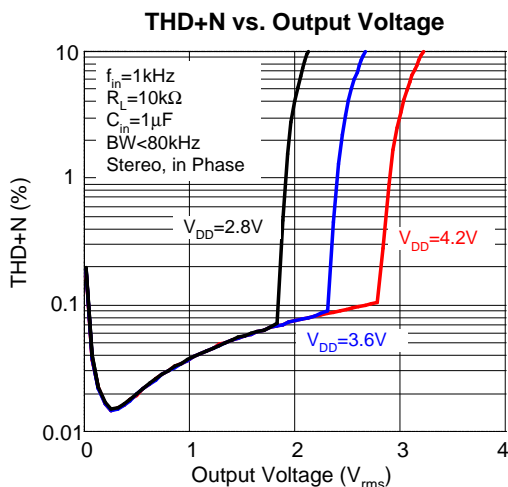
$V_{DD}=3.6V$ ,  $V_{GND}=V_{PGND}=0V$ ,  $V_{SDN}=V_{DD}$ ,  $C_{CPF}=C_{CPO}=1\mu F$ ,  $C_I=1\mu F$ ,  $T_A=25^\circ C$  (unless otherwise noted).

Symbol	Parameter	Test Conditions	APA2180			Unit
			Min.	Typ.	Max.	
<b>DRIVERS (CONT.)</b>						
P <sub>O</sub>	Output Power (Stereo, In Phase)	THD+N=1%, f <sub>in</sub> =1kHz R <sub>L</sub> =16Ω R <sub>L</sub> =32Ω	45	50 60	-	mW
		THD+N=10%, f <sub>in</sub> =1kHz R <sub>L</sub> =16Ω R <sub>L</sub> =32Ω	-	70 80	-	
THD+N	Total Harmonic Distortion Plus Noise	P <sub>O</sub> =20mW, R <sub>L</sub> =32Ω f <sub>in</sub> =20Hz f <sub>in</sub> =1kHz f <sub>in</sub> =20kHz	-	0.03 0.03 0.20	-	%
Crosstalk	Channel Separation	P <sub>O</sub> =20mW, R <sub>L</sub> =16Ω, f <sub>in</sub> =20Hz f <sub>in</sub> =1kHz f <sub>in</sub> =20kHz	75	85 85 70	-	dB
S/N	Signal to Noise Ratio	V <sub>DD</sub> =5V, P <sub>O</sub> =140mW, R <sub>L</sub> =32Ω, With A-weighting Filter	-	95	-	

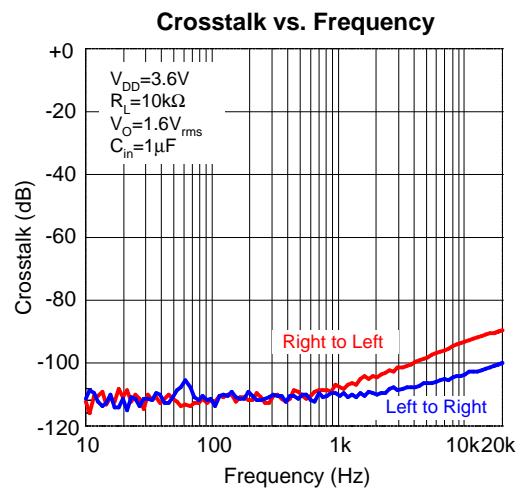
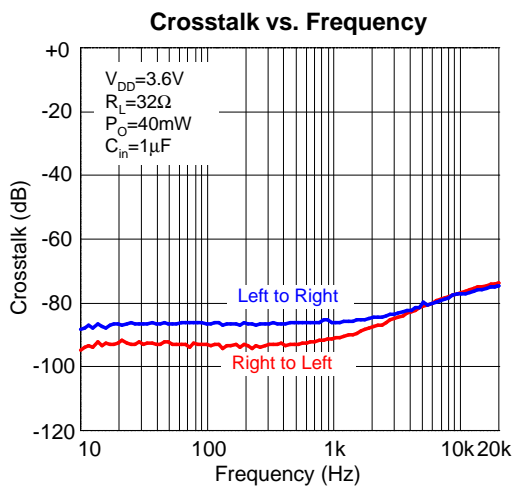
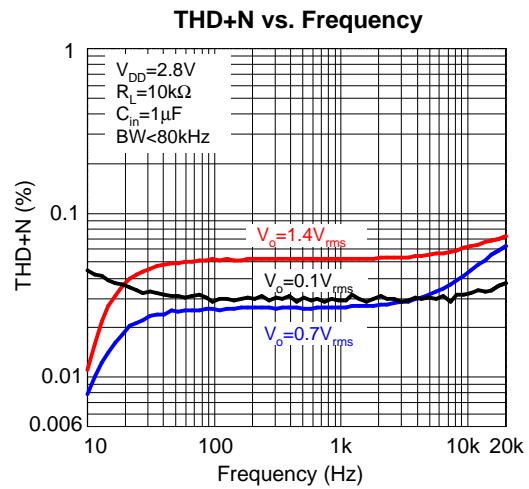
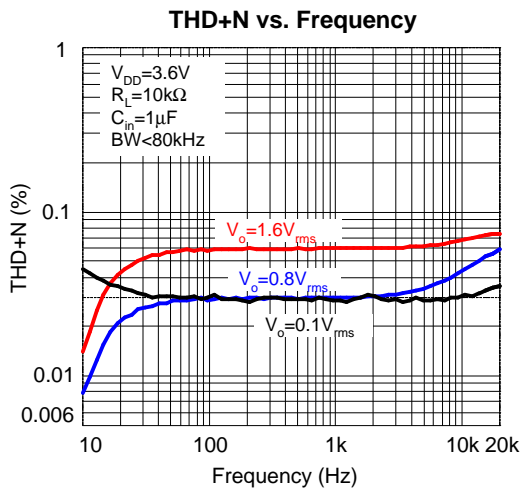
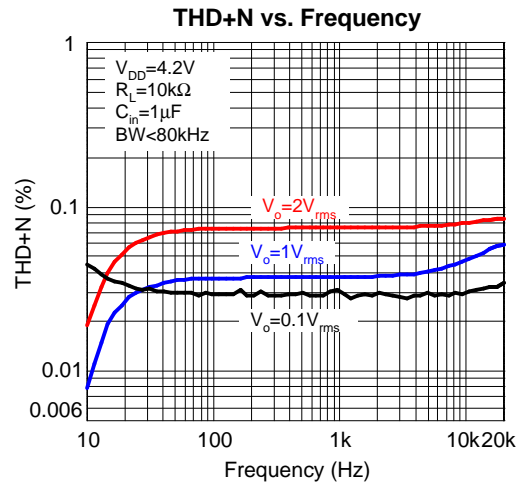
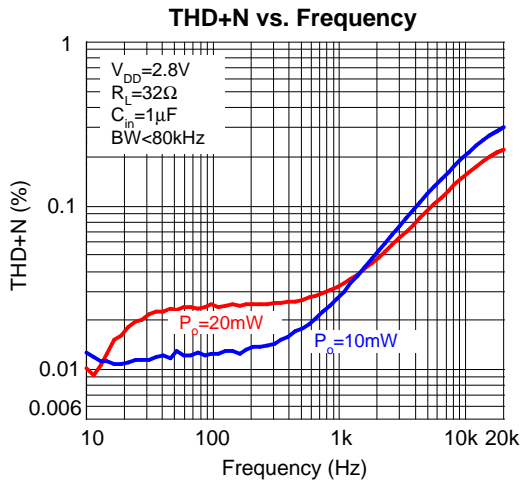
### Typical Operating Characteristics



Typical Operating Characteristics (Cont.)

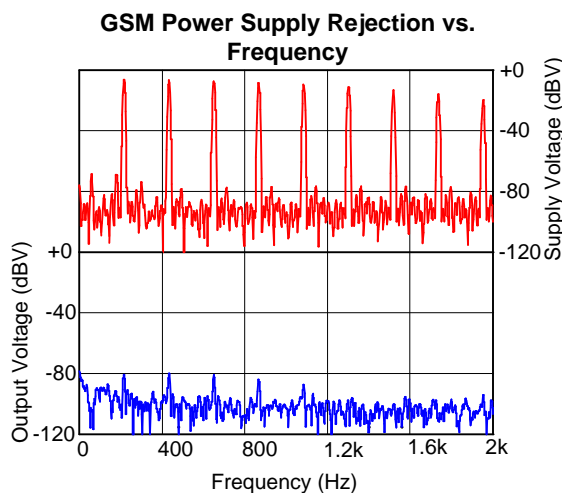
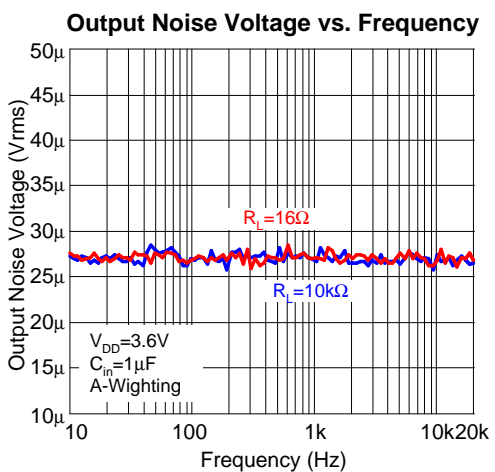
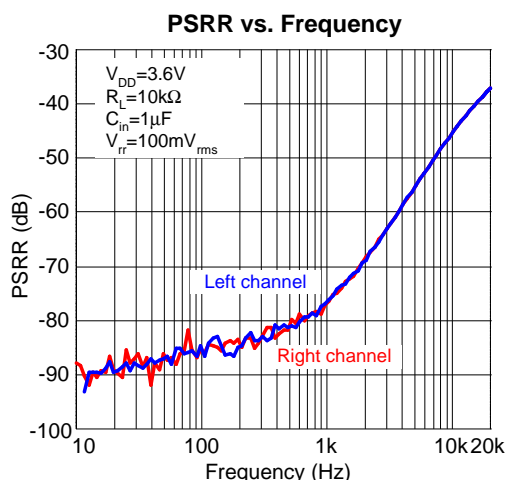
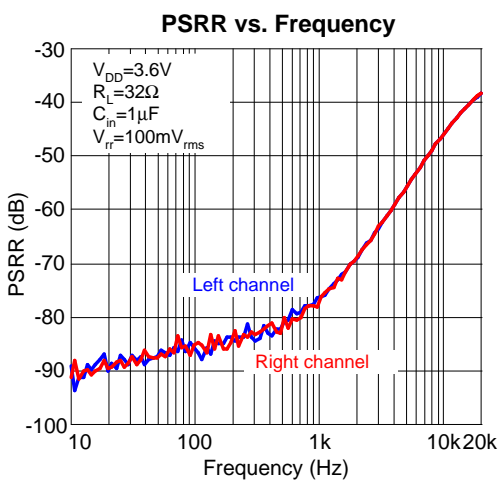
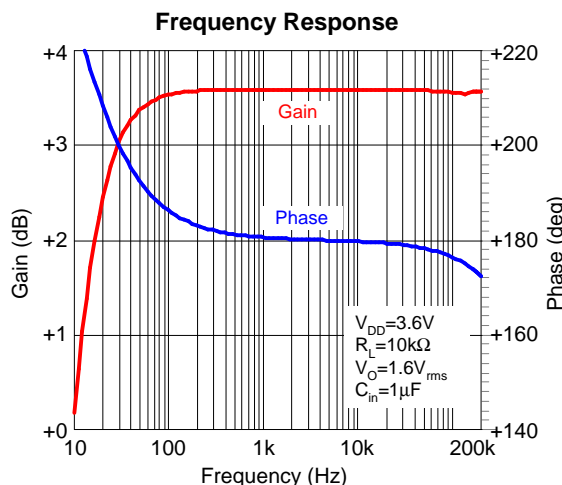
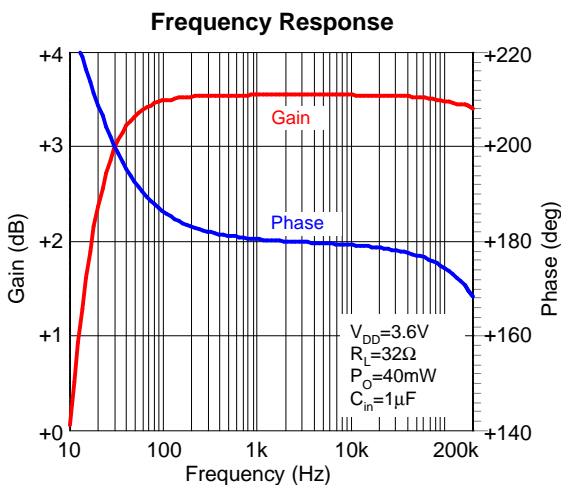


Typical Operating Characteristics (Cont.)



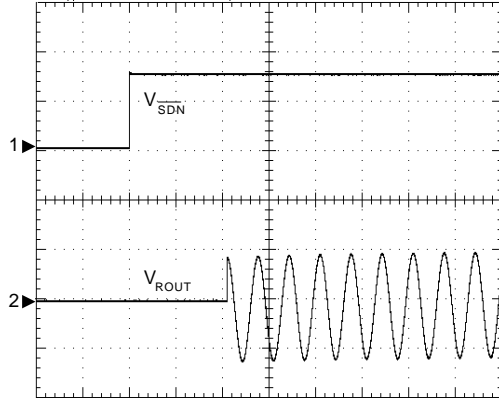


Typical Operating Characteristics (Cont.)



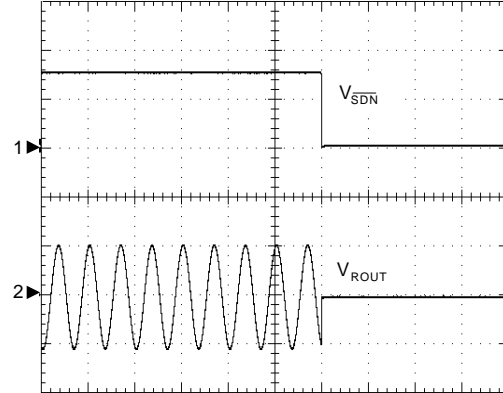
## Operating Waveforms

Shutdown Release



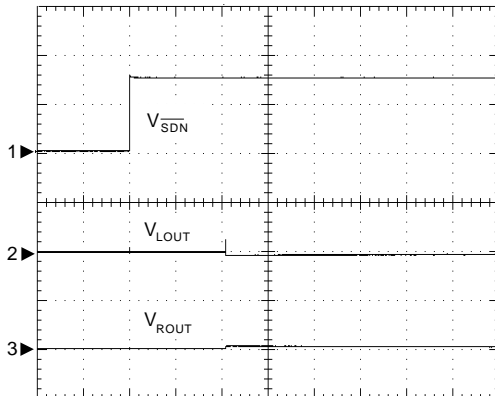
$V_{DD}=3.6V$ ,  $R_L=32\Omega$   
 CH1:  $V_{SDN}$ , 2V/Div, DC  
 CH2:  $V_{ROUT}$ , 1V/Div, DC  
 TIME:2ms/Div

Shutdown



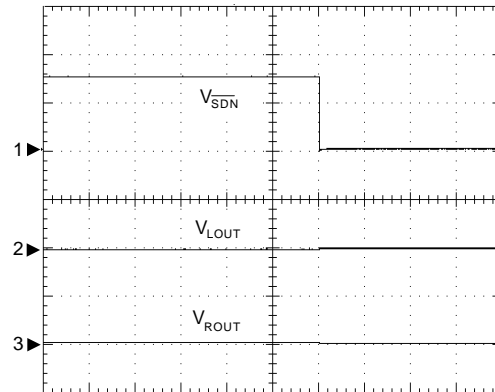
$V_{DD}=3.6V$ ,  $R_L=32\Omega$   
 CH1:  $V_{RSD}$ , 2V/Div, DC  
 CH2:  $V_{ROUT}$ , 1V/Div, DC  
 TIME:2ms/Div

Output Transient at Shutdown Release



$V_{DD}=3.6V$ ,  $R_L=32\Omega$   
 CH1:  $V_{SDN}$ , 2V/Div, DC  
 CH2:  $V_{LOUT}$ , 20mV/Div, DC  
 CH3:  $V_{ROUT}$ , 20mV/Div, DC  
 TIME:2ms/Div

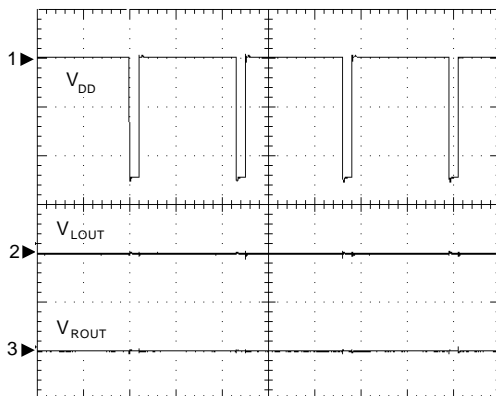
Output Transient at Shutdown



$V_{DD}=3.6V$ ,  $R_L=32\Omega$   
 CH1:  $V_{SDN}$ , 2V/Div, DC  
 CH2:  $V_{LOUT}$ , 20mV/Div, DC  
 CH3:  $V_{ROUT}$ , 20mV/Div, DC  
 TIME:2ms/Div

## Operating Waveforms (Cont.)

GSM Power Supply Rejection vs. Time



$V_{DD}=3.6V$ ,  $R_L=32\Omega$

CH1:  $V_{DD}$ , 200mV/Div, DC, Offset=3.6V

CH2:  $V_{LOUT}$ , 20mV/Div, DC

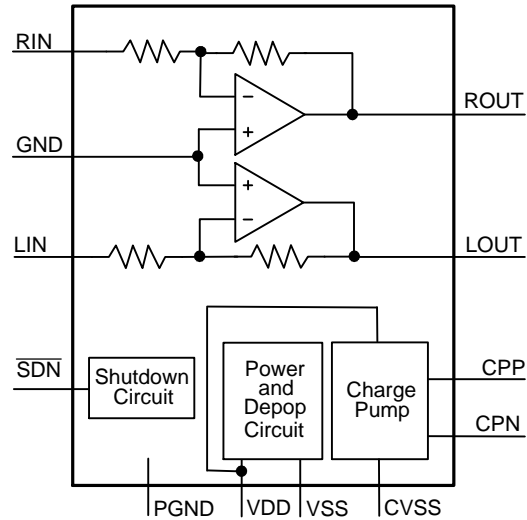
CH3:  $V_{ROUT}$ , 20mV/Div, DC

TIME:2ms/Div

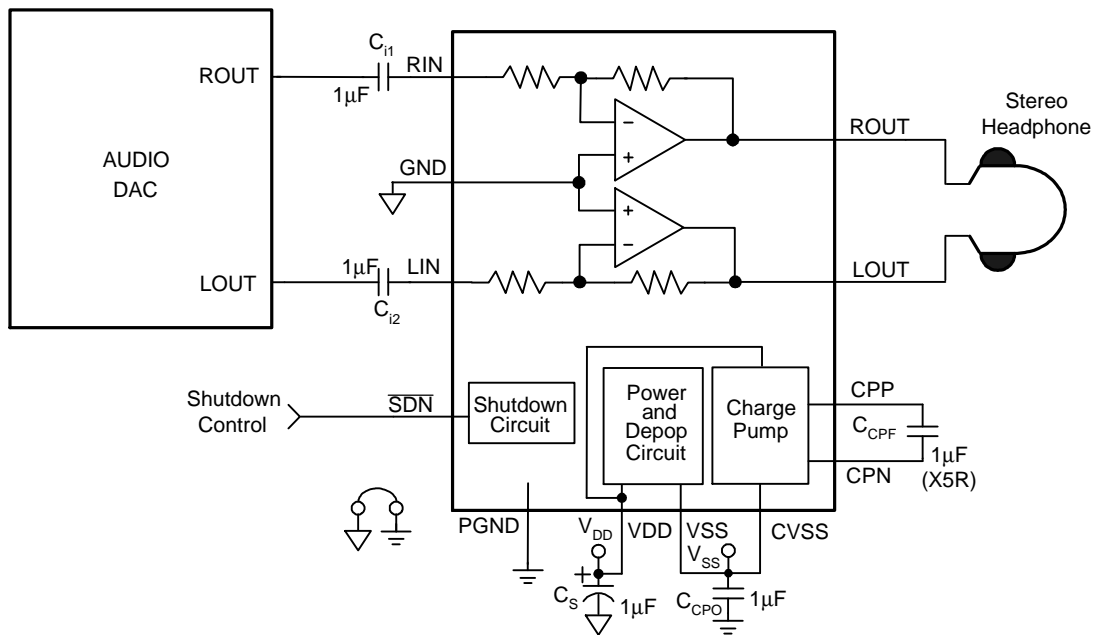
## Pin Description

PIN			I/O/P	FUNCTION
NO.		NAME		
WLCSP 1.6x1.6-12	TDFN3x3-12			
A1	11	CVSS	O	Charge pump output, connect to the "VSS".
A2	10	CPN	I/O	Charge pump flying capacitor negative connection.
A3	9	PGND	P	Charge pump's ground.
A4	8	CPP	I/O	Charge pump flying capacitor positive connection.
B1	12	VSS	P	Headphone driver negative power supply.
B2	3	$\overline{\text{SDN}}$	I	Shutdown mod control input signal, pull low for shutdown headphone driver.
B3	7	GND	P	Ground connection for circuitry.
B4	6	VDD	P	Supply voltage input pin.
C1	1	LOUT	O	Left channel output for headphone.
C2	2	ROUT	O	Right channel output for headphone.
C3	4	LIN	I	Left channel input terminal.
C4	5	RIN	I	Right channel input terminal.

Block Diagram



Typical Application Circuit



## Function Description

### Headphone Driver Operation

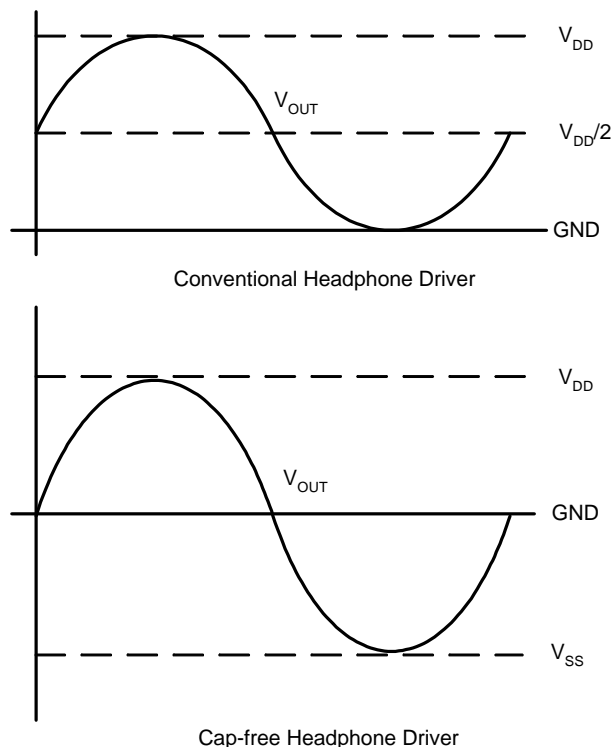


Figure 1. Cap-free Operation

The APA2180's headphone drivers use a charge pump to invert the positive power supply ( $V_{DD}$ ) to negative power supply ( $V_{SS}$ ), see figure1. The headphone drivers operate at this bipolar power supply ( $V_{DD}$  and  $V_{SS}$ ) and the outputs reference refers to the ground. This feature eliminates the output capacitor that is using in conventional single-ended headphone drive amplifier. Compare with the single power supply amplifier, the power supply range has almost doubled.

### Thermal Protection

The thermal protection circuit limits the junction temperature of the APA2180. When the junction temperature exceeds  $T_j = +150^{\circ}C$ , a thermal sensor turns off the driver, allowing the devices to cool. The thermal sensor allows the driver to start-up after the junction temperature down about  $125^{\circ}C$ . The thermal protection is designed with a  $25^{\circ}C$  hysteresis to lower the average  $T_j$  during continuous thermal overload conditions, increasing lifetime of the ICs.

### Shutdown Function

In order to reduce power consumption while not in use, the APA2180 contains shutdown controllers to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the  $\overline{SDN}$  pins for the APA2180. The trigger point between a logic high level is 1.0V and logic low level is 0.35V. It is recommended to switch between the ground and the supply voltage  $V_{DD}$  to provide maximum device performance. By switching the  $\overline{SDN}$  pins to a low level, the amplifier enters a low-consumption current circumstance, charge pump is disabled, and  $I_{DD}$  for the APA2180 is in shutdown mode. In normal operating, the APA2180's  $\overline{SDN}$  pins should be pulled to a high level to keep the IC out of the shutdown mode. The  $\overline{SDN}$  pins should be tied to a definite voltage to avoid unwanted circumstance changes.

## Application Information

### Charge Pump Flying Capacitor ( $C_{CPF}$ )

The flying capacitor ( $C_{CPF}$ ) affects the load transient of the charge pump. If the capacitor's value is too small, and then this increases charge pump's output resistance and degrades the performance of headphone amplifier.

Increasing the flying capacitor's value improves the load transient of charge pump. It is recommend to use the low ESR ceramic capacitors (X5R or X7R type is recommended) above  $1\mu\text{F}$ .

### Charge Pump Output Capacitor ( $C_{CPO}$ )

The charge pump needs an output capacitor( $C_{CPO}$ ) to filter the negative output current pulse flowing into CVSS pin as well as reduces the output voltage ripple(CVSS). The capacitor also sucks in surge current flowing from the  $V_{SS}$  pin, the negative power input pin for the amplifiers. The output ripple is determined by the capacitance, ESR, and current ripple of the output capacitor. Increasing the value of output capacitor and decreasing the ESR can reduce the voltage ripple. Using a low-ESR ceramic capacitor greater than  $1\mu\text{F}$  is recommended. For reducing the parasitic inductance and improving the noise decoupling, place the capacitor near the CVSS and PGND pins as close as possible.

### Input Capacitor ( $C_i$ )

In the typical application, an input capacitor ( $C_i$ ) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case,  $C_i$  and the input impedance  $R_i$  from a high-pass filter with the cutoff frequency are determined in the following equation:

$$f_{C(\text{highpass})} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of  $C_i$  must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where  $R_i$  is  $14\text{k}\Omega$  and the specification that calls for a flat bass response down to  $10\text{Hz}$ . The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When input resistance variation is considered, the  $C_i$  is  $1\mu\text{F}$ . Therefore, a value in the range of  $1\mu\text{F}$  to  $2.2\mu\text{F}$  would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network ( $R_i + R_i, C_i$ ) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the negative side of the capacitor should face the amplifiers' inputs in most applications because the DC level of the amplifiers' inputs are held at  $0\text{V}$ . Please note that it is important to confirm the capacitor polarity in the application.

### Power Supply Decoupling ( $C_s$ )

The APA2180 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitor that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically  $0.1\mu\text{F}$ , is placed as close as possible to the device VDD lead for the best performance. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of  $10\mu\text{F}$  or greater placed near the audio power amplifier is recommended.

### Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package in normal operating condition. The first consideration to calculate maximum ambient temperatures is the numbers from the Power Dissipation vs. Output Power graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given  $\theta_{JA}$ , the maximum allowable junction temperature ( $T_{J\text{max}}$ ), the total internal dissipation ( $P_D$ ), and the maximum ambient temperature can be calcu-

## Application Information (Cont.)

### Thermal Consideration (Cont.)

lated with the following equation. The maximum recommended junction temperature for the APA2180 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs. Output Power graphs. The APA2180 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

### Layout Consideration

1. All components should be placed close to the APA2180. For example, the input capacitor ( $C_{iR}$ ,  $C_{iL}$ ) should be close to APA2180 input pins to avoid causing noise coupling to APA2180 high impedance inputs; the decoupling capacitor ( $C_D$ ) should be placed by the APA2180 power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should be greater than 50mil.
5. The input trace and output trace should be away from  $C_{CPF}$  and  $C_{CPB}$  possible.

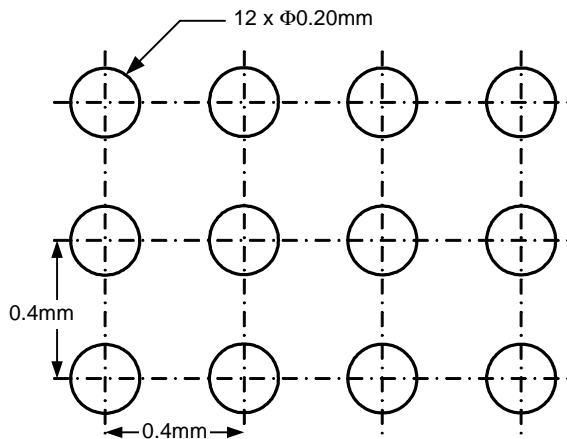


Figure 2. WLCSP2x2-16 land pattern recommendation

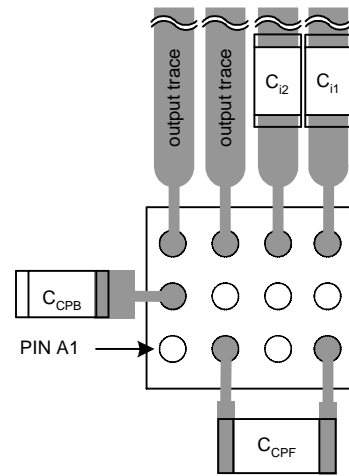


Figure 3. WLCSP2x2-16 Layout Suggestion

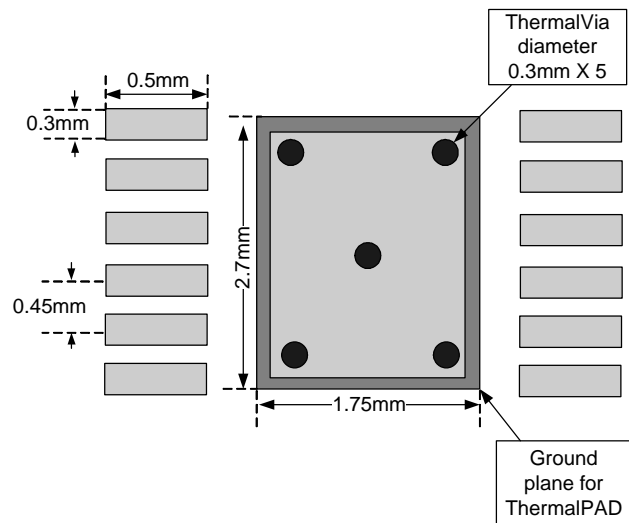
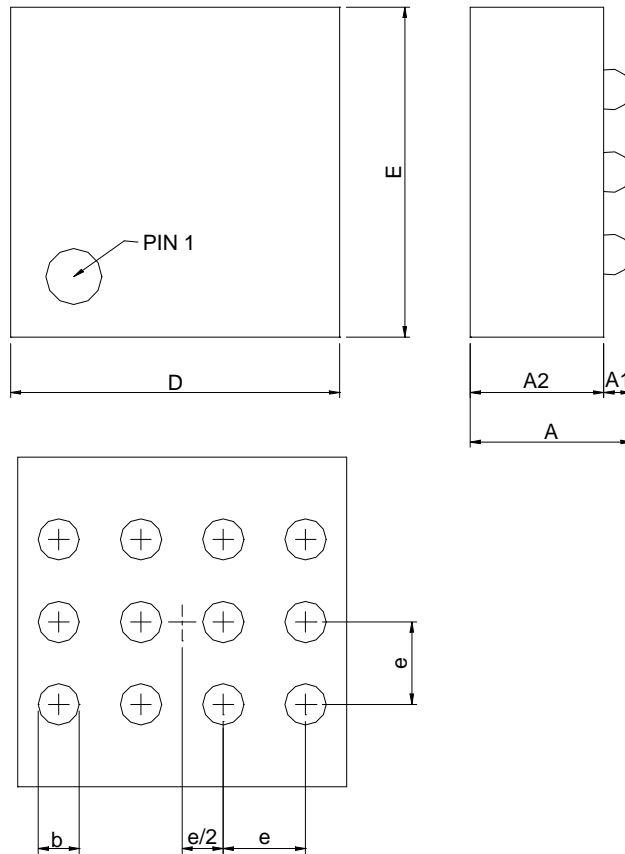


Figure 4: TDFN3x3-12 Layout Recommendation

Package Information

WLCSP1.6x1.6-12

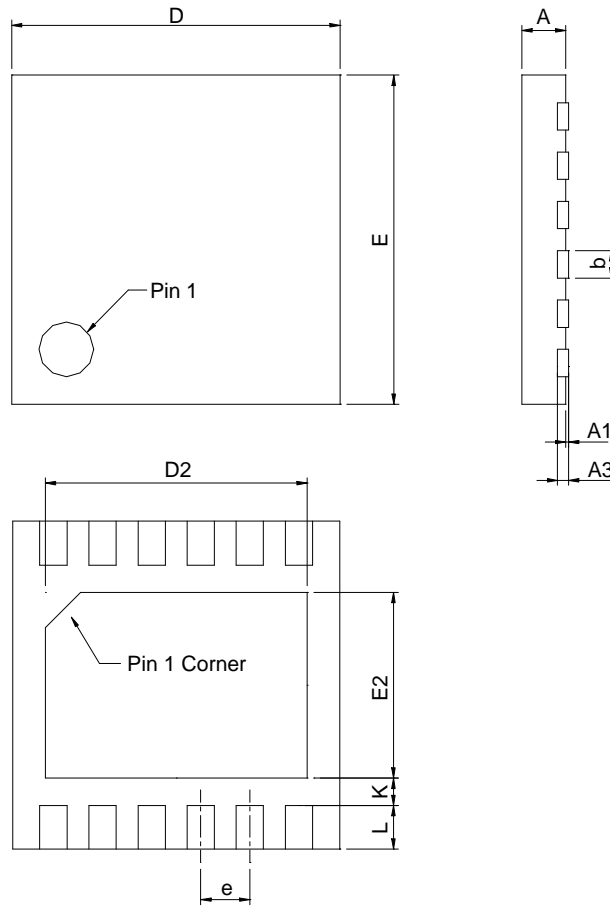


SYMBOL	WLCSP1.6x1.6-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.45	0.55	0.017	0.022
A1	0.10	0.20	0.004	0.008
A2	0.55	0.75	0.022	0.030
b	0.15	0.25	0.006	0.010
D	1.50	1.60	0.059	0.063
E	1.50	1.60	0.059	0.063
e	0.4 BSC		0.016 BSC	



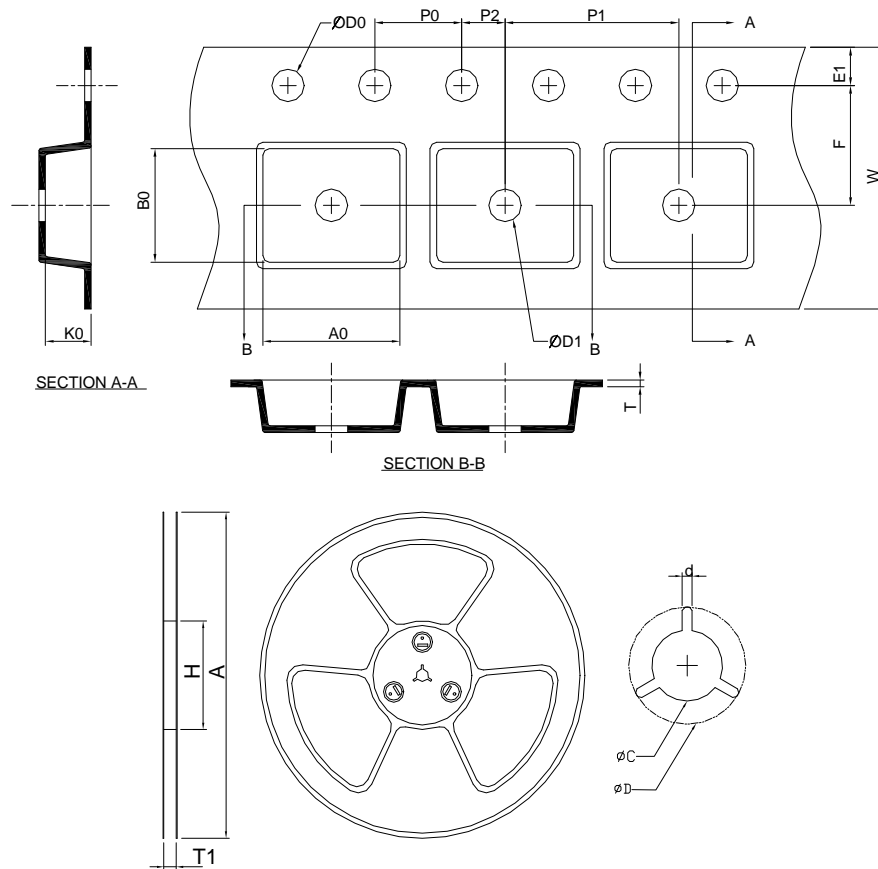
Package Information

TDFN3x3-12



SYMBOL	TDFN3x3-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.45 BSC		0.018 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

### Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP1.6x1.6-12	178.0 ±0.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0 ±0.30	1.75 ±0.10	3.5 ±0.05
	<b>P0</b>	<b>P1</b>	<b>P2</b>	<b>D0</b>	<b>D1</b>	<b>T</b>	<b>A0</b>	<b>B0</b>	<b>K0</b>
	4.0 ±0.10	4.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.75 ±0.15	1.75 ±0.15	0.75 ±0.10
Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-12	330 ±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	<b>P0</b>	<b>P1</b>	<b>P2</b>	<b>D0</b>	<b>D1</b>	<b>T</b>	<b>A0</b>	<b>B0</b>	<b>K0</b>
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30 ±0.20	3.30 ±0.20	1.30 ±0.20

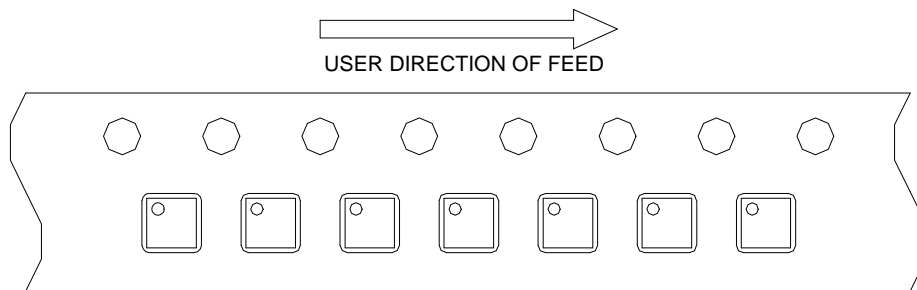
(mm)

**Devices Per Unit**

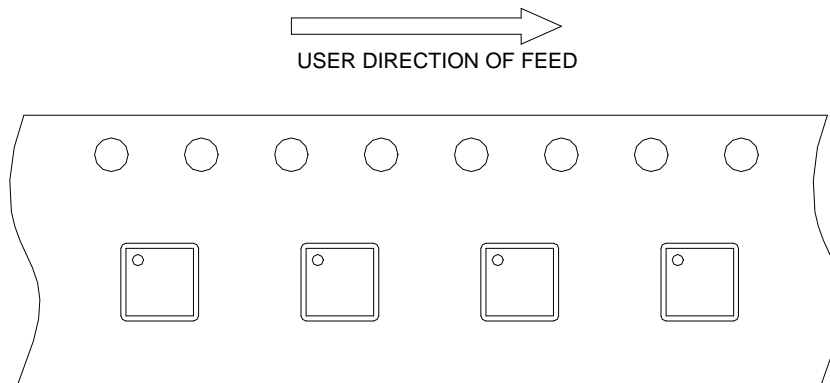
Package Type	Unit	Quantity
WLCSP1.6x1.6-12	Tape & Reel	3000
TDFN3x3-12	Tape & Reel	3000

**Taping Direction Information**

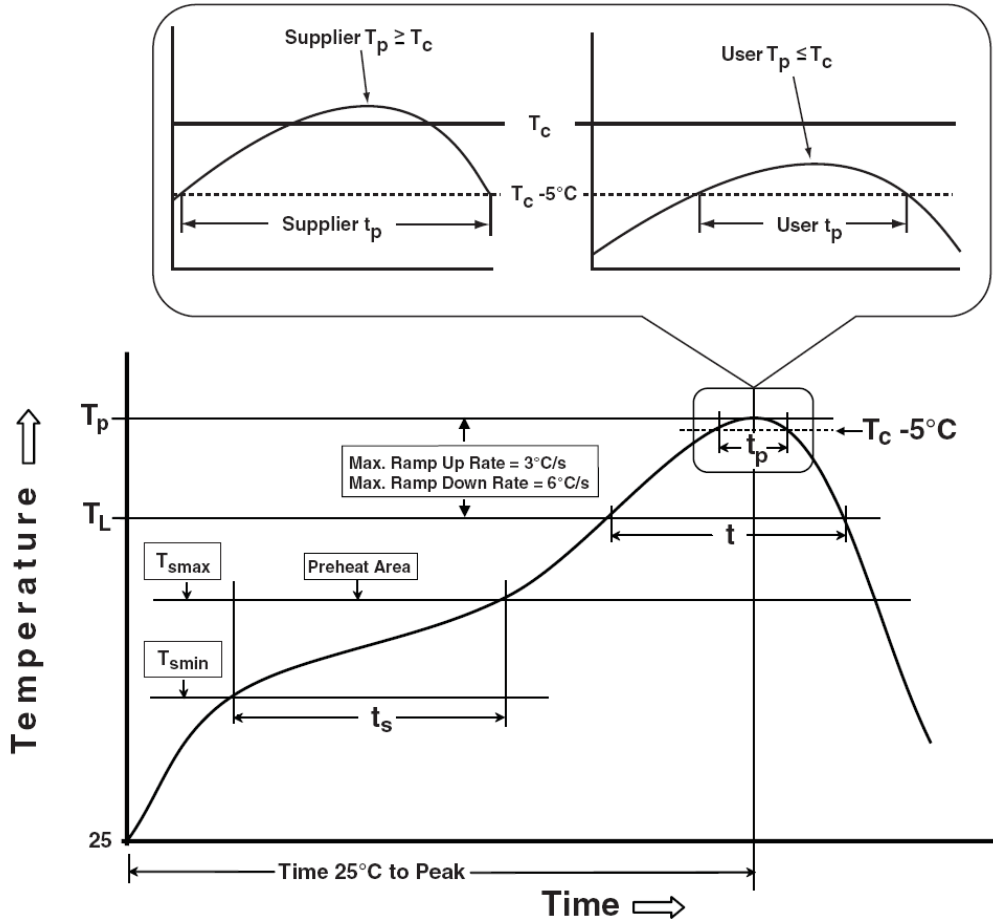
WLCSP1.6x1.6-12



TDFN3x3-12



Classification Profile



### Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b> Temperature min ( $T_{smin}$ ) Temperature max ( $T_{smax}$ ) Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3°C/second max.
Liquidous temperature ( $T_L$ ) Time at liquidous ( $t_L$ )	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

### Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^{\circ}\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> 100mA

## Customer Service

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