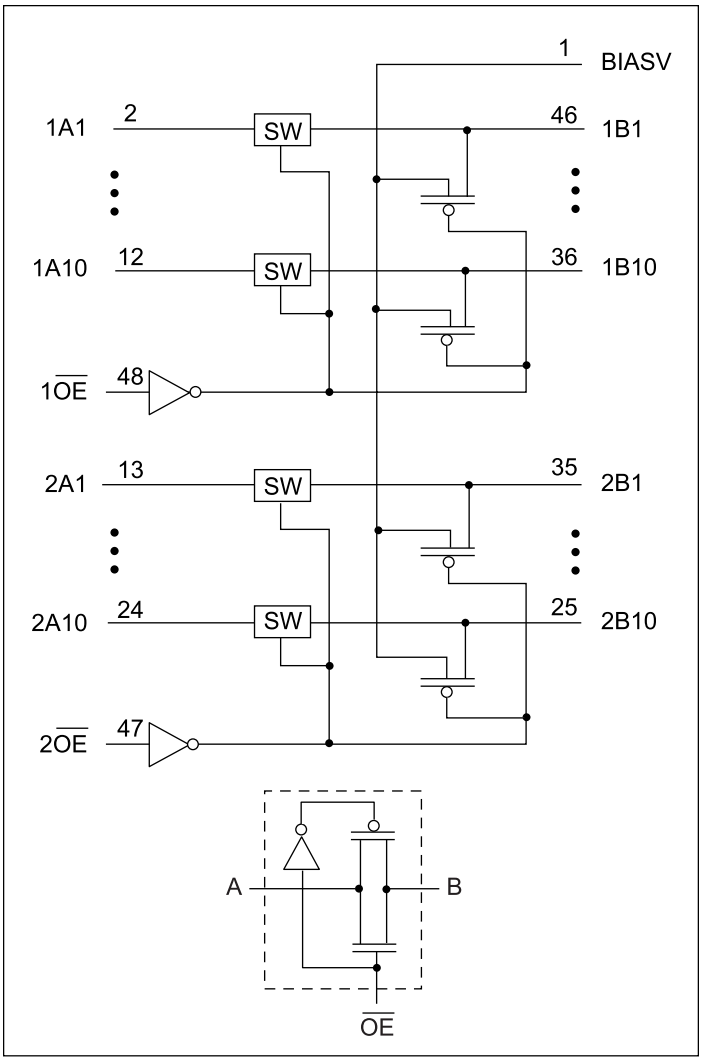
# PI3B16215

## 3.3V, Hot Insertion, 20-Bit FET BusSwitch w/Precharged Outputs

### Product Features

- Near Zero Propagation Delay
- 5Ω Switches Connect Between Two Ports
- Fast Switching Speed: 4.5ns max.
- Permits Hot Insertion
- Isolation during Power-Off conditions
- B-Port Outputs are precharged by Bias Voltage to minimize signal distortion during live insertion
- Package options include:
  – 48-pin 150-mil wide plastic BQSOP (B)
  – 48-pin 240-mil wide plastic TSSOP (A)
  – 48-pin 300-mil wide plastic SSOP (V)

### Logic Block Diagram




### Product Description

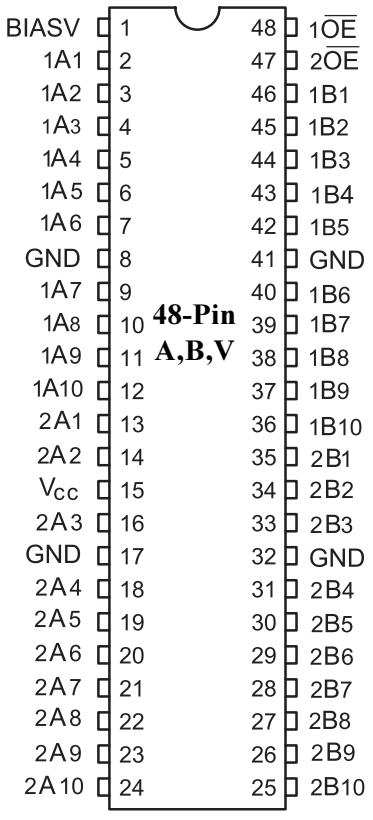
Pericom Semiconductor's PI3B series of logic circuits are produced using the company's advanced 0.35 micron CMOS Technology.

The PI3B16215 provides 20-bits of high-speed bus switching. Low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B-port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The device is organized as dual 10-bit bus switches with individual output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is LOW, the corresponding 10-bit bus switch is on and port A is connected to port B. When $\overline{OE}$ is HIGH, the switch is open, a high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-kΩ resistor.

To ensure the high-impedance state on power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver connected to $\overline{OE}$.

### Product Pin Configuration



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---|
| Storage Temperature Range, $T_{STG}$ | –65ºC to +150ºC |
| Supply Voltage Range, $V_{CC}$ | –0.5V to +4.6V |
| Bias Voltage Range, BIASV | –0.5V to +4.6V |
| Input Voltage Range | –0.5V to +4.6V |
| DC Output Current | 120mA |
| Power Dissipation | 0.5W |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics (Over the Operating Range, $T_A$ = –40°C to +85°C, $V_{CC}$ = 3.0V to 3.6V)

| Parameter | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| BIASV | Bias Voltage | | | 0 | | $V_{CC}$ | V |
| $V_{IH}$ | High-Level Control Input Voltage | $V_{CC}$ = 2.7V to 3.6V | | 2 | | | |
| $V_{IL}$ | Low-Level Control Input Voltage | $V_{CC}$ = 2.7V to 3.6V | | –0.5 | | 0.8 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 3.0V | $I_I$ = –18mA | | –0.7 | –1.2 | |
| $I_I$ | Input Current | $V_{CC}$ = 3.6V | $V_I$ = $V_{CC}$ or GND | | | ±5 | µA |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = 0 | $V_I$ = $V_O$ = 0 to 3.6V | | | 10 | |
| $I_O$ | Output Current | $V_{CC}$ = 3.0V | BIASV = 2.4V, $V_O$ = 0 | 0.15 | | | mA |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | | 10 | µA |
| $\Delta I_{CC}$(1) | Supply Current | $V_{CC}$ = 3.6V | One Input at 3V, Other Inputs at $V_{CC}$ or GND | | | 750 | |
| $C_{IN}$ | Input Capacitance | $V_I$ = 3.0V or 0 | | | 3.0 | | pF |
| $C_{OFF}$ | A/B Capacitance Switch Off | $V_O$ = 3.0V or 0 | Switch Off | | 8.5 | | |
| $R_{ON}$(2) | Switch On Resistance | $V_I$ = 0 | $I_I$ = 64mA | | 5 | 8 | Ω |
| | | | $I_I$ = 24mA | | 5 | 8 | |
| | | $V_I$ = 2.4V | $I_I$ = 15mA | | 10 | 15 | |

**Notes:**
1. This is the increase in supply current for each input ($\overline{OE}$ only) that is at the specified voltage level rather than $V_{CC}$ or GND.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## Truth Table

| $\overline{OE}$ | Function |
|---|---|
| L | A port = B port |
| H | A port = Z, B Port = BIASV |

## Switching Characteristics over Operating Range

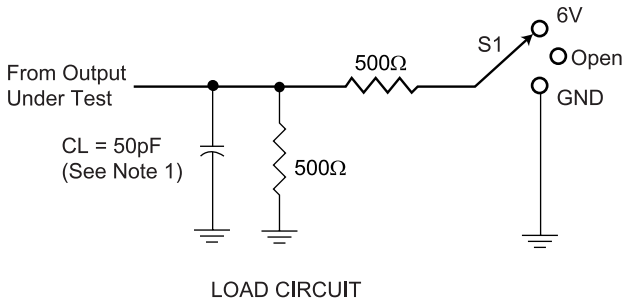
(Switching characteristics over recommended operating free-air temperature range unless otherwise noted)

| Parameter | Test Conditions | From (Input) | To (Output) | $V_{CC}$ = 3.3V ±10% | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| $t_{PD}$(1) | | A or B | B or A | | 0.25 | ns |
| $t_{PZH}$ | BIASV = GND | $\overline{OE}$ | A or B | | 4.5 | |
| $t_{PZL}$ | BIASV = 3V | | | | 4.5 | |
| $t_{PHZ}$ | BIASV = GND | | | | 5.0 | |
| $t_{PLZ}$ | BIASV = 3V | | | | 5.0 | |

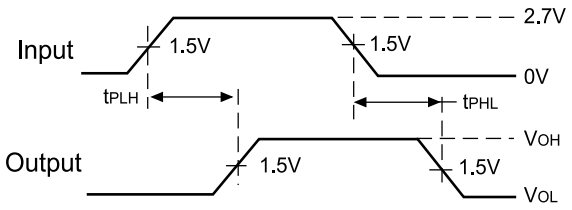
**Note:**

1. The propagation delay is the calculated RC time of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

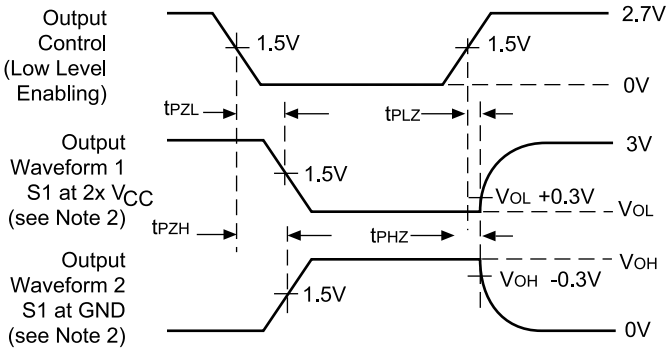
## Parameter Measurements ($V_{CC}$ = 2.7 and 3.3V ±10%)




| Test | S1 |
|---|---|
| $t_{PD}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6V |
| $t_{PHZ}/t_{PZH}$ | GND |




Voltage Waveforms Propagation Delay Times



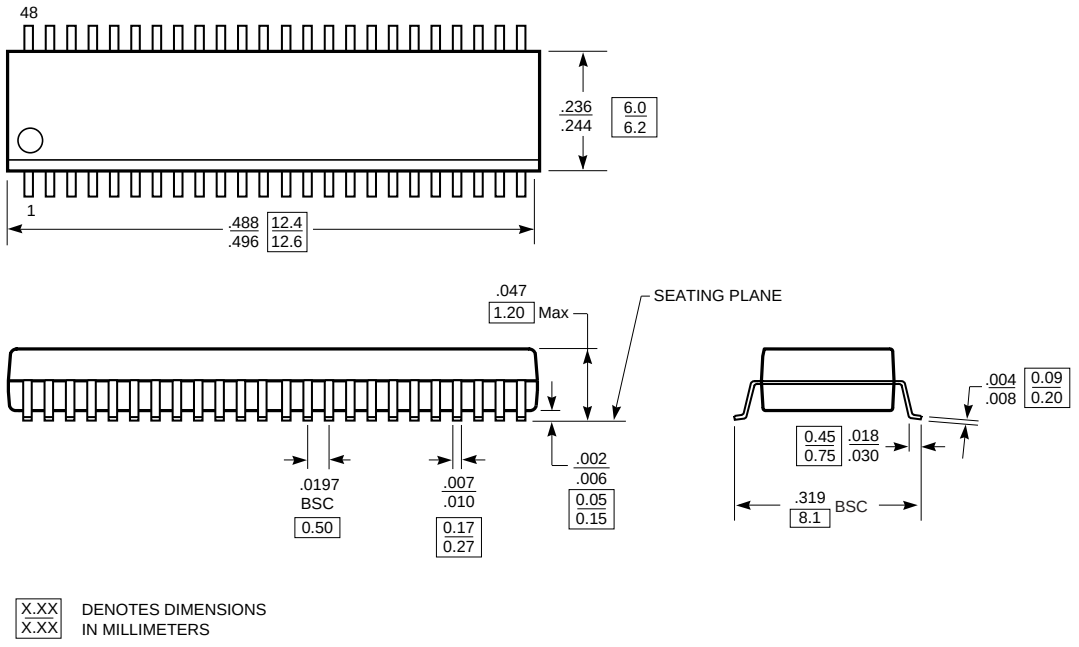

Voltage Waveforms Enable and Disable Times

**Figure 2. Load Circuit and Voltage Waveforms**

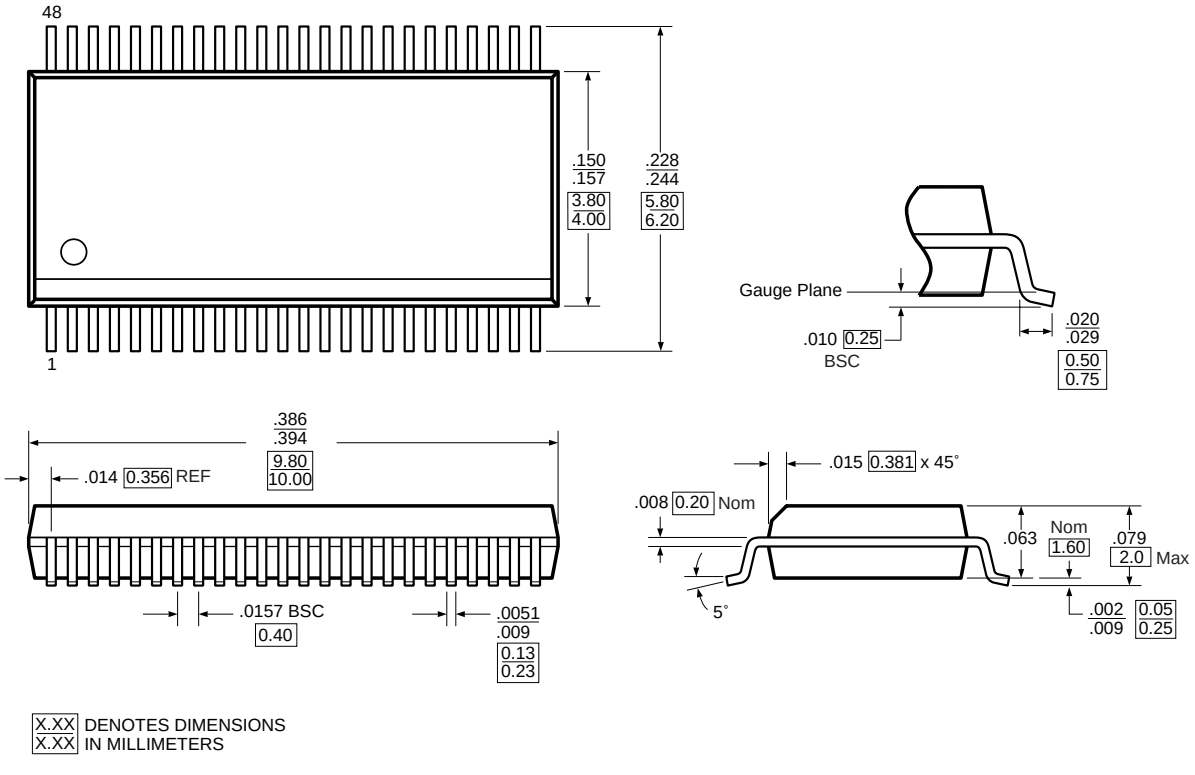
**Notes:**

1. $C_L$ includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O$ = 50Ω, $t_R$ ≤ 2.5ns, $t_F$ ≤ 2.5ns.
4. The outputs are measured one at a time with one transition per measurement.
5. $t_{TPZ}$ and $t_{PHZ}$ are the same as $t_{DIS}$
6. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{EN}$
7. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{PD}$

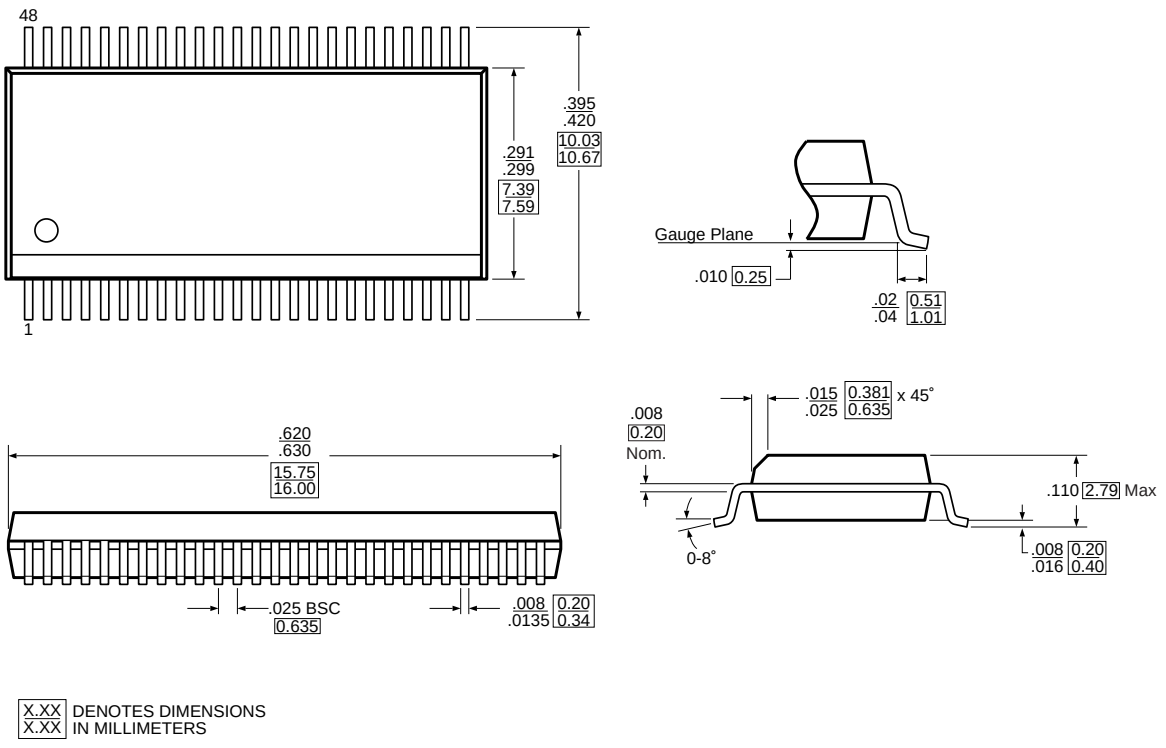
## 48-Pin TSSOP (A) Package




## 48-Pin BQSOP (B) Package



## 48-Pin SSOP (V) Package




## Order Information

| Part | Pin - Package | Width | Temperature |
|---|---|---|---|
| PI3B16215A | 56-TSSOP (A56) | 240-mil | –40ºC to +85ºC |
| PI3B16215B | 56-BQSOP (B56) | 150-mil | |
| PI3B16215V | 56-SSOP (V56) | 300-mil | |

## Applications Information

### Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a +3.3V supply, IN may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

### Power-Supply Sequencing

Proper power-supply sequencing is recommended for all CMOS devices. Always apply $V_{CC}$ before applying $V_{BIAS}$ and signals to input/output or control pins.

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