# NPC

## OVERVIEW

The SM8703CV is a 27MHz master clock, 5-system output clock generator for DVD players. It has 2 built-in PLLs that, with the addition of a single crystal oscillator element, can generate 384fs, 512fs and 768fs clocks which are necessary for MPEG2 systems, plus independent fixed-frequency 27MHz and 33.8688MHz output clocks. Each output has an output disable function, when the output is not used, to suppress unwanted radiation. Also, the normal output frequency ratio between each output is maintained so that the visual and audio signals remain synchronized. Supported sampling frequencies (fs) include 44.1 and 48kHz.

## FEATURES

- 27MHz master clock (internal PLL reference clock)
- Generated clocks
  - 27MHz output
  - 33.8688MHz output
  - 384fs output
  - 512fs output
  - 768fs output
- Sampling frequency fs
  - 44.1/48kHz
- Output disable function
- Low jitter output: 100ps (typ, 15pF load)
- Supply voltage: 3.3V
- 24-pin VSOP package

## APPLICATIONS

- DVD players
- Set-top boxes
- MPEG2 systems

## ORDERING INFORMATION

| Device | Package |
|---|---|
| SM8703CV | 24-pin VSOP |

## PINOUT

(Top view)
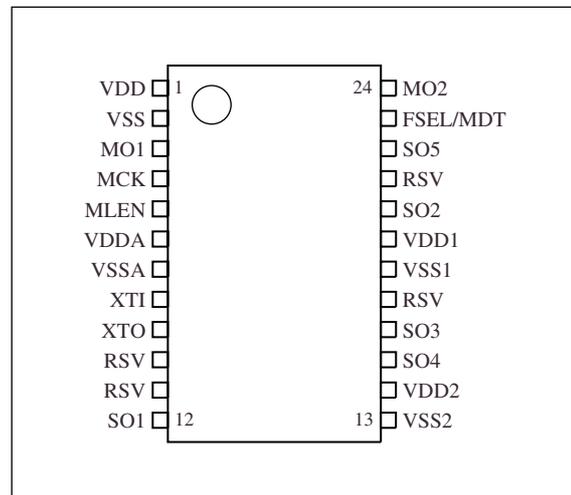


## PACKAGE DIMENSIONS

(Unit: mm)
Weight: 0.1g
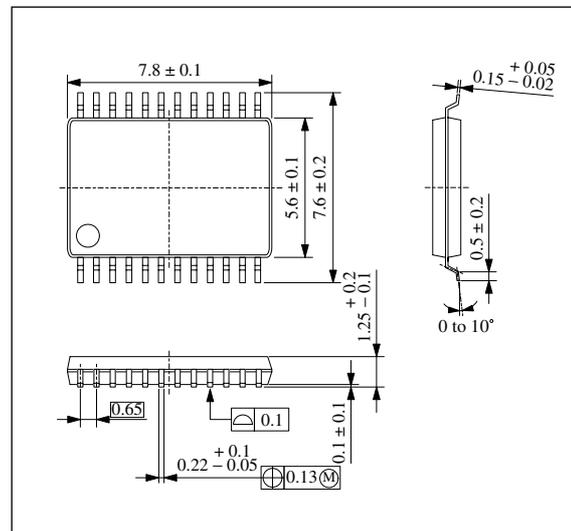
# BLOCK DIAGRAM
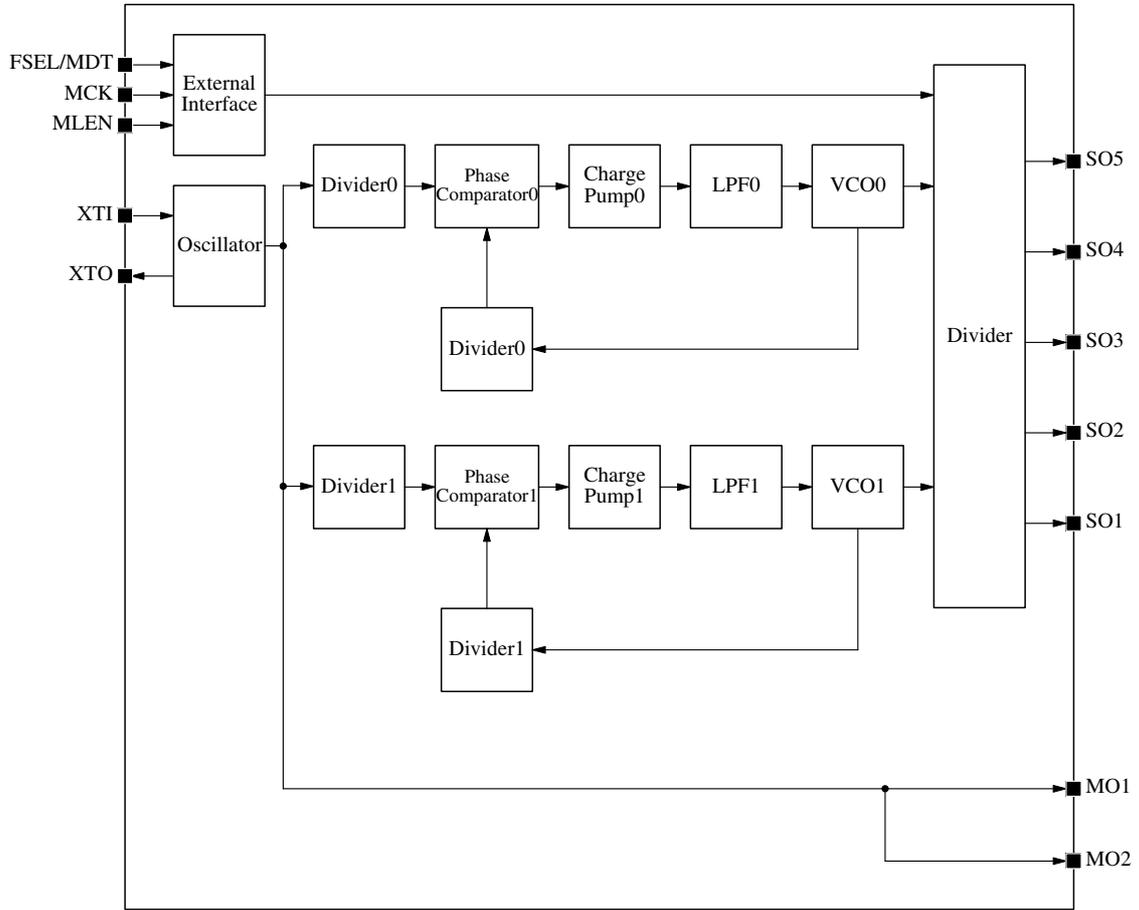
## PIN DESCRIPTION

| Number | Name | I/O | Description |
|--------|------|-----|-------------|
| 1 | VDD | – | Power supply for Digital block |
| 2 | VSS | – | VSS for Digital block |
| 3 | MO1 | O | 27MHz fixed-frequency output 1 |
| 4 | MCK | Ip[1] | Serial interface bit clock input |
| 5 | MLEN | Ip[1] | Serial interface latch enable input |
| 6 | VDDA | – | Power supply for Analog block |
| 7 | VSSA | – | VSS for Analog block |
| 8 | XTI | I | Reference signal crystal oscillator element connection or external clock input |
| 9 | XTO | O | Reference signal crystal oscillator element connection |
| 10 | RSV | – | Reserved (must be open) |
| 11 | RSV | – | Reserved (must be open) |
| 12 | SO1 | O | 33.8688MHz fixed-frequency output |
| 13 | VSS2 | – | VSS for Output buffer |
| 14 | VDD2 | – | Power supply for Output buffer |
| 15 | SO4 | O | 512fs output |
| 16 | SO3 | O | 512fs output |
| 17 | RSV | – | Reserved (must be open) |
| 18 | VSS1 | – | VSS for Output buffer |
| 19 | VDD1 | – | Power supply for Output buffer |
| 20 | SO2 | O | 384fs output |
| 21 | RSV | – | Reserved (must be open) |
| 22 | SO5 | O | 768fs output |
| 23 | FSEL/MDT | Ip[1] | Parallel mode: Sampling frequency select signal input<br>Serial mode: Control data input |
| 24 | MO2 | O | 27MHz fixed-frequency output 2 |

1. Schmitt trigger input with internal pull-up resistor

# SPECIFICATIONS

## Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage range | $V_{DDA}$, $V_{DD}$, $V_{DD1}$, $V_{DD2}$ | | $-0.3$ to $6.5$ | V |
| Supply voltage deviation | $V_{DDA} - V_{DD}$, $V_{DDA} - V_{DD1}$, $V_{DDA} - V_{DD2}$, $V_{DD} - V_{DD1}$, $V_{DD} - V_{DD2}$, $V_{DD1} - V_{DD2}$ | | $\pm0.1$ | V |
| Ground voltage deviation | $V_{SSA} - V_{SS}$, $V_{SSA} - V_{SS1}$, $V_{SSA} - V_{SS2}$, $V_{SS} - V_{SS1}$, $V_{SS} - V_{SS2}$, $V_{SS1} - V_{SS2}$ | | $\pm0.1$ | V |
| Input voltage range | $V_{IN}$ | Digital inputs | $-0.3$ to $V_{DD} + 0.3$ | V |
| Output voltage range | $V_{OUT}$ | Digital outputs | $-0.3$ to $V_{DD} + 0.3$ | V |
| Power dissipation | $P_D$ | | 300 | mW |
| Storage temperature range | $T_{stg}$ | | $-55$ to $125$ | °C |

## Recommended Operating Conditions

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage ranges | $V_{DDA}$, $V_{DD}$, $V_{DD1}$, $V_{DD2}$ | | 3.0 to 3.6 | V |
| Operating temperature range | $T_{opr}$ | | $-40$ to $85$ | °C |

## DC Electrical Characteristics

External clock, Ta = –40 to 85°C, $V_{DDA} = V_{DD} = V_{DD1} = V_{DD2}$ = 3.0 to 3.6V unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Current consumption | $I_{DD}$ | All supplies. $V_{DDA} = V_{DD} = V_{DD1} = V_{DD2}$ = 3.3V, Ta = 25°C, fs = 48kHz, Crystal oscillator element, no load on all outputs | – | 32 | 45 | mA |
| HIGH-level input voltage | $V_{IH}$ | XTI, FSEL/MDT, MCK, MLEN | $0.8V_{DD}$ | – | – | V |
| LOW-level input voltage | $V_{IL}$ | XTI, FSEL/MDT, MCK, MLEN | – | – | $0.2V_{DD}$ | V |
| HIGH-level input current | $I_{IH1}$ | FSEL/MDT, MCK, MLEN (Note 1) $V_{IN} = V_{DD}$ | – | – | 1 | µA |
| LOW-level input current | $I_{IL1}$ | FSEL/MDT, MCK, MLEN (Note 1) $V_{IN}$ = 0V | – | – | –100 | µA |
| HIGH-level input current | $I_{IH2}$ | XTI, $V_{IN} = V_{DD}$ | – | – | 40 | µA |
| LOW-level input current | $I_{IL2}$ | XTI, $V_{IN}$ = 0V | – | – | –40 | µA |
| HIGH-level output voltage | $V_{OH}$ | All outputs. $I_{OH}$ = –2mA | $V_{DD} - 0.4$ | – | – | V |
| LOW-level output voltage | $V_{OL}$ | All outputs. $I_{OL}$ = 4mA | – | – | 0.4 | V |

Note 1: Schmitt trigger input with internal pull-up resistor

## AC Electrical Characteristics

External clock, Ta = –40 to 85°C, $V_{DDA} = V_{DD} = V_{DD1} = V_{DD2}$ = 3.0 to 3.6V unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| XTI external input clock frequency | $f_M$ | | – | 27.0000 | – | MHz |
| Output clock rise time | $t_R$ | All outputs, 0.2 to $0.8V_{DD}$, $C_L$ = 15pF | – | 2.0 | – | ns |
| Output clock fall time | $t_F$ | All outputs, 0.8 to $0.2V_{DD}$, $C_L$ = 15pF | – | 2.0 | – | ns |
| Output clock jitter | JITTER | All outputs, Standard tolerance, Crystal oscillator element, $C_L$ = 15pF | – | 100 | – | ps |
| Output clock duty[1] | DUTY | All outputs, Crystal oscillator element, $C_L$ = 15pF | 45 | 50 | 55 | % |
| Settling time | $t_S$ | All outputs | – | – | 100 | ns |
| Power-up time[2] | $t_P$ | All outputs | – | 15 | 30 | ms |

1. 1.4V to 1.4V. Ta = 20°C. The characteristics of output clock jitter and output clock duty depends on crystal oscillator.
   NPC's standard crystal oscillator: R = 10.5Ω, L = 5.38mH, Ca = 6.74fF, Cb = 1.85pF
   measurement apparatus: HP4195
   Load capacitance: C1 = 7pF, C2 = 11pF
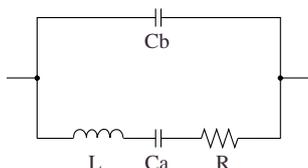


2. Time from OFF condition to stable frequency output.

## Serial Interface AC Characteristics

External clock, Ta = –40 to 85°C, $V_{DDA} = V_{DD} = V_{DD1} = V_{DD2} = 3.0$ to 3.6V unless otherwise noted.

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| MCK HIGH-level pulsewidth | $t_{MCWH}$ | | 40 | – | – | ns |
| MCK LOW-level pulsewidth | $t_{MCWL}$ | | 40 | – | – | ns |
| MCK pulse cycle time | $t_{MCY}$ | | 100 | – | – | ns |
| MDT setup time | $t_{MDS}$ | | 40 | – | – | ns |
| MDT hold time | $t_{MDH}$ | | 40 | – | – | ns |
| MLEN setup time[1] | $t_{MLS}$ | | 40 | – | – | ns |
| MLEN hold time[2] | $t_{MLH}$ | | 40 | – | – | ns |
| MLEN HIGH-level pulsewidth | $t_{MHH}$ | | 200 | – | – | ns |
| MLEN LOW-level pulsewidth | $t_{MLL}$ | | $16 \times t_{MCY}$ | – | – | ns |

1. Time from the MLEN falling edge to the next MCK rising edge. If the MCK clock stops after the LSB, the MLEN rise timing is optional.
2. Time from MCK rising edge corresponding to the LSB to the MLEN rising edge.
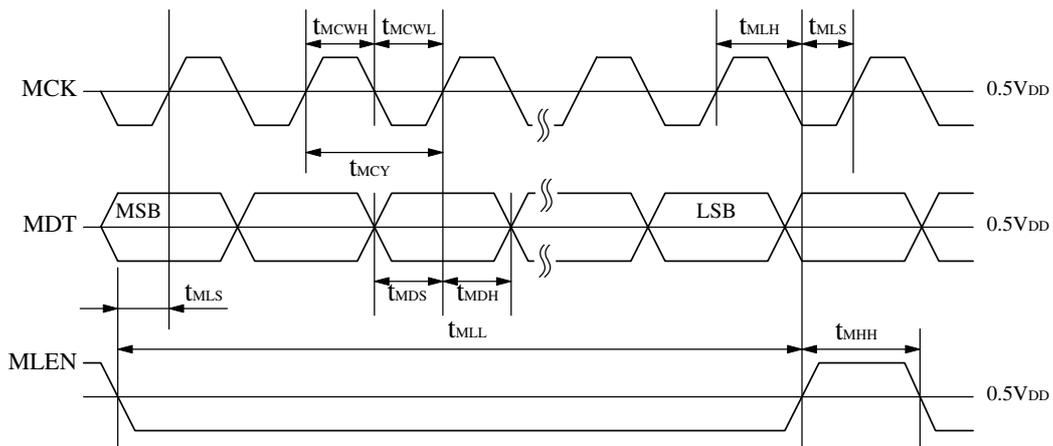
## FUNCTIONAL DESCRIPTION

### 27MHz Master Clock

The 27MHz master clock is generated either by connecting a crystal oscillator element between XTI (pin 8) and XTO (pin 9), as shown in figure 1, or by connecting an external 27MHz clock to XTI, as shown in figure 2. The crystal oscillator element must be used in fundamental frequency mode.
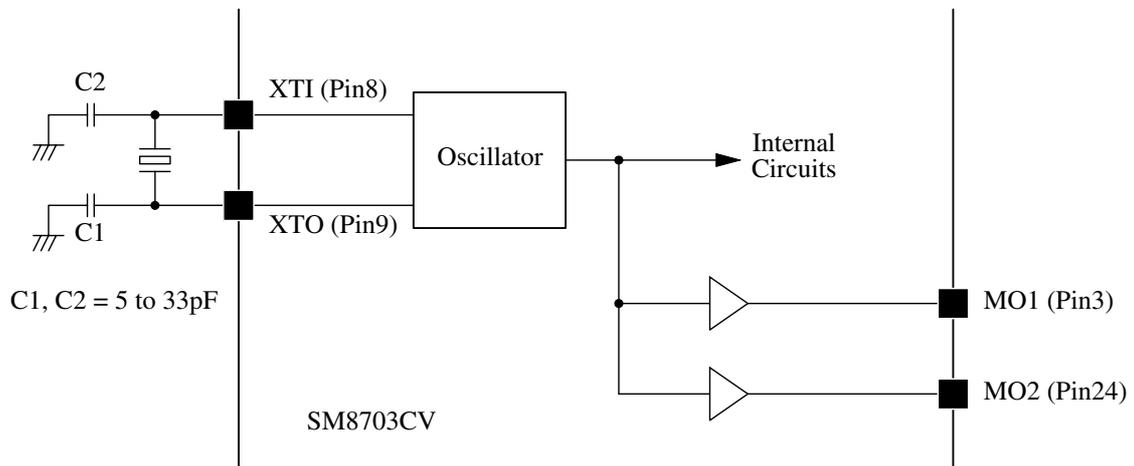


Figure 1. Crystal oscillator connection
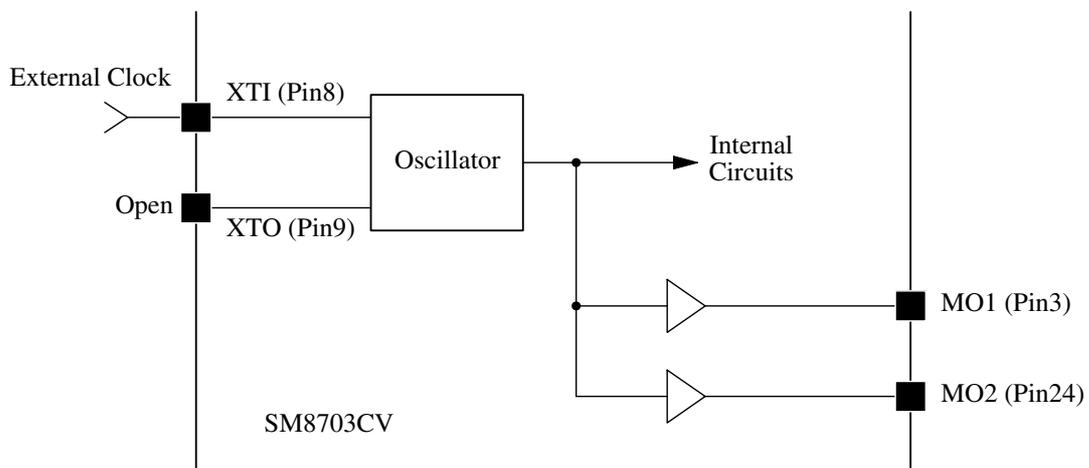


Figure 2. External clock input

## Sampling Frequency and Output Clock Frequency

The SM8703CV generates several output clocks from the 27MHz master clock, with frequencies of 384fs (SO2), 512fs (SO3, SO4) and 768fs (SO5), where fs is the sampling frequency selected by external control inputs. SO1 outputs a 33.8688MHz clock. The supported sampling frequencies are 44.1kHz and 48kHz, selected by the sampling frequency select pin (FSEL). The generated frequencies are shown in table 1.

Table 1. Sampling frequency and output clock frequency

| FSEL | Sampling frequency fs | Output clock frequency [MHz] | | | |
|---|---|---|---|---|---|
| | | SO1 | SO2 | SO3, SO4 | SO5 |
| LOW | 44.1kHz | 33.8688 | 16.9344 | 22.5792 | 33.8688 |
| HIGH | 48kHz | 33.8688 | 18.4320 | 24.5760 | 36.8640 |

## Enable/Disable control

A 3-wire serial interface is provided using MCK (pin 4), MLEN (pin 5), and MDT (pin 23, MDT/FSEL). Using serial control, each output frequency can be enabled (disabled when LOW) individually, or disabled to prevent unwanted output.
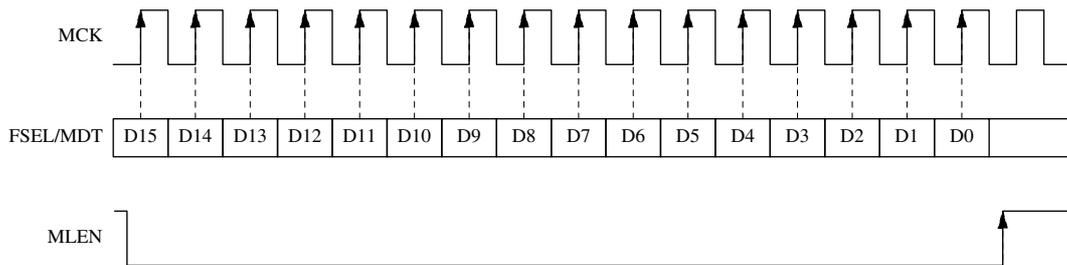


Figure 3. Serial control format

The 16-bit mode register (MREG) is shown in Figure 4. The name and function of each bit are shown in Tables 2 and 3. Serial control is enabled by setting D15-D10 to "011100".



| MREG | 0 | 1 | 1 | 1 | 0 | 0 | RSV | CE5 | CE4 | CE3 | CE2 | CE1 | RSV | RSV | RSV | RSV |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
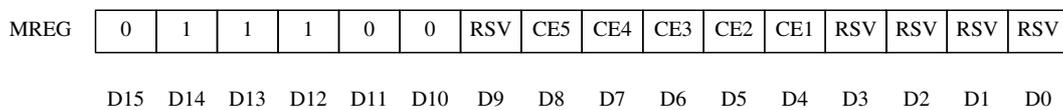
Note: RSV is fixed LOW.

Figure 4. Mode register

Table 2. Mode register function

| Bit | Name | Function |
|-----|------|----------|
| D9 | RSV | Must be "LOW" |
| D8 | CE5 | SO2 output enable/disable |
| D7 | CE4 | SO3, SO4 output enable/disable |
| D6 | CE3 | SO5 output enable/disable |
| D5 | CE2 | SO1 output enable/disable |
| D4 | CE1 | MO1, MO2 output enable/disable |
| D3/D2/D1/D0 | RSV | Must be "LOW" |

Table 3. Clock output control settings (CE5 to 1)

| CE5 to CE1 | Clock output |
|------------|--------------|
| LOW | Disable (Output fixed "LOW") |
| HIGH | Enable (Default) |

**Note**

The output frequency changes depending on the MDT pin function (as MDT and FSEL, the sampling frequency select signal input, share a common pin). Refer to the section "Settling Time (when the sampling frequency is changed)".
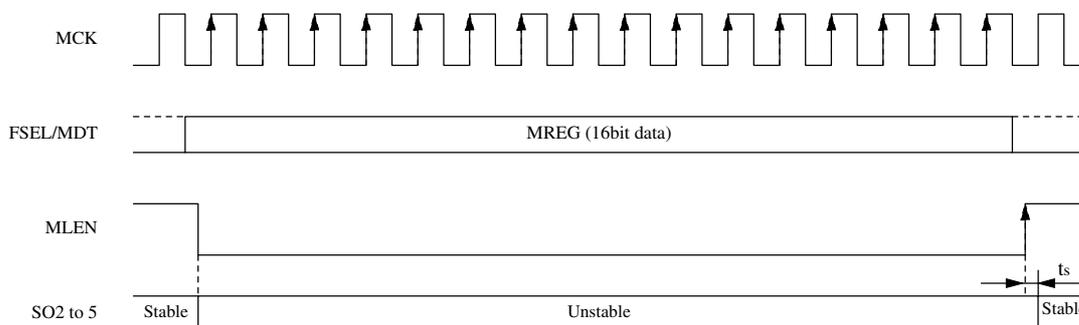


Figure 5. Serial transfer timing

## Settling Time (when the sampling frequency is changed)

The output response when the frequency is changed is shown in figure 6.
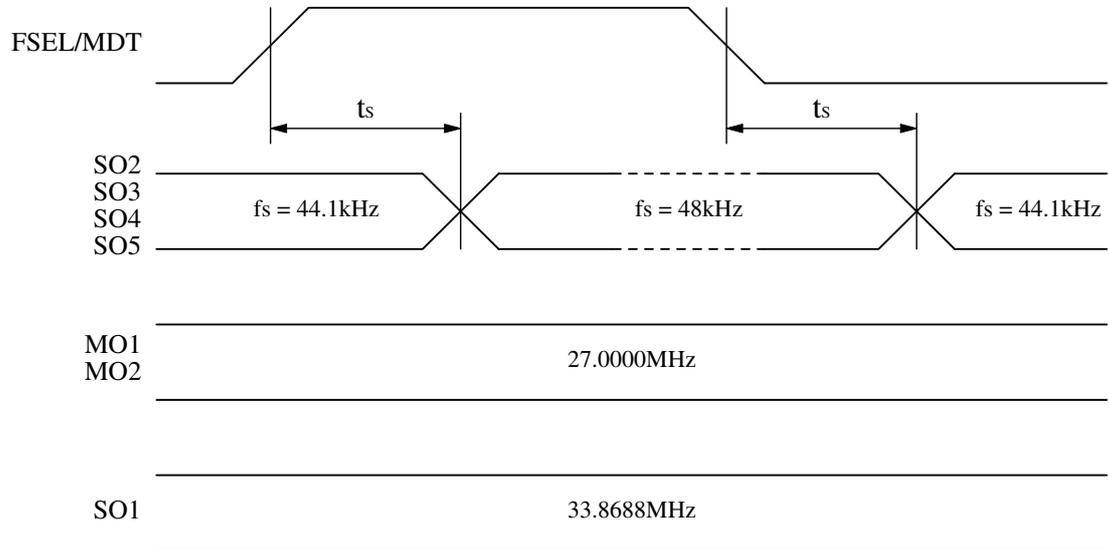
Figure 6. System clock transient timing

## TYPICAL APPLICATION
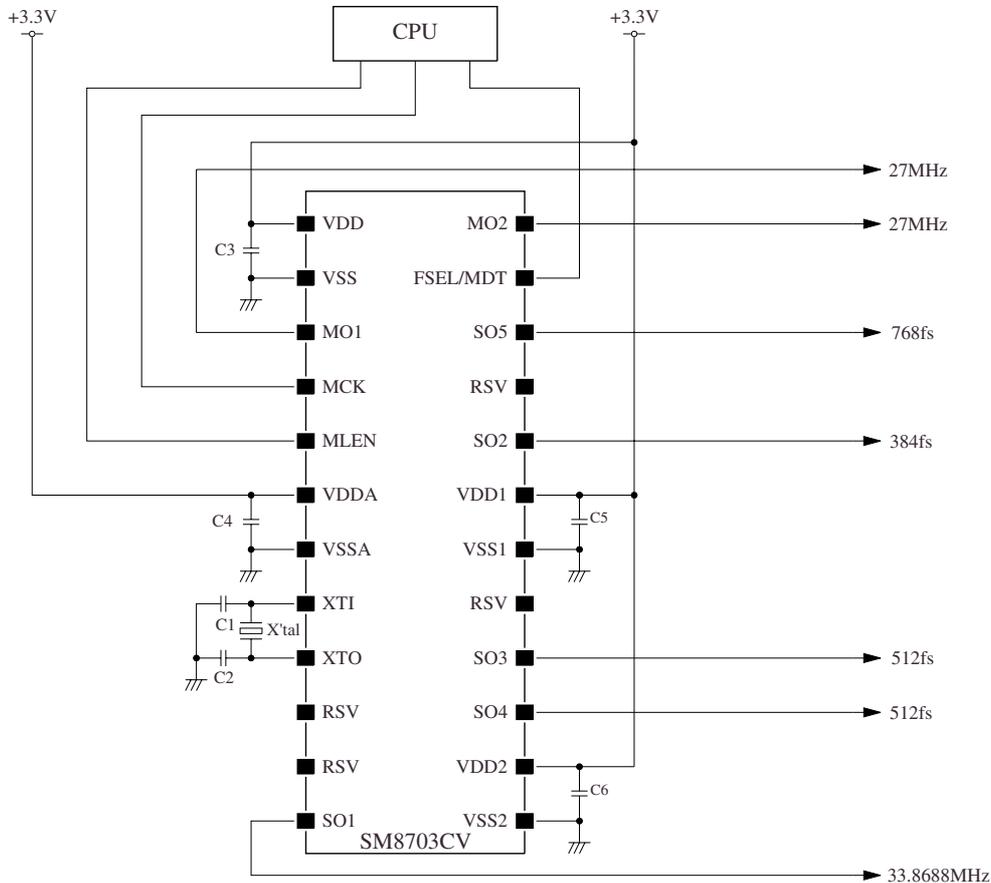


- Connect the decoupling capacitors (approximately 0.1μF and 1000pF) in parallel, as close to the power supply pins as possible.
- A solid VSS pattern beneath the IC should be used to minimize noise.
- Master clock stability affects the stability of the other outputs. If a crystal oscillator is used, the oscillator element and load capacitors should be placed as close to the SM8703CV as possible, and connected with wires as short as possible. The crystal oscillator element and load capacitor combination has an effect on frequency accuracy, and the load capacitors (C1, C2) should be selected to match the required application.
- The SM8703CV outputs several high-frequency clocks, so the supply wiring pattern (including decoupling capacitors) should be considered carefully. In particular, the output supply wiring and PLL supply wiring should separated to prevent noise insertion. The output wiring capacitance should be minimized as much as possible to prevent noise. If necessary, the output clocks can be buffered.

- Power supply and VSS pins.
  - VDD   : Power supply for digital block (CPU I/F*, MO1, MO2)
  - VSS    : VSS for digital block (CPU I/F*, MO1, MO2)
  - VDDA : Power supply for PLL block (XTI, XTO, PLL/VCO)
  - VSSA : VSS for PLL block (XTI, XTO, PLL/VCO)
  - VDD1 : Power supply for output block (except SO1)
  - VSS1  : VSS for output block (except SO1)
  - VDD2 : Power supply for SO1
  - VSS2  : VSS for SO1

*: CPU I/F: FSEL/MDT, MLEN, MCK

Please pay your attention to the following points at time of using the products shown in this document.