

2.5V Single Data Rate 1:10 Clock Buffer Terabuffer

Features

- Guaranteed Low Skew < 25pS (max)
- Very low duty cycle distortion
- High speed propagation delay < 2.5nS. (max)
- Up to 250MHz operation
- Very low CMOS power levels
- 1.5V V_{DDQ} for HSTL interface
- Hot Insertable and over-voltage tolerant inputs
- 3-level inputs for selectable interface
- Selectable HSTL, eHSTL, 1.8V / 2.5V LVTTTL, or LVEPECL input interface
- Selectable differential or single-ended inputs and ten single ended outputs
- 2.5V Supply Voltage
- Available in TSSOP Package

Functional Description

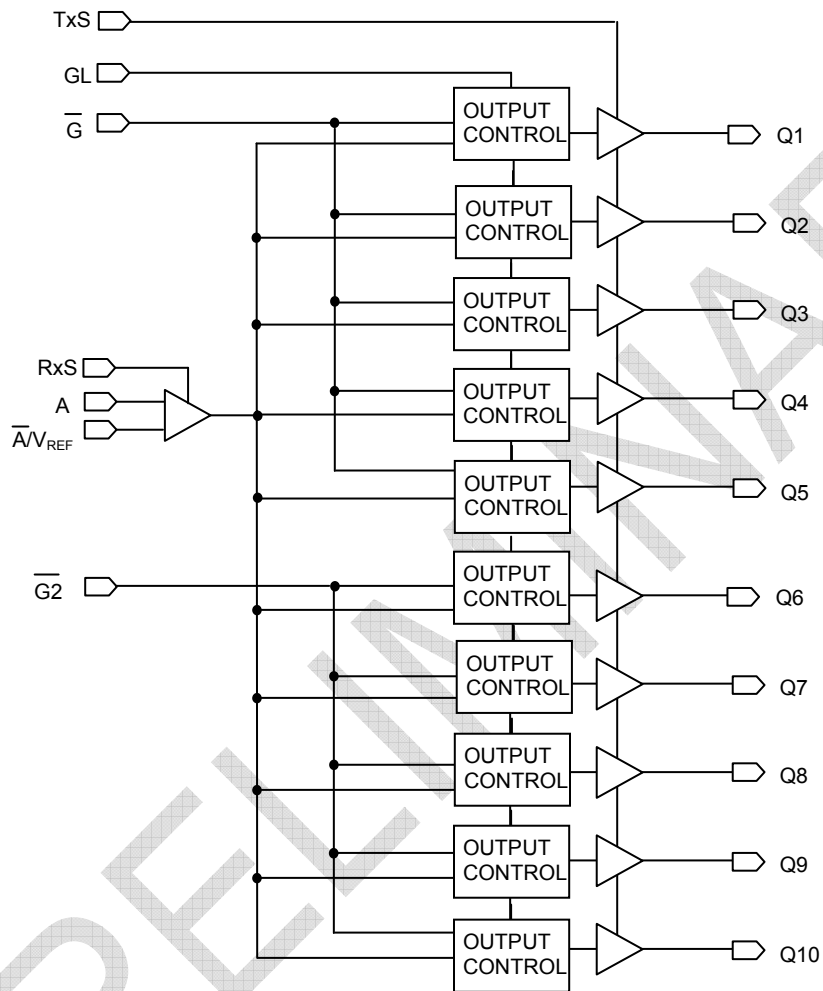
The PCS2P5T907A 2.5V single data rate (SDR) clock buffer is a user-selectable single-ended or differential input to ten single-ended outputs built on advanced metal CMOS technology. The SDR clock buffer fanout from a single or differential input to ten single-ended outputs reduces the loading on the preceding driver and provides an efficient clock distribution network. The PCS2P5T907A can act as a translator from a differential HSTL, eHSTL, 1.8V/2.5V LVTTTL, LVEPECL, or single-ended 1.8V/2.5V LVTTTL input to HSTL, eHSTL, 1.8V/2.5V LVTTTL outputs. Selectable interface is controlled by 3-level input signals that may be hard-wired to appropriate high-mid-low levels.

The PCS2P5T907A has two output banks that can be asynchronously enabled/ disabled. Multiple power and grounds reduce noise.

Applications:

PCS2P5T907A is targeted towards Clock and signal distribution applications.

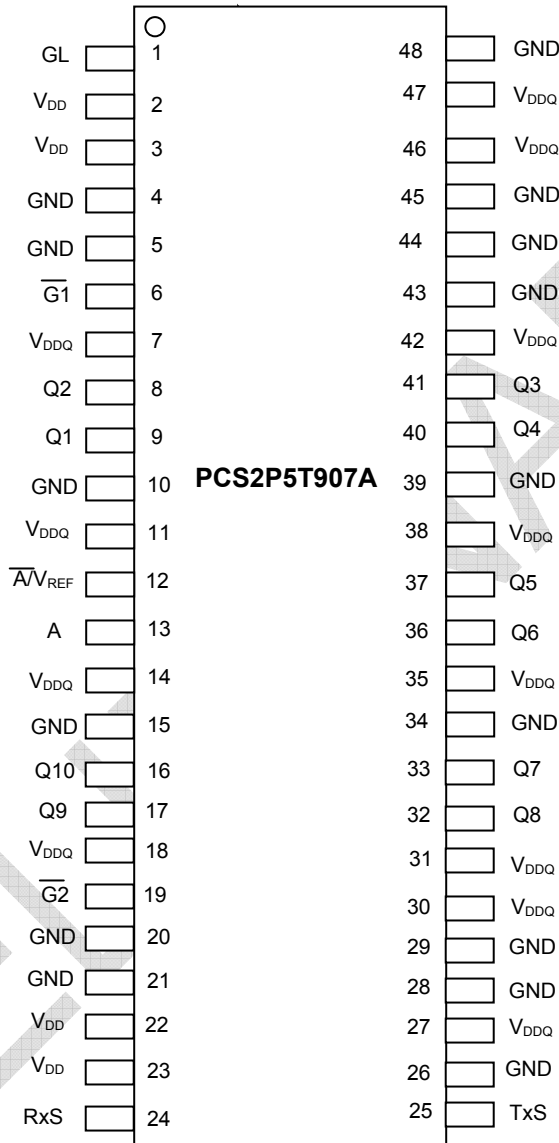
Block Diagram



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Pin Configuration



Pin Description¹

Symbol	I/O	Type	Description
A	I	Adjustable ¹	Clock input. A is the "true" side of the differential clock input. If operating in single-ended mode, A is the clock input.
\bar{A} / V_{REF}	I	Adjustable ¹	Complementary clock input. \bar{A}/V_{REF} is the "complementary" side of A if the input is in differential mode. If operating in single-ended mode, A/V_{REF} is connected to GND. For single-ended operation in differential mode, A/V_{REF} should be set to the desired toggle voltage for A: 2.5V LVTTTL $V_{REF}= 1250mV$ 1.8V LVTTTL, eHSTL $V_{REF}= 900mV$ HSTL $V_{REF}= 750mV$ LVEPECL $V_{REF}= 1082mV$
$\bar{G}1$	I	LVTTTL ⁵	Gate for outputs Q1 through Q5. When $\bar{G}1$ is LOW, these outputs are enabled. When G1 is HIGH, these outputs are asynchronously disabled to the level designated by GL ⁴ .
$\bar{G}2$	I	LVTTTL ⁵	Gate for outputs Q6 through Q10. When $\bar{G}2$ is LOW, these outputs are enabled. When G2 is HIGH, these outputs are asynchronously disabled to the level designated by GL ⁴ .
GL	I	LVTTTL ⁵	Specifies output disable level. If HIGH, the outputs disable HIGH. If LOW, the outputs disable LOW.
Qn	O	Adjustable ²	Clock outputs
RxS	I	3 Level ³	Selects single-ended 2.5V LVTTTL (HIGH), 1.8V LVTTTL (MID) clock input or differential (LOW) clock input
TxS	I	3 Level ³	Sets the drive strength of the output drivers to be 2.5V LVTTTL (HIGH), 1.8V LVTTTL (MID) or HSTL (LOW) compatible. Used in conjunction with V_{DDQ} to set the interface levels.
V_{DD}	I	PWR	Power supply for the device core and inputs
V_{DDQ}	I	PWR	Power supply for the device outputs. When utilizing 2.5V LVTTTL outputs, V_{DDQ} should be connected to V_{DD} .
GND		PWR	Power supply return for all power

NOTES:

- Inputs are capable of translating the following interface standards. User can select between:
 Single-ended 2.5V LVTTTL levels or Differential 2.5V/1.8V LVTTTL levels
 Single-ended 1.8V LVTTTL levels or Differential HSTL and eHSTL levels
 Differential LVEPECL levels
- Outputs are user selectable to drive 2.5V, 1.8V LVTTTL, eHSTL, or HSTL interface levels when used with the appropriate V_{DDQ} voltage.
- 3 level inputs are static inputs and must be tied to V_{DD} or GND or left floating. These inputs are not hot-insertable or over-voltage tolerant.
- Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.
- Pins listed as LVTTTL inputs will accept 2.5V signals when RxS = HIGH or 1.8V signals when RxS = LOW or MID.

Absolute Maximum Ratings¹

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage ²	-0.5 to +3.6	V
V_{DDQ}	Output Power Supply ²	-0.5 to +3.6	V
V_i	Input Voltage	-0.5 to +3.6	V
V_o	Output Voltage ³	-0.5 to $V_{DDQ} + 0.5$	V
V_{REF}	Reference Voltage ³	-0.5 to +3.6	V
T_{STG}	Storage Temperature	-65 to +165	°C
T_J	Junction Temperature	150	°C

Note:

- These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.
- V_{DDQ} and V_{DD} internally operate independently. No power sequencing requirements need to be met.
- Not to exceed 3.6V.

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Capacitance¹ (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min	Typ	Max	Unit
C _{IN}	Input Capacitance		3.5		pF

NOTE:

1. This parameter is measured at characterization but not tested. Capacitance applies to all inputs except RxS and TxS.

Recommended Operating Range

Symbol	Description	Min	Typ	Max	Unit
T _A	Ambient Operating Temperature	-40	+25	+85	°C
V _{DD} ¹	Internal Power Supply Voltage	2.4	2.5	2.6	V
V _{DDQ} ¹	HSTL Output Power Supply Voltage	1.4	1.5	1.6	V
	Extended HSTL and 1.8V LVTTTL Output Power Supply Voltage	1.65	1.8	1.95	V
	2.5V LVTTTL Output Power Supply Voltage		V _{DD}		V
V _T	Termination Voltage		V _{DDQ} / 2		V

NOTE:

1. All power supplies should operate in tandem; if V_{DD} or V_{DDQ} is at a maximum, then V_{DDQ} or V_{DD} (respectively) should be at a maximum, and vice-versa.

Input/Output Selection¹

Input	Output	Input	Output		
2.5V LVTTTL SE	2.5V LVTTTL	2.5V LVTTTL SE	eHSTL		
1.8V LVTTTL SE		1.8V LVTTTL SE			
2.5V LVTTTL DSE		2.5V LVTTTL DSE			
1.8V LVTTTL DSE		1.8V LVTTTL DSE			
LVEPECL DSE		LVEPECL DSE			
eHSTL DSE		eHSTL DSE			
HSTL DSE		HSTL DSE			
2.5V LVTTTL DIF		2.5V LVTTTL DIF			
1.8V LVTTTL DIF		1.8V LVTTTL DIF			
LVEPECL DIF		LVEPECL DIF			
eHSTL DIF		eHSTL DIF			
HSTL DIF		HSTL DIF			
2.5V LVTTTL SE		1.8V LVTTTL		2.5V LVTTTL SE	HSTL
1.8V LVTTTL SE				1.8V LVTTTL SE	
2.5V LVTTTL DSE	2.5V LVTTTL DSE				
1.8V LVTTTL DSE	1.8V LVTTTL DSE				
LVEPECL DSE	LVEPECL DSE				
eHSTL DSE	eHSTL DSE				
HSTL DSE	HSTL DSE				
2.5V LVTTTL DIF	2.5V LVTTTL DIF				
1.8V LVTTTL DIF	1.8V LVTTTL DIF				
LVEPECL DIF	LVEPECL DIF				
eHSTL DIF	eHSTL DIF				
HSTL DIF	HSTL DIF				

NOTE: 1. The INPUT/OUTPUT SELECTION Table describes the total possible combinations of input and output interfaces. Single-Ended (SE) inputs in a single-ended mode require the A_{VREF} pin to be connected to GND. Differential Single-Ended (DSE) is for single-ended operation in differential mode.

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requiring a V_{REF} . Differential (DIF) inputs are used only in differential mode.

DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IHH}	Input HIGH Voltage Level ¹	3-Level Inputs Only	$V_{DD} - 0.4$		V
V_{IMM}	Input MID Voltage Level ¹	3-Level Inputs Only	$V_{DD}/2 - 0.2$	$V_{DD}/2 + 0.2$	V
V_{ILL}	Input LOW Voltage Level ¹	3-Level Inputs Only		0.4	V
I_3	3-Level Input DC Current (RxS, TxS)	$V_{IN} = V_{DD}$ HIGH Level		200	μA
		$V_{IN} = V_{DD}/2$ MID Level	-50	+50	
		$V_{IN} = GND$ LOW Level	-200		

NOTE:

1. These inputs are normally wired to V_{DD} , GND, or left floating. Internal termination resistors bias unconnected inputs to $V_{DD}/2$.

DC Electrical Characteristics Over Operating Range for HSTL¹

Symbol	Parameter	Test Conditions	Min	Typ ⁷	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current ⁹	$V_{DD} = 2.6V$ $V_I = V_{DDQ}/GND$			± 5	μA
I_{IL}	Input LOW Current ⁹	$V_{DD} = 2.6V$ $V_I = GND/V_{DDQ}$			± 5	
V_{IK}	Clamp Diode Voltage	$V_{DD} = 2.4V$, $I_{IN} = -18mA$		-0.7	- 1.2	V
V_{IN}	DC Input Voltage		-0.3		+3.6	V
V_{DIF}	DC Differential Voltage ^{2,8}		0.2			V
V_{CM}	DC Common Mode Input Voltage ^{3,8}		680	750	900	mV
V_{IH}	DC Input HIGH ^{4,5,8}		$V_{REF} + 100$		-	mV
V_{IL}	DC Input LOW ^{4,6,8}				$V_{REF} - 100$	mV
V_{REF}	Single-Ended Reference Voltage ^{4,8}			750	-	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	$I_{OH} = -8mA$	$V_{DDQ} - 0.4$			V
		$I_{OH} = -100\mu A$	$V_{DDQ} - 0.1$			V
V_{OL}	Output LOW Voltage	$I_{OL} = 8mA$			0.4	V
		$I_{OL} = 100\mu A$			0.1	V

NOTES:

- See RECOMMENDED OPERATING RANGE table.
- V_{DIF} specifies the minimum input differential voltage ($V_{TR} - V_{CP}$) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP}) / 2$. Differential mode only.
- For single-ended operation, in differential mode, A/V_{REF} is tied to the DC voltage V_{REF} .
- Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- Typical values are at $V_{DD} = 2.5V$, $V_{DDQ} = 1.5V$, +25°C ambient.
- The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. The correct input interface table should be referenced.
- For differential mode ($RxS = LOW$), A and A/V_{REF} must be at the opposite rail.

Power Supply Characteristics for HSTL Outputs¹

Symbol	Parameter	Test Conditions ²	Typ	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	$V_{DDQ} = \text{Max.}$, Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V_{DDQ} Power Supply Current	$V_{DDQ} = \text{Max.}$, Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	$V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $C_L = 0\text{pF}$	20	30	$\mu\text{A}/\text{MHz}$
I_{DDQD}	Dynamic V_{DDQ} Power Supply Current per Output	$V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $C_L = 0\text{pF}$	30	50	$\mu\text{A}/\text{MHz}$
I_{TOT}	Total Power V_{DD} Supply Current	$V_{DDQ} = 1.5\text{V}$, $F_{\text{REFERENCE CLOCK}} = 100\text{MHz}$, $C_L = 15\text{pF}$	20	40	mA
		$V_{DDQ} = 1.5\text{V}$, $F_{\text{REFERENCE CLOCK}} = 250\text{MHz}$, $C_L = 15\text{pF}$	35	50	
I_{TOTQ}	Total Power V_{DDQ} Supply Current	$V_{DDQ} = 1.5\text{V}$, $F_{\text{REFERENCE CLOCK}} = 100\text{MHz}$, $C_L = 15\text{pF}$	35	70	mA
		$V_{DDQ} = 1.5\text{V}$, $F_{\text{REFERENCE CLOCK}} = 250\text{MHz}$, $C_L = 15\text{pF}$	50	100	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

Differential Input AC Test Conditions for HSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	1	V
V_X	Differential Input Signal Crossing Point ²	750	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t_R, t_F	Input Signal Edge Rate ⁴	1	V/nS

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

DC Electrical Characteristics Over Operating Range for eHSTL¹

Symbol	Parameter	Test Conditions	Min	Typ ⁷	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current ⁹	$V_{DD} = 2.6V$ $V_I = V_{DDQ}/GND$			± 5	μA
I_{IL}	Input LOW Current ⁹	$V_{DD} = 2.6V$ $V_I = GND/V_{DDQ}$			± 5	
V_{IK}	Clamp Diode Voltage	$V_{DD} = 2.4V$, $I_{IN} = -18mA$		- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		-0.3		+3.6	V
V_{DIF}	DC Differential Voltage ^{2,8}		0.2		-	V
V_{CM}	DC Common Mode Input Voltage ^{3,8}		800	900	1000	mV
V_{IH}	DC Input HIGH ^{4,5,8}		$V_{REF} + 100$		-	mV
V_{IL}	DC Input LOW ^{4,6,8}				$V_{REF} - 100$	mV
V_{REF}	Single-Ended Reference Voltage ^{4,8}			900	-	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	$I_{OH} = -8mA$	$V_{DDQ} - 0.4$			V
		$I_{OH} = -100\mu A$	$V_{DDQ} - 0.1$			V
V_{OL}	Output LOW Voltage	$I_{OL} = 8mA$			0.4	V
		$I_{OL} = 100\mu A$			0.1	V

NOTES:

- See RECOMMENDED OPERATING RANGE table.
- V_{DIF} specifies the minimum input differential voltage ($V_{TR} - V_{CP}$) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP}) / 2$. Differential mode only.
- For single-ended operation, in a differential mode, A / V_{REF} is tied to the DC voltage V_{REF} .
- Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- Typical values are at $V_{DD} = 2.5V$, $V_{DDQ} = 1.8V$, +25°C ambient.
- The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. The correct input interface table should be referenced.
- For differential mode (RxS = LOW), A and A / V_{REF} must be at the opposite rail.

Power Supply Characteristics for eHSTL Outputs¹

Symbol	Parameter	Test Conditions ²	Typ	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	$V_{DDQ} = \text{Max.}$, Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V_{DDQ} Power Supply Current	$V_{DDQ} = \text{Max.}$, Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	$V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $C_L = 0pF$	20	30	$\mu A/MHz$
I_{DDDQ}	Dynamic V_{DDQ} Power Supply Current per Output	$V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $C_L = 0pF$	40	60	$\mu A/MHz$
I_{TOT}	Total Power V_{DD} Supply Current	$V_{DDQ} = 1.8V$, $F_{REFERENCE\ CLOCK} = 100MHz$, $C_L = 15pF$	20	40	mA
		$V_{DDQ} = 1.8V$, $F_{REFERENCE\ CLOCK} = 250MHz$, $C_L = 15pF$	35	50	
I_{TOTQ}	Total Power V_{DDQ} Supply Current	$V_{DDQ} = 1.8V$, $F_{REFERENCE\ CLOCK} = 100MHz$, $C_L = 15pF$	40	80	mA
		$V_{DDQ} = 1.8V$, $F_{REFERENCE\ CLOCK} = 250MHz$, $C_L = 15pF$	80	160	

- NOTES: 1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
 2. The termination resistors are excluded from these measurements.
 3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

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Differential Input AC Test Conditions for eHSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	1	V
V_X	Differential Input Signal Crossing Point ²	900	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t_R, t_F	Input Signal Edge Rate ⁴	1	V/nS

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

DC Electrical Characteristics Over Operating Range for LVEPECL¹

Symbol	Parameter	Test Conditions	Min	Typ ²	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current ⁶	$V_{DD} = 2.6V$ $V_I = V_{DDQ}/GND$			± 5	μA
I_{IL}	Input LOW Current ⁶	$V_{DD} = 2.6V$ $V_I = GND/V_{DDQ}$			± 5	
V_{IK}	Clamp Diode Voltage	$V_{DD} = 2.4V, I_{IN} = -18mA$		-0.7	-1.2	V
V_{IN}	DC Input Voltage		-0.3		3.6	V
V_{CM}	DC Common Mode Input Voltage ^{3,5}		915	1082	1248	mV
V_{REF}	Single-Ended Reference Voltage ^{4,5}			1082		mV
V_{IH}	DC Input HIGH		1275		1620	mV
V_{IL}	DC Input LOW		555		875	mV

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at $V_{DD} = 2.5V, +25^\circ C$ ambient.
3. V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP}) / 2$. Differential mode only.
4. For single-ended operation while in differential mode, A/V_{REF} is tied to the DC voltage V_{REF} .
5. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. The correct input interface table should be referenced.
6. For differential mode ($RxS = LOW$), A and A/V_{REF} must be at the opposite rail.

Differential Input AC Test Conditions for LVEPECL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	732	mV
V_X	Differential Input Signal Crossing Point ²	1082	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t_R, t_F	Input Signal Edge Rate ⁴	1	V/nS

NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A 1082mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

DC Electrical Characteristics Over Operating Range for 2.5V LVTTTL¹

Symbol	Parameter	Test Conditions	Min.	Typ ⁸	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current ¹⁰	$V_{DD} = 2.6V$ $V_I = V_{DDQ}/GND$			± 5	μA
I_{IL}	Input LOW Current ¹⁰	$V_{DD} = 2.6V$ $V_I = GND/V_{DDQ}$			± 5	
V_{IK}	Clamp Diode Voltage	$V_{DD} = 2.4V$, $I_{IN} = -18mA$		- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		-0.3		+3.6	V
Single-Ended Inputs²						
V_{IH}	DC Input HIGH		1.7			V
V_{IL}	DC Input LOW				0.7	V
Differential Inputs						
V_{DIF}	DC Differential Voltage ^{3,9}		0.2			V
V_{CM}	DC Common Mode Input Voltage ^{4,9}		1150	1250	1350	mV
V_{IH}	DC Input HIGH ^{5,6,9}		$V_{REF} + 100$			mV
V_{IL}	DC Input LOW ^{5,7,9}				$V_{REF} - 100$	mV
V_{REF}	Single-Ended Reference Voltage ^{5,9}			1250	-	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	$I_{OH} = -12mA$	$V_{DDQ} - 0.4$			V
		$I_{OH} = -100\mu A$	$V_{DDQ} - 0.1$			V
V_{OL}	Output LOW Voltage	$I_{OL} = 12mA$			0.4	V
		$I_{OL} = 100\mu A$			0.1	V

NOTES:

- See RECOMMENDED OPERATING RANGE table.
- For 2.5V LVTTTL single-ended operation, the RxS pin is tied HIGH and \overline{A}/V_{REF} is tied to GND.
- V_{DIF} specifies the minimum input differential voltage ($V_{TR} - V_{CP}$) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP}) / 2$. Differential mode only.
- For single-ended operation, in differential mode, \overline{A}/V_{REF} is tied to the DC voltage V_{REF} .
- Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- Typical values are at $V_{DD} = 2.5V$, $V_{DDQ} = V_{DD}$, +25°C ambient.
- The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. The correct input interface table should be referenced.
- For differential mode (RxS = LOW), A and \overline{A}/V_{REF} must be at the opposite rail.

Power Supply Characteristics for 2.5V LVTTTL Outputs¹

Symbol	Parameter	Test Conditions ²	Typ	Max	Unit
I _{DDQ}	Quiescent V _{DD} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I _{DDQQ}	Quiescent V _{DDQ} Power Supply Current	V _{DDQ} = Max., Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I _{DDD}	Dynamic V _{DD} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	25	40	μA/MHz
I _{DDQD}	Dynamic V _{DDQ} Power Supply Current per Output	V _{DD} = Max., V _{DDQ} = Max., C _L = 0pF	40	70	μA/MHz
I _{TOT}	Total Power V _{DD} Supply Current	V _{DDQ} = 2.5V, F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	25	40	mA
		V _{DDQ} = 2.5V, F _{REFERENCE CLOCK} = 200MHz, C _L = 15pF	40	70	
I _{TOTQ}	Total Power V _{DDQ} Supply Current	V _{DDQ} = 2.5V, F _{REFERENCE CLOCK} = 100MHz, C _L = 15pF	40	80	mA
		V _{DDQ} = 2.5V, F _{REFERENCE CLOCK} = 200MHz, C _L = 15pF	100	200	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

Differential Input AC Test Conditions for 2.5V LVTTTL

Symbol	Parameter	Value	Units
V _{DIF}	Input Signal Swing ¹	V _{DD}	V
V _X	Differential Input Signal Crossing Point ²	V _{DD} /2	V
V _{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t _R , t _F	Input Signal Edge Rate ⁴	2.5	V/nS

NOTES:

1. A nominal 2.5V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 1.25V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2.5V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

Single-Ended Input AC Test Conditions for 2.5V LVTTTL

Symbol	Parameter	Value	Units
V _{IH}	Input HIGH Voltage	V _{DD}	V
V _{IL}	Input LOW Voltage	0	V
V _{THI}	Input Timing Measurement Reference Level ¹	V _{DD} /2	V
t _R , t _F	Input Signal Edge Rate ²	2	V/nS

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/nS or greater is to be maintained in the 10% to 90% range of the input waveform.

DC Electrical Characteristics Over Operating Range for 1.8V LVTTTL¹

Symbol	Parameter	Test Conditions	Min	Typ ⁸	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current ¹²	$V_{DD} = 2.6V$ $V_I = V_{DDQ}/GND$			± 5	μA
I_{IL}	Input LOW Current ¹²	$V_{DD} = 2.6V$ $V_I = GND/V_{DDQ}$			± 5	
V_{IK}	Clamp Diode Voltage	$V_{DD} = 2.4V$, $I_{IN} = -18mA$		-0.7	-1.2	V
V_{IN}	DC Input Voltage		-0.3		$V_{DDQ} + 0.3$	V
Single-Ended Inputs²						
V_{IH}	DC Input HIGH		1.073 ¹⁰			V
V_{IL}	DC Input LOW				0.683 ¹¹	V
Differential Inputs						
V_{DIF}	DC Differential Voltage ^{3,9}		0.2			V
V_{CM}	DC Common Mode Input Voltage ^{4,9}		825	900	975	mV
V_{IH}	DC Input HIGH ^{5,6,9}		$V_{REF} + 100$			mV
V_{IL}	DC Input LOW ^{5,7,9}				$V_{REF} - 100$	mV
V_{REF}	Single-Ended Reference Voltage ^{5,9}			900		mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	$I_{OH} = -6mA$	$V_{DDQ} - 0.4$			V
		$I_{OH} = -100\mu A$	$V_{DDQ} - 0.1$			V
V_{OL}	Output LOW Voltage	$I_{OL} = 6mA$			0.4	V
		$I_{OL} = 100\mu A$			0.1	V

NOTES:

- See RECOMMENDED OPERATING RANGE table.
- For 1.8V LVTTTL single-ended operation, the RxS pin is allowed to float or tied to $V_{DD}/2$ and \overline{A}/V_{REF} is tied to GND.
- V_{DIF} specifies the minimum input differential voltage ($V_{TR} - V_{CP}$) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
- V_{CM} specifies the maximum allowable range of $(V_{TR} + V_{CP})/2$. Differential mode only.
- For single-ended operation in differential mode, \overline{A}/V_{REF} is tied to the DC voltage V_{REF} . The input is guaranteed to toggle within $\pm 200mV$ of V_{REF} when V_{REF} is constrained within $+600mV$ and $V_{DDI} - 600mV$, where V_{DDI} is the nominal 1.8V power supply of the device driving the A input. To guarantee switching in voltage range specified in the JEDEC 1.8V LVTTTL interface specification, V_{REF} must be maintained at 900mV with appropriate tolerances.
- Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
- Voltage required to maintain a logic LOW, single-ended operation in differential mode.
- Typical values are at $V_{DD} = 2.5V$, $V_{DDQ} = 1.8V$, $+25^\circ C$ ambient.
- The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTTL operation independent of the device output. The correct input interface table should be referenced.
- This value is the worst case minimum V_{IH} over the specification range of the 1.8V power supply. The 1.8V LVTTTL specification is $V_{IH} = 0.65 \cdot V_{DD}$ where V_{DD} is $1.8V \pm 0.15V$. However, the LVTTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value ($V_{IH} = 0.65 \cdot [1.8 - 0.15V]$) rather than reference against a nominal 1.8V supply.
- This value is the worst case maximum V_{IL} over the specification range of the 1.8V power supply. The 1.8V LVTTTL specification is $V_{IL} = 0.35 \cdot V_{DD}$ where V_{DD} is $1.8V \pm 0.15V$. However, the LVTTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value ($V_{IL} = 0.35 \cdot [1.8 + 0.15V]$) rather than reference against a nominal 1.8V supply.
- For differential mode (RxS = LOW), A and \overline{A}/V_{REF} must be at the opposite rail.

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Power Supply Characteristics for 1.8V LVTTTL Outputs¹

Symbol	Parameter	Test Conditions ²	Typ	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current	$V_{DDQ} = \text{Max.}$, Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	20	30	mA
I_{DDQQ}	Quiescent V_{DDQ} Power Supply Current	$V_{DDQ} = \text{Max.}$, Reference Clock = LOW ³ Outputs enabled, All outputs unloaded	0.1	0.3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	$V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $C_L = 0\text{pF}$	20	40	$\mu\text{A}/\text{MHz}$
I_{DDQD}	Dynamic V_{DDQ} Power Supply Current per Output	$V_{DD} = \text{Max.}$, $V_{DDQ} = \text{Max.}$, $C_L = 0\text{pF}$	55	80	$\mu\text{A}/\text{MHz}$
I_{TOT}	Total Power V_{DD} Supply Current	$V_{DDQ} = 1.8\text{V}$, $F_{\text{REFERENCE CLOCK}} = 100\text{MHz}$, $C_L = 15\text{pF}$	25	40	mA
		$V_{DDQ} = 1.8\text{V}$, $F_{\text{REFERENCE CLOCK}} = 200\text{MHz}$, $C_L = 15\text{pF}$	40	60	
I_{TOTQ}	Total Power V_{DDQ} Supply Current	$V_{DDQ} = 1.8\text{V}$, $F_{\text{REFERENCE CLOCK}} = 100\text{MHz}$, $C_L = 15\text{pF}$	55	110	mA
		$V_{DDQ} = 1.8\text{V}$, $F_{\text{REFERENCE CLOCK}} = 200\text{MHz}$, $C_L = 15\text{pF}$	130	260	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.

Differential Input AC Test Conditions for 1.8V LVTTTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing ¹	V_{DDI}	V
V_X	Differential Input Signal Crossing Point ²	$V_{DDI}/2$	mV
V_{THI}	Input Timing Measurement Reference Level ³	Crossing Point	V
t_R, t_F	Input Signal Edge Rate ⁴	1.8	V/nS

NOTES:

1. V_{DDI} is the nominal 1.8V supply ($1.8\text{V} \pm 0.15\text{V}$) of the part or source driving the input. A nominal 1.8V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. Compliant devices must meet the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1.8V/nS or greater is to be maintained in the 20% to 80% range of the input waveform.

Single-Ended Input AC Test Conditions for 1.8V LVTTTL

Symbol	Parameter	Value	Units
V_{IH}	Input HIGH Voltage ¹	V_{DDI}	V
V_{IL}	Input LOW Voltage	0	V
V_{THI}	Input Timing Measurement Reference Level ²	$V_{DDI}/2$	mV
t_R, t_F	Input Signal Edge Rate ³	2	V/nS

NOTES:

1. V_{DDI} is the nominal 1.8V supply ($1.8\text{V} \pm 0.15\text{V}$) of the part or source driving the input.
2. A nominal 900mV timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
3. The input signal edge rate of 2V/nS or greater is to be maintained in the 10% to 90% range of the input waveform.

AC Electrical Characteristics Over Operating Range⁷

Symbol	Parameter	Min	Typ	Max	Unit
Skew Parameters					
$t_{SK(O)}$	Same Device Output Pin-to-Pin Skew ¹	Single-Ended and Differential Modes		25	pS
		Single-Ended in Differential Mode (DSE)		25	
$t_{SK(P)}^2$	Pulse Skew ³	Single-Ended and Differential Modes		300	pS
		Single-Ended in Differential Mode (DSE)		300	
$t_{SK(P)}^4$	Pulse Skew ³	Single-Ended and Differential Modes		350	pS
		Single-Ended in Differential Mode (DSE)		350	
d_T^5	Duty Cycle	40		60	%
$t_{SK(PP)}$	Part-to-Part Skew ⁶	Single-Ended and Differential Modes		300	pS
		Single-Ended in Differential Mode (DSE)		300	
Propagation Delay					
t_{PLH} t_{PHL}	Propagation Delay A to Qn			2.5	nS
t_R	Output Rise Time (20% to 80%)	2.5V/1.8V LVTTTL Outputs	350	1050	pS
		HSTL / eHSTL Outputs	350	1350	
t_F	Output Fall Time (20% to 80%)	2.5V/1.8V LVTTTL Outputs	350	1050	pS
		HSTL / eHSTL Outputs	350	1350	
f_O	Frequency Range (HSTL/eHSTL outputs)			250	MHz
	Frequency Range (2.5V/1.8V LVTTTL outputs)			200	
Output Gate Enable/Disable Delay					
t_{PGE}	Output Gate Enable to Qn			3.5	nS
t_{PGD}	Output Gate Enable to Qn Driven to GL Designated Level			3	nS

NOTES:

1. Skew measured between all outputs under identical input and output interfaces, transitions, and load conditions on any one device.
2. For 1.8V LVTTTL and eHSTL outputs only.
3. Skew measured is difference between propagation times t_{PLH} and t_{PHL} of any output under identical input and output interfaces, transitions, and load conditions on any one device.
4. For 2.5V LVTTTL outputs only.
5. For HSTL outputs only.
6. Skew measured is the magnitude of the difference in propagation times between any outputs of two devices, given identical transitions and load conditions at identical V_{DD}/V_{DDQ} levels and temperature.
7. Guaranteed by design.

AC Differential Input Specifications¹

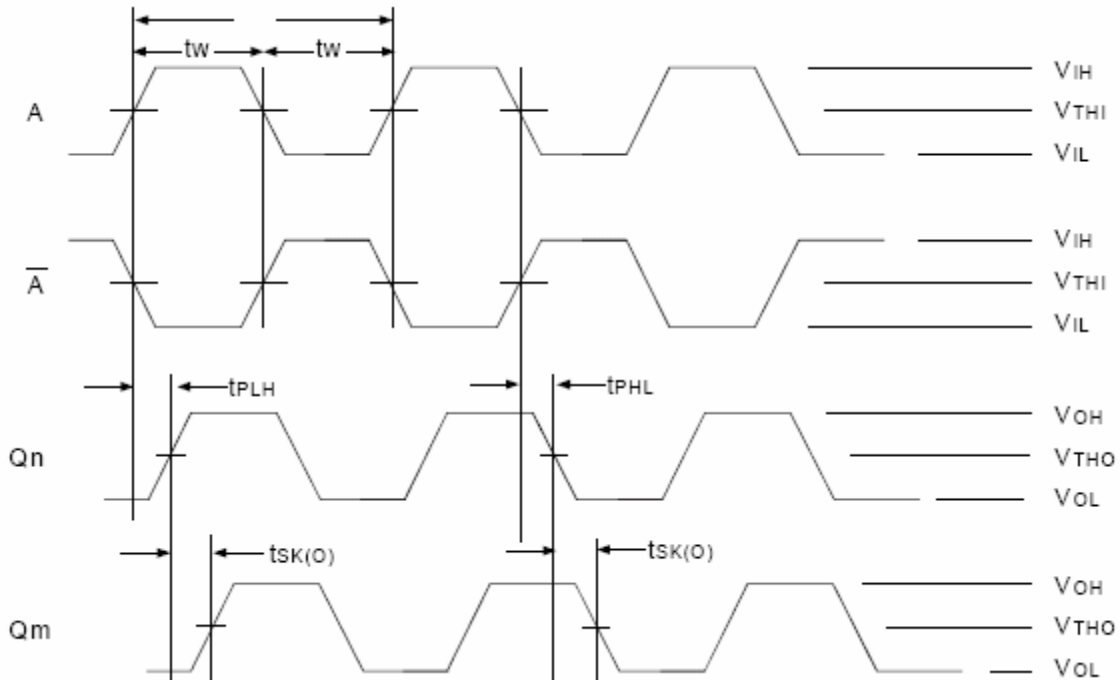
Symbol	Parameter	Min	Typ	Max	Unit
t_w	Reference Clock Pulse Width HIGH or LOW (HSTL/eHSTL outputs) ²	1.73			nS
	Reference Clock Pulse Width HIGH or LOW (2.5V / 1.8V LVTTTL outputs) ²	2.17			
HSTL/eHSTL/1.8V LVTTTL/2.5V LVTTTL					
V_{DIF}	AC Differential Voltage ³	400			mV
V_{IH}	AC Input HIGH ^{4,5}	$V_x + 200$			mV
V_{IL}	AC Input LOW ^{4,6}			$V_x - 200$	mV
LVEPECL					
V_{DIF}	AC Differential Voltage ³	400			mV
V_{IH}	AC Input HIGH ⁴	1275			mV
V_{IL}	AC Input LOW ⁴			875	mV

NOTES:

- For differential input mode, RxS is tied to GND.
- Both differential input signals should not be driven to the same level simultaneously. The input will not change state until the inputs have crossed and the voltage range defined by V_{DIF} has been met or exceeded.
- Differential mode only. V_{DIF} specifies the minimum input voltage ($V_{TR} - V_{CP}$) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.
- For single-ended operation, A/V_{REF} is tied to DC voltage (V_{REF}). Refer to each input interface's DC specification for the correct V_{REF} range.
- Voltage required to switch to a logic HIGH, single-ended operation only.
- Voltage required to switch to a logic LOW, single-ended operation only.

PRELIMINARY

AC Timing Waveforms



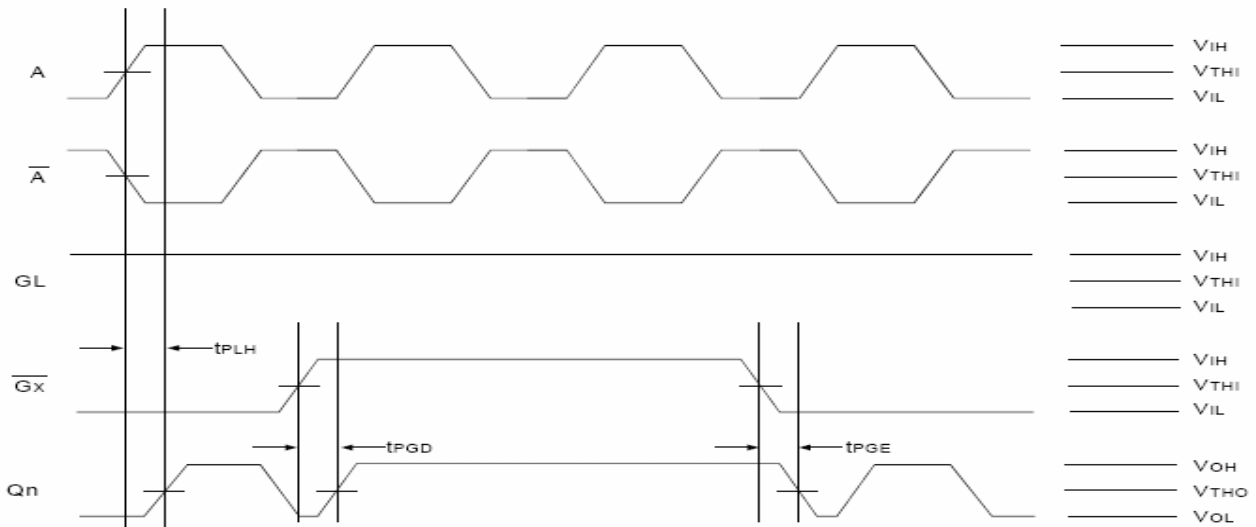
Propagation and Skew Waveforms

NOTES:

1. t_{PHL} and t_{PLH} signals are measured from the input passing through V_{THI} or input pair crossing to Qn passing through V_{THO} .
2. Pulse Skew is calculated using the following expression:

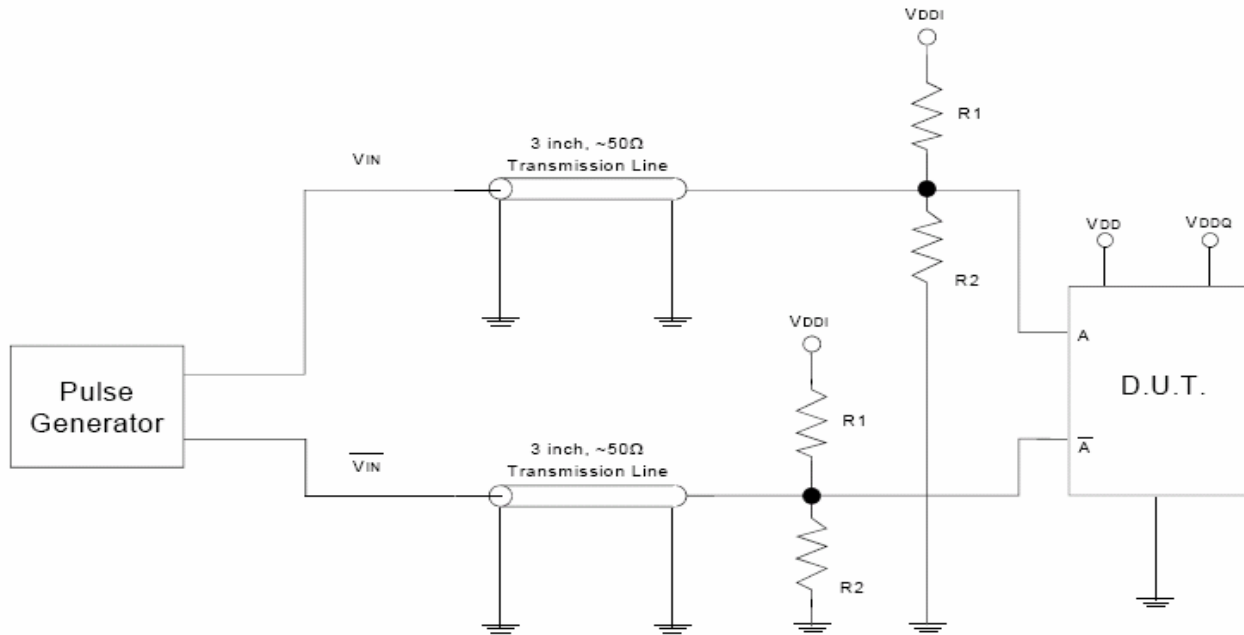
$$t_{SK(P)} = |t_{PHL} - t_{PLH}|$$

where t_{PHL} and t_{PLH} are measured on the controlled edges of any one output from rising and falling edges of a single pulse. Please note that the t_{PHL} and t_{PLH} shown are not valid measurements for this calculation because they are not taken from the same pulse.



Gate Disable/Enable Showing Runt Pulse Generation

Test Circuits and Conditions



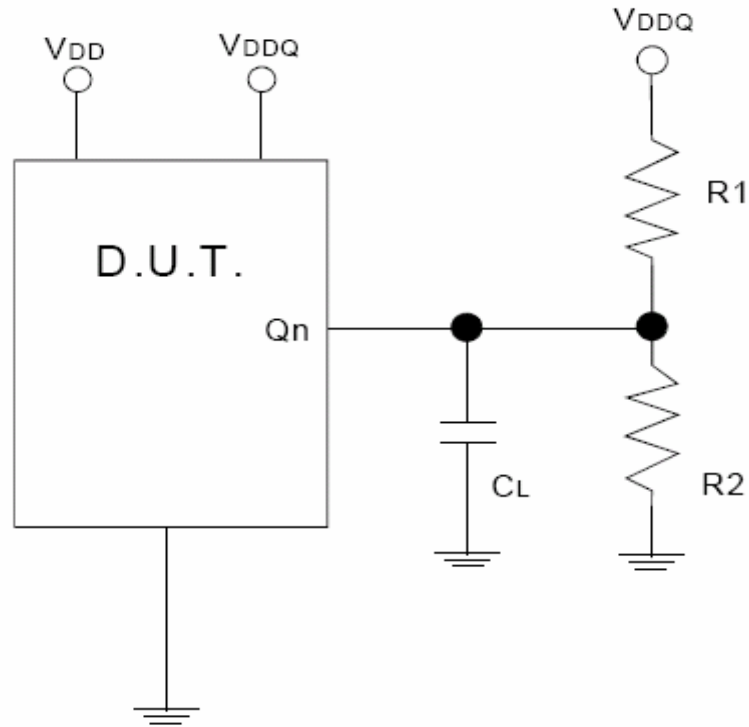
Test Circuit for Differential Input¹

Differential Input Test Conditions

Symbol	$V_{DD} = 2.5V \pm 0.1V$	Unit
R1	100	Ω
R2	100	Ω
V_{DDI}	$V_{CM} * 2$	V
V_{THI}	HSTL: Crossing of A and A eHSTL: Crossing of A and A LVEPECL: Crossing of A and A 1.8V LVTTTL: $V_{DDI}/2$ 2.5V LVTTTL: $V_{DD}/2$	V

NOTE:

1. This input configuration is used for all input interfaces. For single-ended testing, the \overline{V}_{IN} input is tied to GND. For testing single-ended in differential input mode, the \overline{V}_{IN} is left floating.

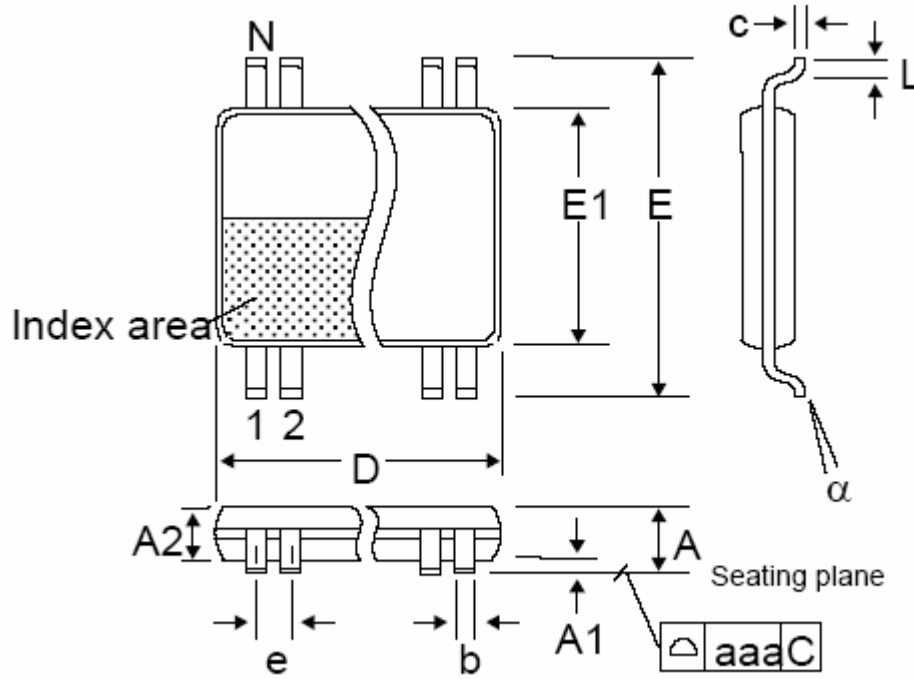


Test Circuit for SDR Outputs

SDR Output Test Conditions

Symbol	$V_{DD} = 2.5V \pm 0.1V$ $V_{DDQ} = \text{Interface Specified}$	Unit
C_L	15	pF
R1	100	Ω
R2	100	Ω
V_{TH0}	$V_{DDQ} / 2$	V

48-lead TSSOP Package (6.10 mm Body, JEDEC MO-153-ED)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.047	...	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.8	1.05
b	0.008 BSC		0.20 BSC	
c	0.004	0.008	0.09	0.20
D	0.488	0.496	12.40	12.60
E1	0.236	0.244	6.00	6.20
E	0.319 BSC		8.10 BSC	
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
N	48			
α	0°	8°	0°	8°

September 2006

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Ordering code

Part Number	Marking	Package Type	Operating Range
PCS2P5T907AG-48TT	2P5T907AG	48 Pin TSSOP, Tube, Pb Free	Commercial
PCS2P5T907AG-48TR	2P5T907AG	48 Pin TSSOP, Tape and Reel, Pb Free	Commercial
PCS2I5T907AG-48TT	2I5T907AG	48 Pin TSSOP, TUBE, Pb Free	Industrial
PCS2I5T907AG-48TR	2I5T907AG	48 Pin TSSOP, Tape and Reel, Pb Free	Industrial

Ordering Information

PCS2P5T907AG-48TR

OR – TSOT23 -6,T/R TT – TSSOP, TUBE TR – TSSOP, T/R VT – TVSOP, TUBE VR – TVSOP, T/R ST – SOIC, TUBE AR – SSOP, T/R AT – SSOP, TUBE	SR – SOIC, T/R QR – QFN, T/R QT – QFN, TRAY BT – BGA, TRAY BR – BGA, T/R UR – SOT-23, T/R DR – QSOP, T/R DT – QSOP, TUBE
PIN COUNT	
G = GREEN PACKAGE, LEAD FREE, and RoHS	
PART NUMBER	
X = Automotive (-40C to +125C) I = Industrial (-40C to +85C) P or n/c = Commercial (0C to +70C)	
1 – reserved 2 – Non PLL based 3 – EMI Reduction 4 – DDR support products 5 – STD Zero Delay Buffer	6 – power management 7 – power management 8 – power management 9 – Hi performance 0 - reserved
PULSECORE Semiconductor Mixed Signal Product	

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



PulseCore Semiconductor Corporation
1715 S. Bascom Ave Suite 200
Campbell, CA 95008
Tel: 408-879-9077
Fax: 408-879-9018
www.pulsecoresemi.com

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Preliminary Information
Part Number: PCS2P5T907A
Document Version: 0.2

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003

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