

DATA SHEET

74F258A

Quad 2-line to 1-line selector/multiplexer,
inverting (3-State)

Product specification

1996 Jan 05

IC15 Data Handbook

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

74F258A

FEATURES

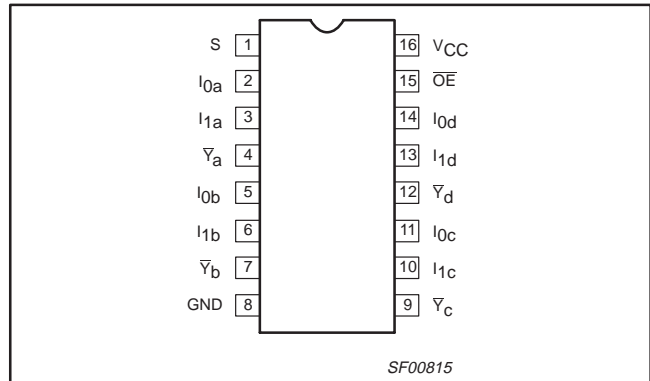
- Multifunction capability
- Non-inverting data path
- 3-State outputs
- See 74F257A for non-inverting version

DESCRIPTION

The 74F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the Output Enable input (\overline{OE}) is High. All but one device must be in the High impedance state to avoid currents that would exceed the maximum ratings if outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

The 74F258A is the logical implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a High impedance "off" state when the Output Enable input (\overline{OE}) is High. All but one device must be in the High impedance state to avoid currents that would exceed the maximum ratings if outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258A	3.5ns	14mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG. DWG. #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
16-pin plastic DIP	N74F258AN	SOT38-4
16-pin plastic SO	N74F258AD	SOT109-1

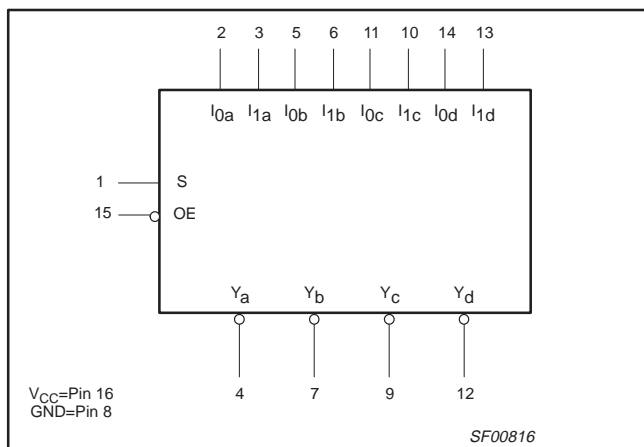
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20 μ A/0.6mA
S	Common select input	1.0/1.0	20 μ A/0.6mA
\overline{OE}	Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
$\overline{Y}_a - \overline{Y}_d$	Data outputs	150/40	3.0mA/24mA

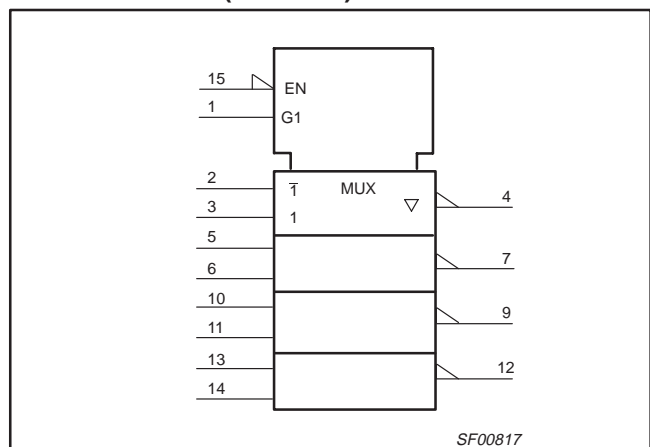
NOTE:

One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



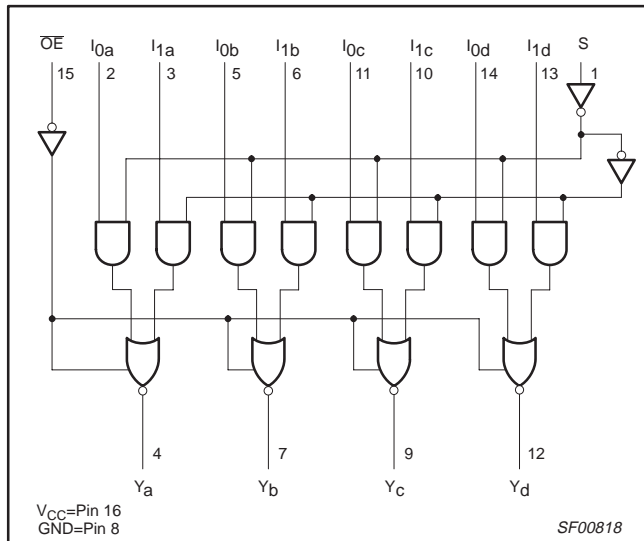
LOGIC SYMBOL (IEEE/IEC)



Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
\overline{OE}	S	I ₀	I ₁	Y
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	48	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-3	mA
I _{OL}	Low-level output current			24	mA
T _{amb}	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT	
				MIN	TYP ²	MAX		
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}	2.4			V	
			±5%V _{CC}	2.7	3.3		V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.30	0.50	V	
			±5%V _{CC}		0.35	0.50	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}		-0.73	-1.2		V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			100		μA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V			20		μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V			-0.6		mA	
I _{OZH}	Off-state output current, High-level voltage applied	V _{CC} = MAX, V _O = 2.7V			50		μA	
I _{OZL}	Off-state output current, High-level voltage applied	V _{CC} = MAX, V _O = 0.5V			-50		μA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-60		-150	mA	
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX	I _{1n} =4.5V, \overline{OE} =I _{0n} =S=GND		8.5	11.5	mA
		I _{CCL}		I _{1n} =S=4.5V, \overline{OE} =I _{0n} =GND		17	23	mA
		I _{CCZ}		I _{1n} = \overline{OE} =4.5V, I _{0n} =S=GND		16	22	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

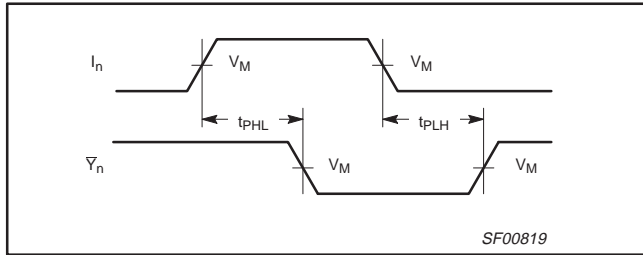
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = -55°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay I _n to \overline{Y}_n	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns ns
t _{PLH} t _{PHL}	Propagation delay S to \overline{Y}_n	Waveform 2	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	9.0 9.0	ns ns
t _{PZH} t _{PZL}	Output enable time to High or Low level	Waveform 3	4.0	6.0	7.5	3.5	8.5	ns
		Waveform 4	4.0	5.5	7.5	3.5	8.5	ns
t _{PHZ} t _{PLZ}	Output disable time from High or Low level	Waveform 3	2.0	3.5	5.5	2.0	6.5	ns
		Waveform 4	2.0	3.5	5.5	2.0	6.0	ns

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

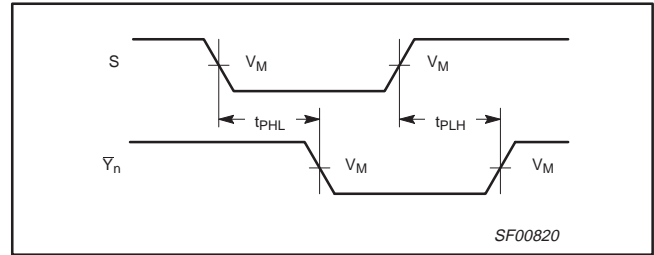
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AC WAVEFORMS

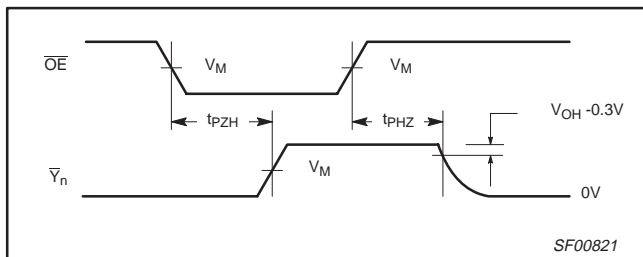
For all waveforms, $V_M = 1.5V$.



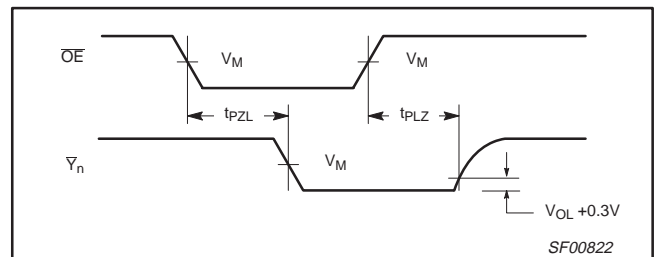
Waveform 1. Propagation Delay Data and Select to Output



Waveform 2. Propagation Delay Select to Output



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{pLZ}	closed
t_{pZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

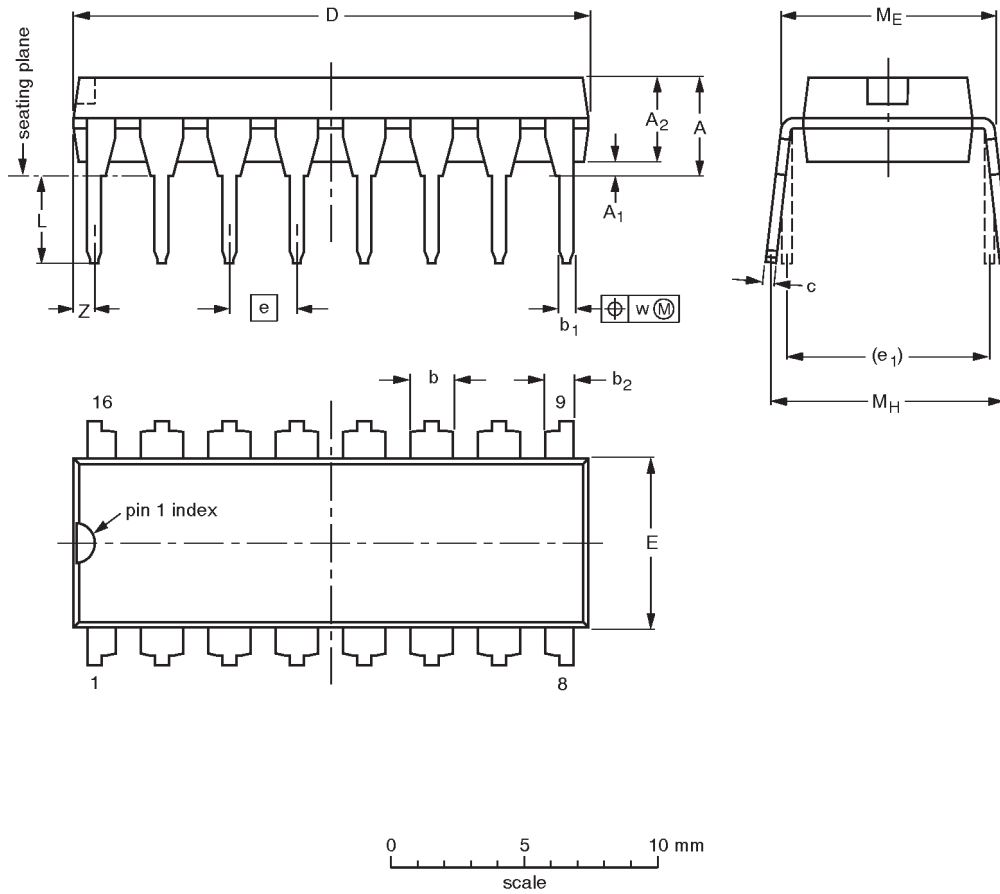
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Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

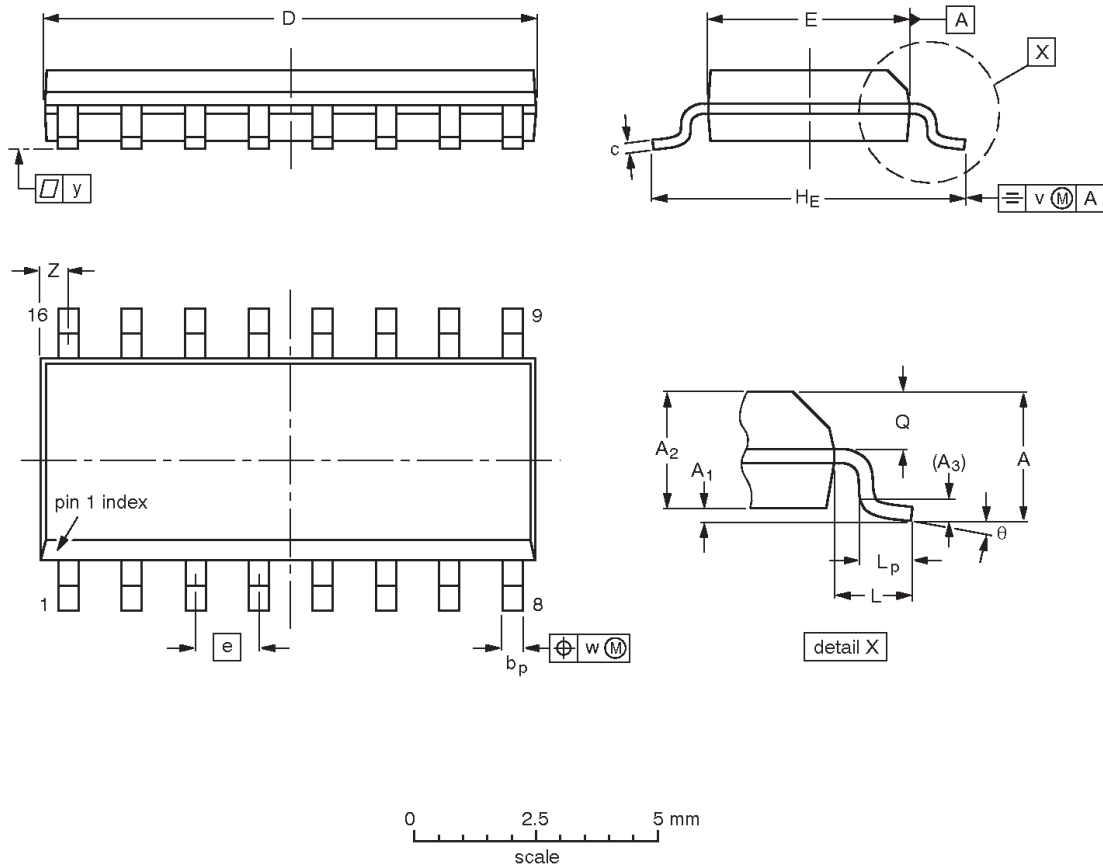
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

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DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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