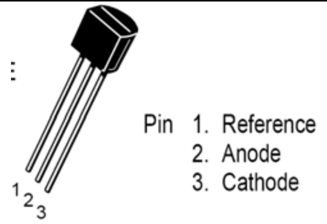
Programmable Precision Reference

TL431Z

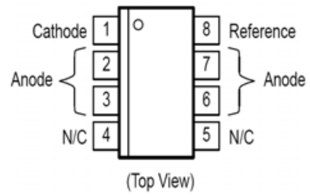
Description

The TL431Z is a three-terminal adjustable regulator series with a guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between Vref (approximately 2.5 volts) and 40 volts with two external resistors. These devices have a typical dynamic output impedance of 0.2Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacement for zener diodes in many applications.The TL431Z is characterized for operation from -25°C to +85°C.

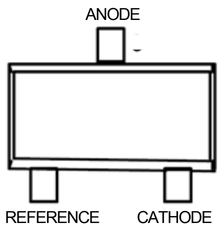
Pin Connections



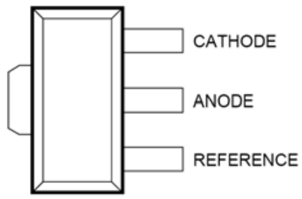
TO-92



SOP-8



SOT-23



SOT-89

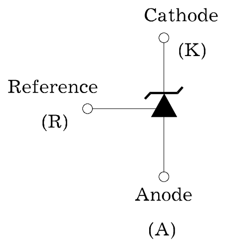
Features

- Programmable Output Voltage to 40V
- Low Dynamic Output Impedance 0.2Ω
- Sink Current Capability of 0.1 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- Fast Turn on Response
- TO-92, SOP- 8, SOT-23, SOT-89 packages

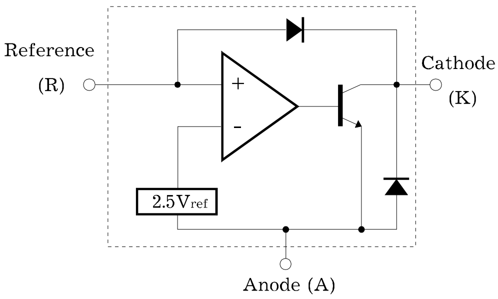
Ordering Information

Product Number	Reference Input Voltage	Package
TL431ZCLF TL431ZCLS	0.5%	TO-92
TL431ZCD		8-SOP
TL431ZCS		SOT-23
TL431ZCP		SOT-89
TL431ZALF TL431ZALS	1%	TO-92
TL431ZAD		8-SOP
TL431ZAS		SOT-23
TL431ZAP		SOT-89
TL431ZLF TL431ZLS	2%	TO-92
TL431ZD		8-SOP
TL431ZS		SOT-23
TL431ZP		SOT-89

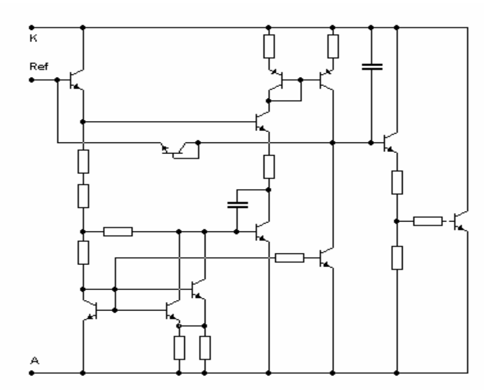
Symbol



Functional Block Diagram



Equivalent Schematic



ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified)

Characteristic	Symbol	Value	Unit
Cathode Voltage	V_{KA}	44	V
Cathode Current Range (Continuous)	I_K	-100 ~ 150	mA
Reference Input Current Range	I_{REF}	0.05 ~ 10	mA
Power Dissipation at 25°C: SOP, TO – 92 Package ($R_{\theta JA}$ = 178°C/W) SOT Package ($R_{\theta JA}$ = 625°C/W)	P_D	 0.7 0.2	 W W
Junction Temperature Range	T_J	-25 ~ 150	°C
Operating Temperature Range	T_g	-25 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{REF}		40	V
Cathode Current	I_K	0.5		100	mA

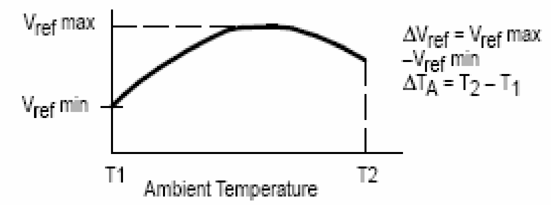
ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{KA} = V_{REF}, I_K = 10mA unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Input Voltage	V_{REF}	$V_{KA} = V_{REF}$, I_K = 10mA				
		TL431Z (2%)	2.440	2.495	2.550	
		TL431Z-A (1%)	2.470	2.495	2.520	V
		TL431Z-C (0.5%)	2.482	2.495	2.508	
Deviation of Reference Input Voltage Over Full Temperature Range	$V_{REF(dev)}$	$T_{min} \le Ta \le T_{max}$		3	17	MV
Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	ΔV_{KA} = 10V-V_{REF}		-1.4	-2.7	mV/V
		ΔV_{KA} = 36V- 10V		-1.0	-2.0	
Reference Input Current	I_{REF}	R_1 = 10KΩ, $R_2 = \infty$		1.8	4	μA
Deviation of Reference Input Current Over Full Temperature Range	$I_{REF(dev)}$	R_1 = 10KΩ, $R_2 = \infty$		0.4	1.2	μA
Minimum Cathode Current for Regulation	$I_{K(min)}$			0.25	0.5	mA
Off-State Cathode Current	$I_{K(off)}$	V_{KA} = 40 V, V_{REF} = 0		0.17	0.9	μA
Dynamic Impedance	Z_{KA}	I_K = 10mA to 100 mA , f ≤ 1.0KHz		0.27	0.5	Ω

Note :

1. The deviation parameter ΔVref is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies



The average temperature coefficient of the reference input voltage, aVref is defined as:

$$V_{ref}\ \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref}\ @\ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\ (V_{ref}\ @\ 25°C)}$$

αVref can be positive or negative depending on whether Vref Min or Vref Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C $\qquad \alpha\ V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8$ ppm/°C

2. The dynamic impedance ZKA is defined as

$$|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2}\right)$$

TEST CIRCUITS

Fig.1. Test Circuit for $V_{KA} = V_{REF}$

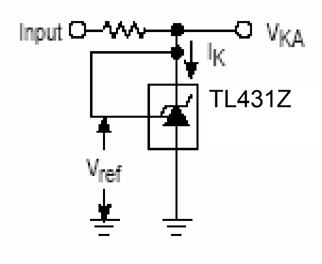


Fig.2. Test Circuit for $V_{KA} \geq V_{REF}$

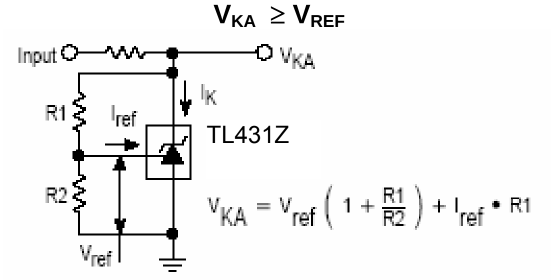


Fig.3. Test Circuit for I_{off}

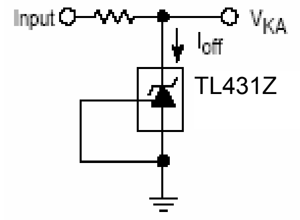


Figure 4. Cathode Current versus Cathode Voltage

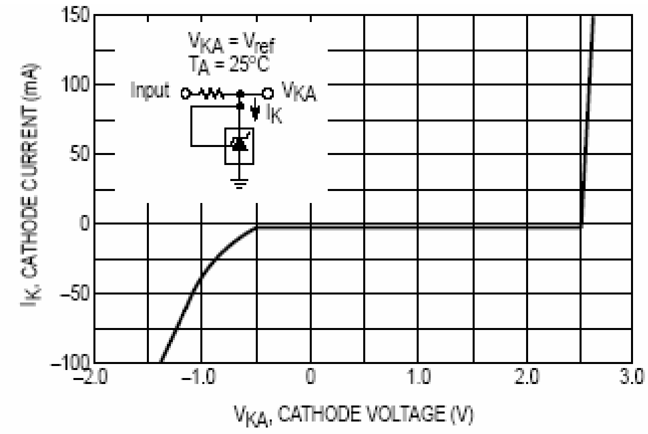


Figure 5. Cathode Current versus Cathode Voltage

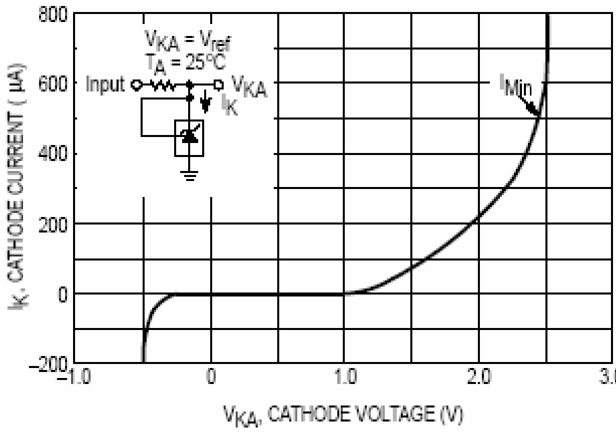


Figure 6. Reference Input Voltage versus Ambient Temperature

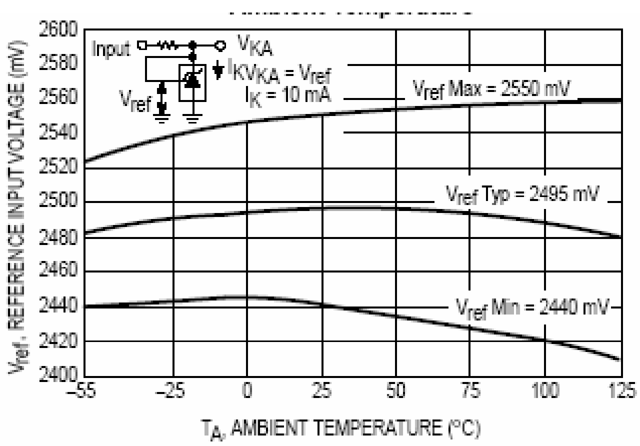


Figure 7. Reference Input Current versus Ambient Temperature

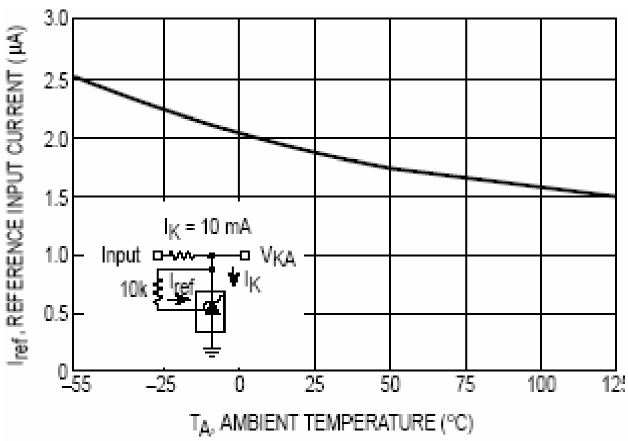


Figure 8. Change in Reference Input Voltage versus Cathode Voltage

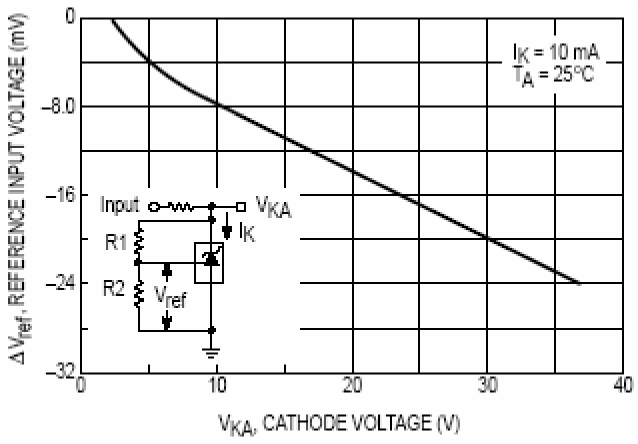


Figure 9. Off–State Cathode Current versus Ambient Temperature

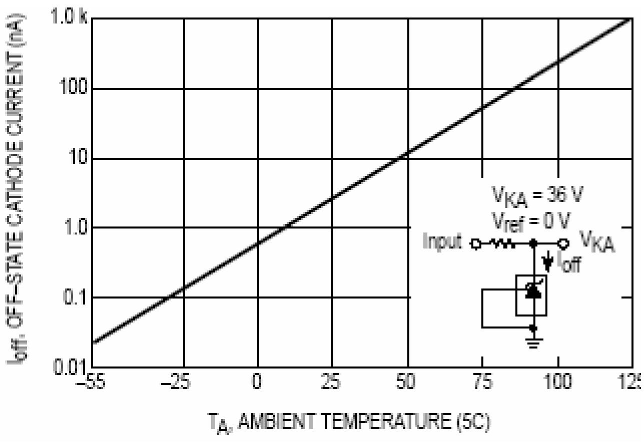


Figure 10. Dynamic Impedance versus Frequency

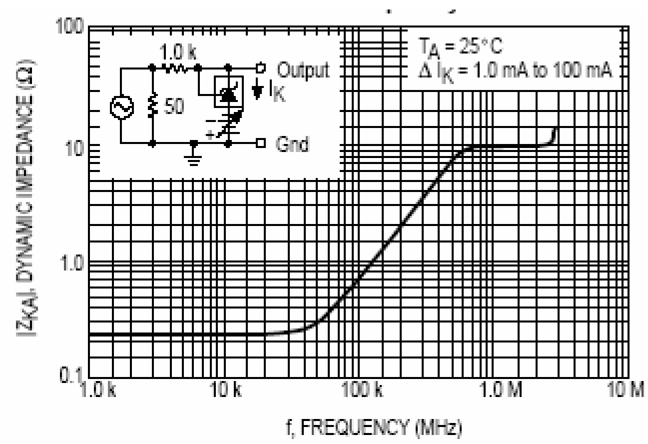


Figure 11. Dynamic Impedance versus Ambient Temperature

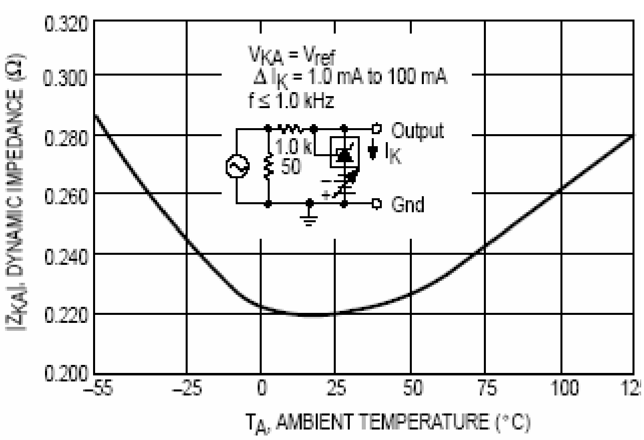


Figure 12. Open–Loop Voltage Gain versus Frequency

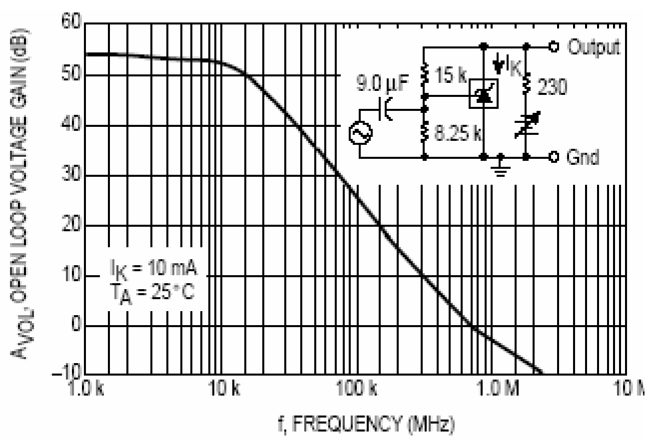


Figure 13. Spectral Noise Density

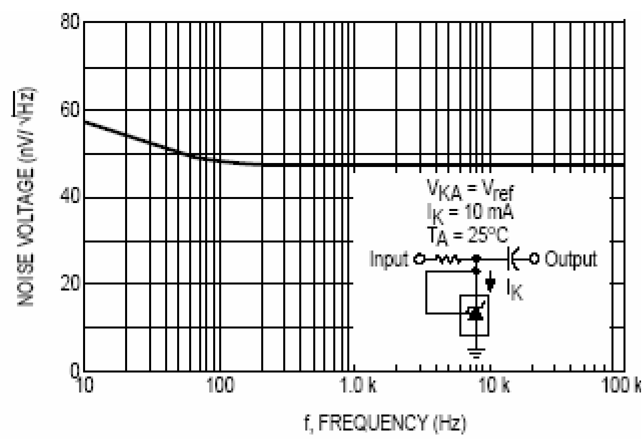


Figure 14. Pulse Response

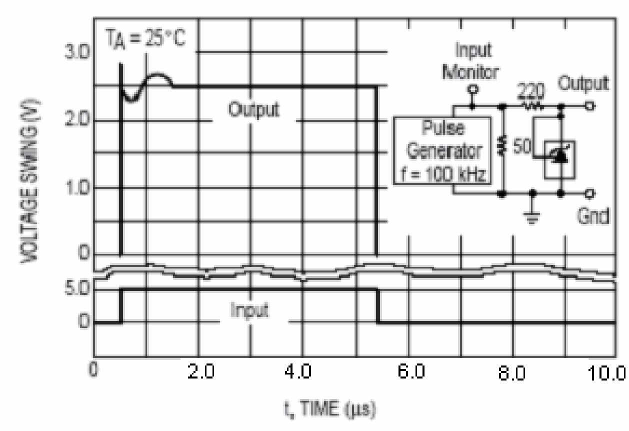


Figure 15. Stability Boundary Conditions

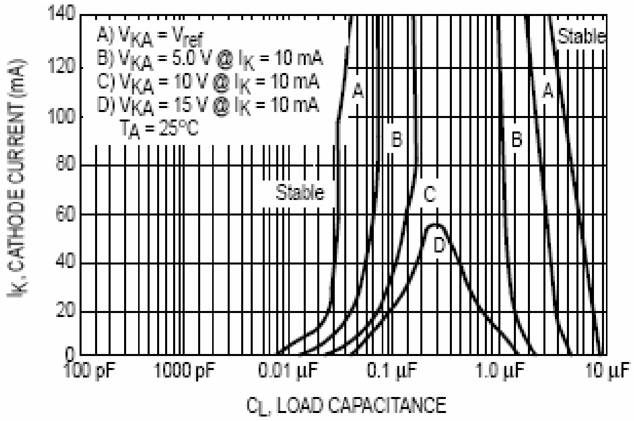


Figure 16. Test Circuit For Curve A of Stability Boundary Conditions

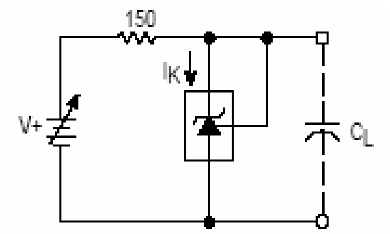
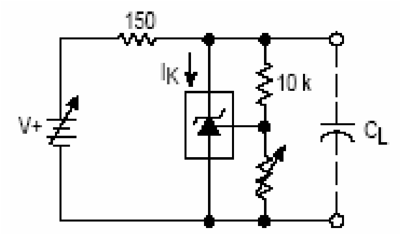
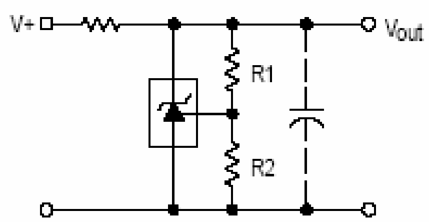


Figure 17. Test Circuit For Curves B, C, And D of Stability Boundary Conditions



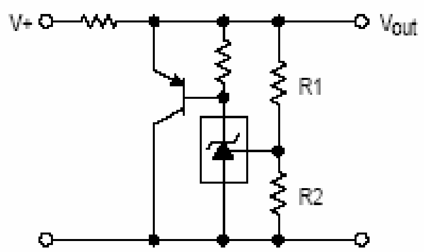
TYPICAL APPLICATIONS

Figure 18. Shunt Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 19. High Current Shunt Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 20. Output Control for a Three–Terminal Fixed Regulator

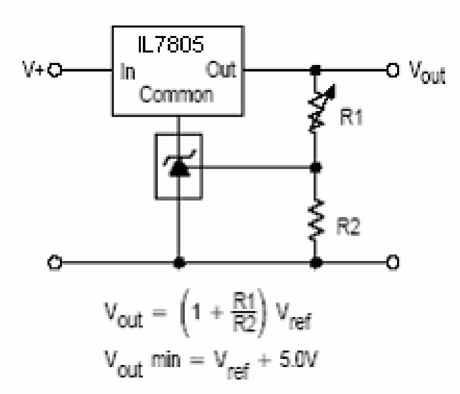


Figure 21. Series Pass Regulator

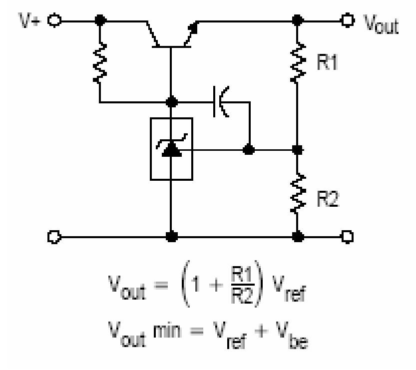


Figure 22. Constant Current Source

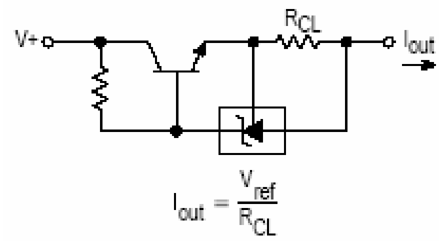


Figure 23. Constant Current Sink

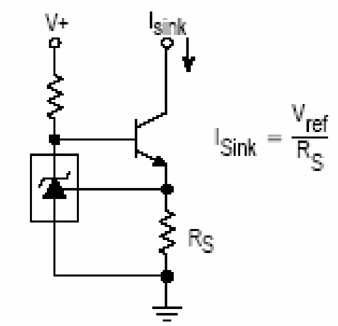


Figure 24. TRIAC Crowbar

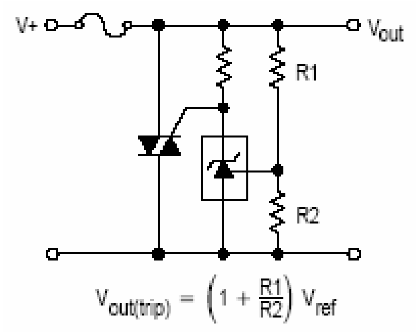


Figure 25. SRC Crowbar

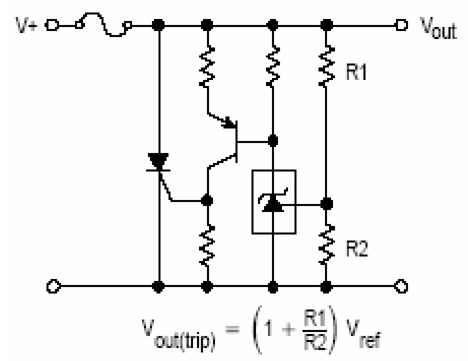


Figure 26. Voltage Monitor

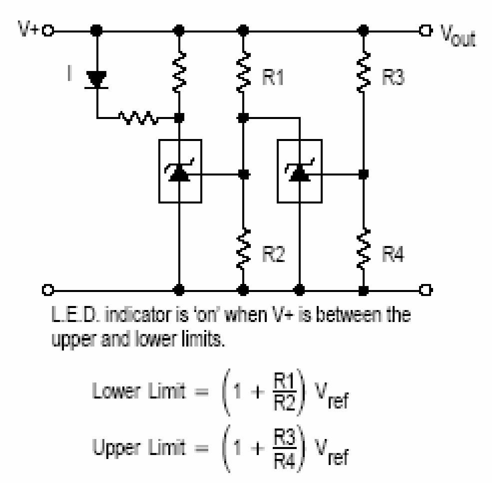


Figure 27. Single–Supply Comparator with Temperature–Compensated Threshold

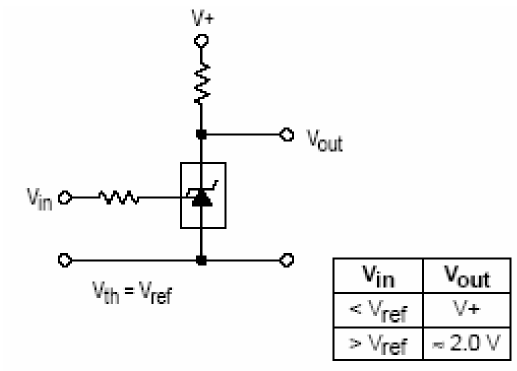


Figure 28. Linear Ohmmeter

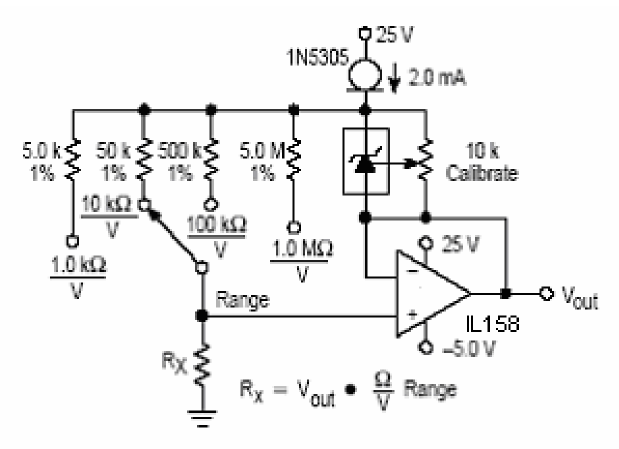


Figure 29. Simple 400 mW Phono Amplifier

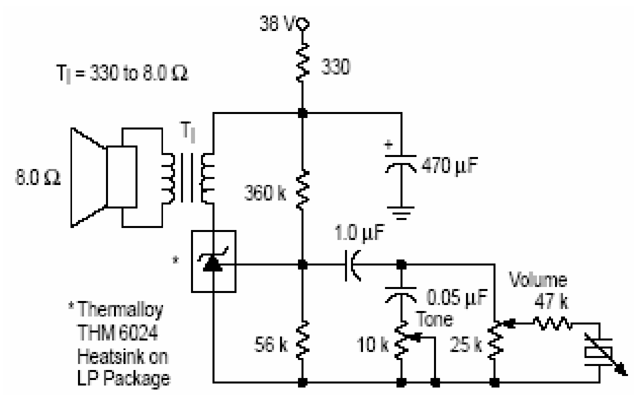
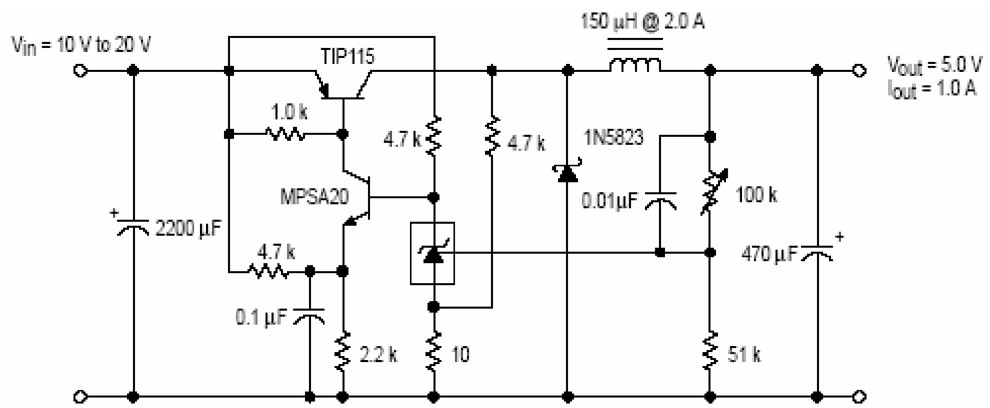


Figure 30. High Efficiency Step–Down Switching Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 20 V, I_o = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_o = 0 A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_o = 1.0 A	50 mVpp P.A.R.D.
Output Ripple	V_{in} = 20 V, I_o = 1.0 A	100 mVpp P.A.R.D.
Efficiency	V_{in} = 15 V, I_o = 1.0 A	82%

APPLICATIONS INFORMATION

The TL431Z is a programmable precision reference which is used in a variety of ways. It serves as a reference voltage in circuits where a non–standard reference voltage is needed. Other uses include feedback control for driving an optocoupler in power supplies, voltage monitor, constant current source, constant current sink and series pass regulator. In each of these applications, it is critical to maintain stability of the device at various operating currents and load capacitances. In some cases the circuit designer can estimate the stabilization capacitance from the stability boundary conditions curve provided in Figure 15. However, these typical curves only provide stability information at specific cathode voltages and at a specific load condition.

Additional information is needed to determine the capacitance needed to optimize phase margin or allow for process variation. A simplified model of the TL431Z is shown in Figure 31. When tested for stability boundaries, the load resistance is 150 Ω. The model reference input consists of an input transistor and a dc emitter resistance connected to the device anode. A dependent current source, Gm, develops a current whose amplitude is determined by the difference between the 1.78 V internal reference voltage source and the input transistor emitter voltage. A portion of Gm flows through compensation capacitance, C_{P2}. The voltage across C_{P2} drives the output dependent current source, Go, which is connected across the device cathode and anode.

Model component values are:
Vref = 1.78 V
Gm = 0.3 + 2.7 exp ($-I_C$/26 mA)
where I_C is the device cathode current and Gm is in mhos
Go = 1.25 (Vcp^2) μmhos.

Resistor and capacitor typical values are shown on the model. Process tolerances are ±20% for resistors, ±10% for capacitors, and ±40% for transconductances.

An examination of the device model reveals the location of circuit poles and zeroes:

$$P1 = \frac{1}{2\pi\ R_{GM}\ C_{P1}} = \frac{1}{2\pi * 1.0\ M * 20\ pF} = 7.96\ kHz$$

$$P2 = \frac{1}{2\pi\ R_{P2} C_{P2}} = \frac{1}{2\pi * 10\ M * 0.265\ pF} = 60\ kHz$$

$$Z1 = \frac{1}{2\pi\ R_{Z1} C_{P1}} = \frac{1}{2\pi * 15.9\ k * 20\ pF} = 500\ kHz$$

In addition, there is an external circuit pole defined by the load:

$$P_L = \frac{1}{2\pi\ R_L C_L}$$

Also, the transfer dc voltage gain of the TL431Z is:

$$G = G_M R_{GM} Go R_L$$

Example 1:

$I_C = 10$ mA, $R_L = 230\ \Omega$, $C_L = 0$. Define the transfer gain.

The DC gain is:

$$G = G_M R_{GM} Go R_L =$$

$$(2.138)(1.0\ M)(1.25\ \mu)(230) = 615 = 56\ dB$$

$$\text{Loop gain} = G\,\frac{8.25\ k}{8.25\ k + 15\ k} = 218 = 47\ dB$$

The resulting transfer function Bode plot is shown in Figure 32. The asymptotic plot may be expressed as the following equation:

$$Av = 615\,\frac{\left(1 + \frac{jf}{500\ kHz}\right)}{\left(1 + \frac{jf}{8.0\ kHz}\right)\left(1 + \frac{jf}{60\ kHz}\right)}$$

The Bode plot shows a unity gain crossover frequency of approximately 600 kHz. The phase margin, calculated from the equation, would be 55.9 degrees. This model matches the Open–Loop Bode Plot of Figure 12. The total loop would have a unity gain frequency of about 300 kHz with a phase margin of about 44 degrees.

Figure 31. Simplified TL431Z Device Model

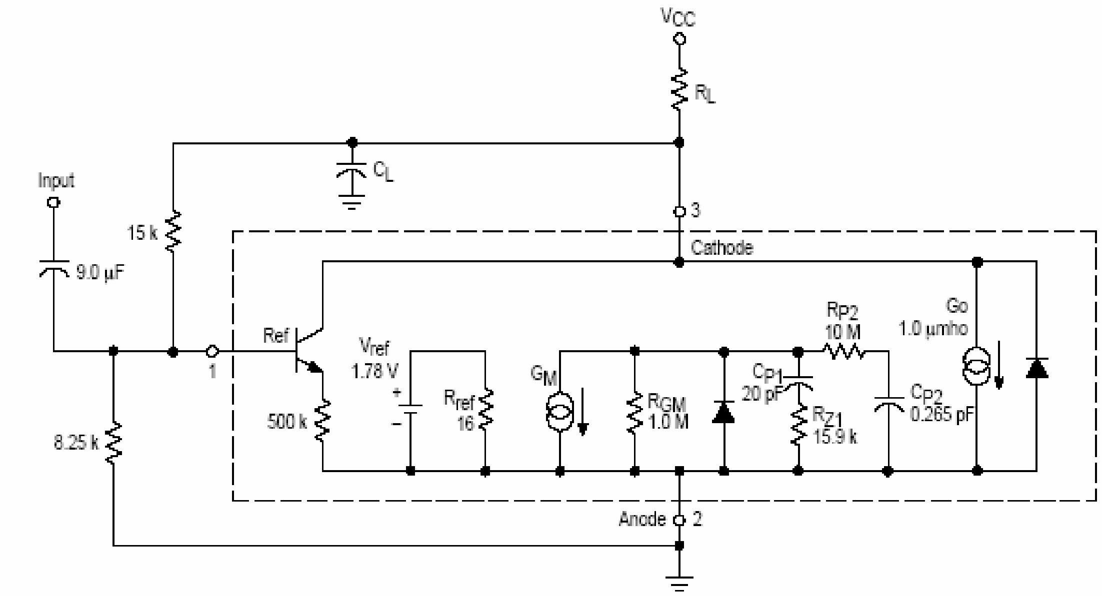


Figure 32. Example 1 Circuit Open Loop Gain Plot

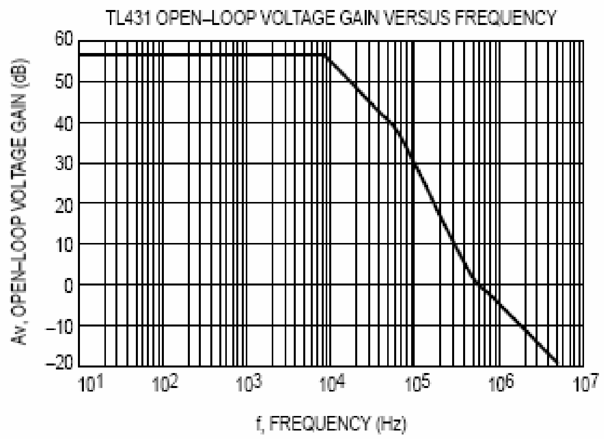
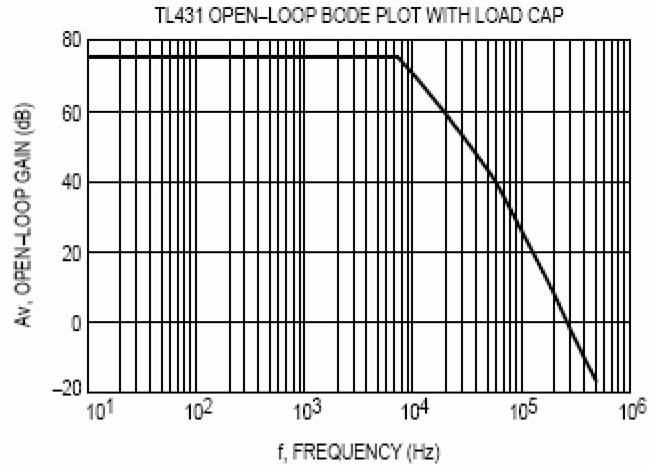


Figure 33. Example 2 Circuit Open Loop Gain Plot



Example 2.
I_C = 7.5 mA, R_L = 2.2 kΩ, C_L = 0.01 µF.
Cathode tied to reference input pin. An examination of the data sheet stability boundary curve (Figure 15) shows that this value of load capacitance and cathode current is on the boundary. Define the transfer gain.
The DC gain is:

$G = G_M R_{GM} Go R_L =$
(2.323)(1.0 M)(1.25 µ)(2200) = 6389 = 76 dB

The resulting open loop Bode plot is shown in Figure 33. The asymptotic plot may be expressed as the following equation:

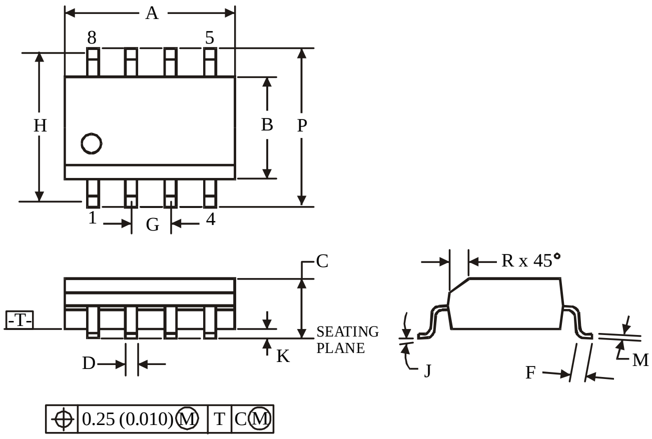
$$Av = 615 \frac{\left(\frac{1 + jf}{500\ kHz}\right)}{\left(\frac{1 + jf}{8.0\ kHz}\right)\left(\frac{1 + jf}{60\ kHz}\right)\left(\frac{1 + jf}{7.2\ kHz}\right)}$$

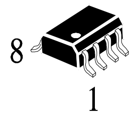
Note that the transfer function now has an extra pole formed by the load capacitance and load resistance.
Note that the crossover frequency in this case is about 250 kHz, having a phase margin of about –46 degrees. Therefore, instability of this circuit is likely.

With three poles, this system is unstable. The only hope for stabilizing this circuit is to add a zero. However, that can only be done by adding a series resistance to the output capacitance, which will reduce its effectiveness as a noise filter. Therefore, practically, in reference voltage applications, the best solution appears to be to use a smaller value of capacitance in low noise applications or a very large value to provide noise filtering and a dominant pole rolloff of the system.

Package Dimensions

D SUFFIX SOIC
(MS - 012AA)



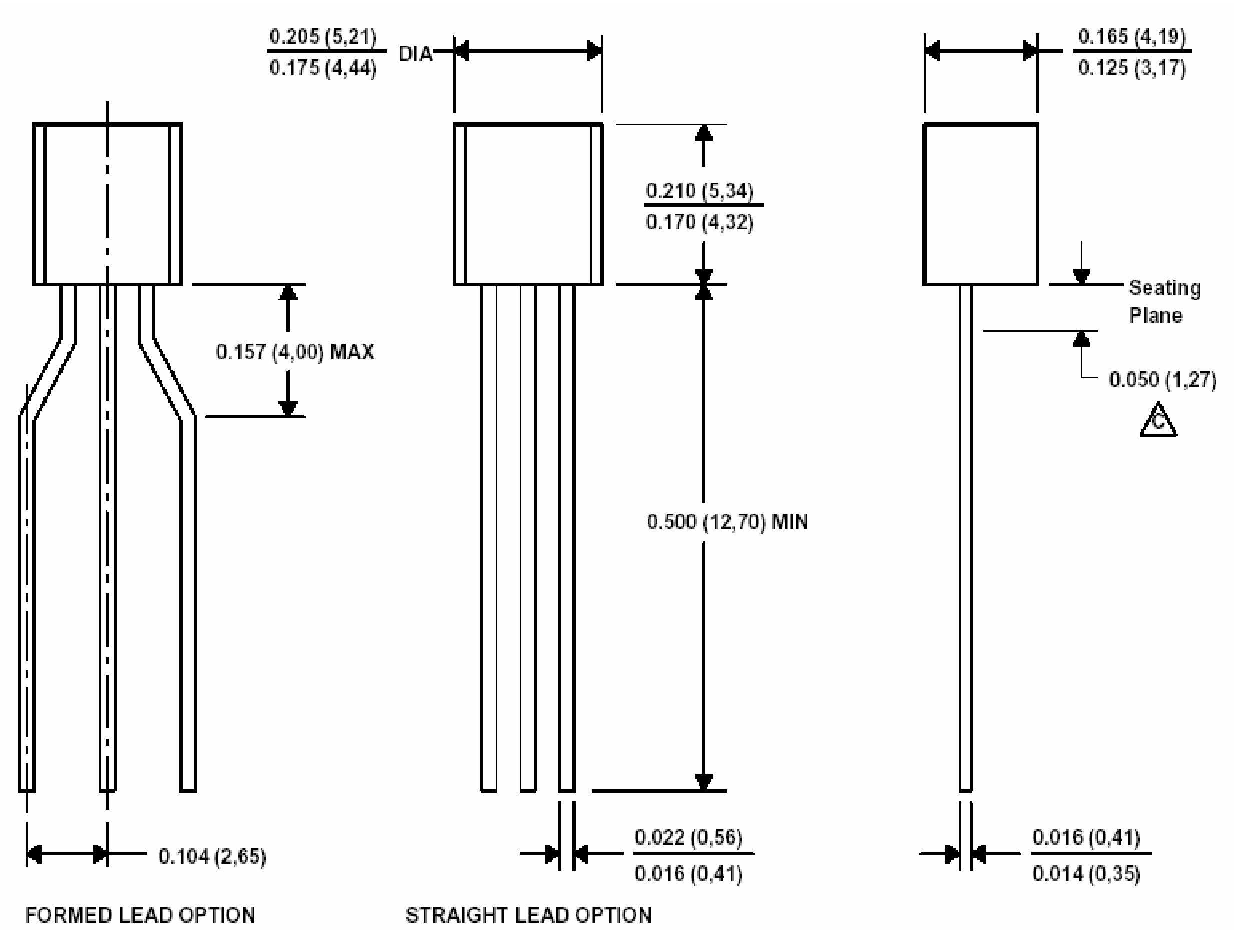


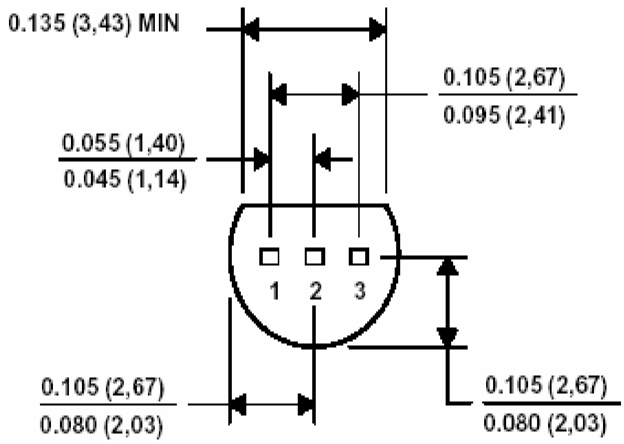
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50

NOTES:

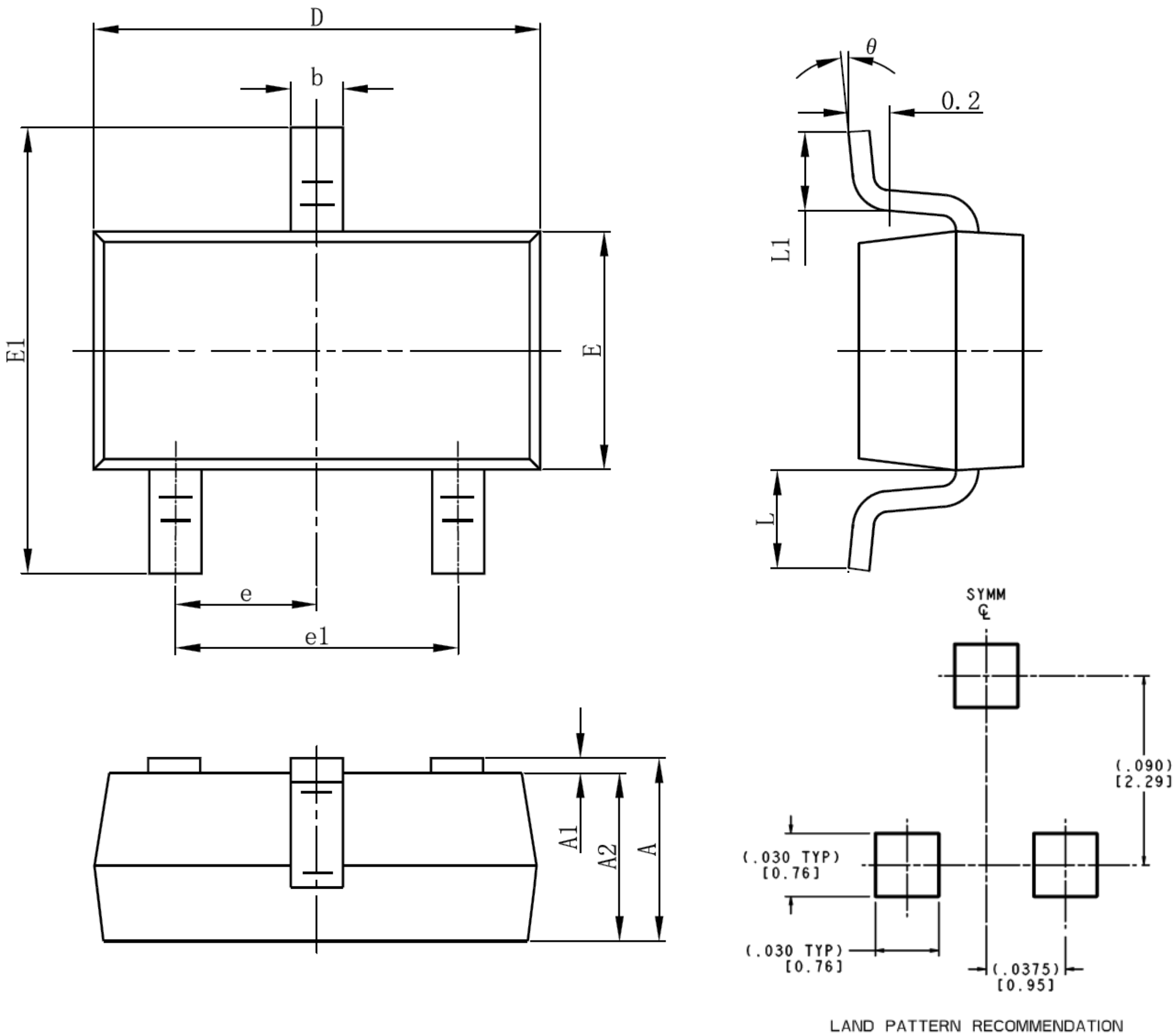
1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B ‑ 0.25 mm (0.010) per side.

TO-92


0.205 (5,21)
0.175 (4,44)
DIA
0.165 (4,19)
0.125 (3,17)
0.210 (5,34)
0.170 (4,32)
0.157 (4,00) MAX
Seating
Plane
0.050 (1,27)
C
0.500 (12,70) MIN
0.104 (2,65)
0.022 (0,56)
0.016 (0,41)
0.016 (0,41)
0.014 (0,35)
FORMED LEAD OPTION
STRAIGHT LEAD OPTION

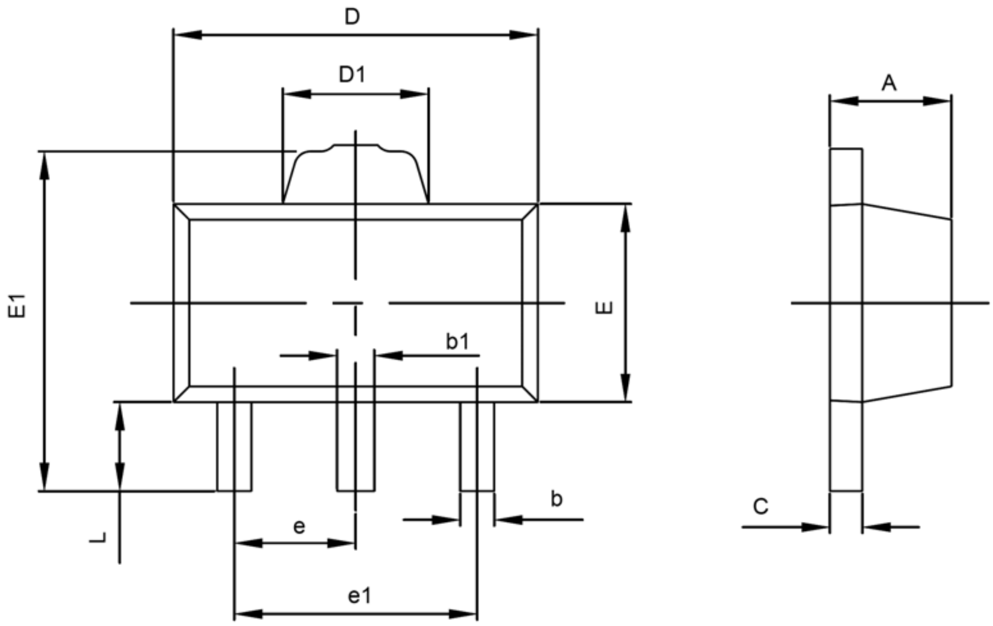

0.135 (3,43) MIN
0.105 (2,67)
0.095 (2,41)
0.055 (1,40)
0.045 (1,14)
1
2
3
0.105 (2,67)
0.080 (2,03)
0.105 (2,67)
0.080 (2,03)

SOT-23-3L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-89-3L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.360	0.560	0.014	0.022
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.400	1.800	0.055	0.071
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	2.900	3.100	0.114	0.122
L	0.900	1.100	0.035	0.043