



# LC9226

**PMU with 2 Synchronous 1.5A Bucks and 4 CMOS 600mA LDOs**

## DESCRIPTION

The LC9226 is a power management unit (PMU), with 2 synchronous Buck and 4 CMOS low-dropout regulators that delivers a maximum current of 1.5A for each Buck's output and a maximum current of 0.6A for each LDO's output.

The synchronous buck is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 1A of output current. The device operates from an input voltage range of 2.6V to 6V and provides an output voltage from 0.6V to VDD, making the buck ideal for low voltage power conversions. Running at a fixed frequency of 1.5MHz allows the use of small external components, such as ceramic input and output caps, as well as small inductors, while still providing low output ripples. This low noise output along with its excellent efficiency achieved by the internal synchronous rectifier, making the buck an ideal green replacement for large power consuming linear regulator. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

The LDO is a low-dropout regulator that delivers a maximum current of 0.5A output. Typical dropout voltage at 0.5A load current is 0.8V. It has excellent load and line transient response and good temperature characteristics, which can assure the stability of chip and power system. The output accuracy is set within 2% by trimming.

Typical LDO output voltage:  $V_{OUT}=1.8V$ . Other fixed voltage can be provided in the range of 1.2V~4.5V every 0.1V step. It also can be customized on command. LDO can also work under a wide input voltage ranging from 2V to 6V. They can provide foldback short-circuit protection and output current limit function.

LC9226 is available in lead (Pb)-free DFN5x5-32 (with exposed pad for heat dissipation) package.

## FEATURES

### BUCK

- High efficiency: up to 97%
- Up to 1.5A Max output current
- 2MHz switching frequency
- Low dropout 100% duty operation
- Internal compensation and soft-start
- Current mode control
- Reference 0.6V
- Logic control shutdown ( $I_Q < 1\mu A$ )
- Thermal shutdown, UVLO

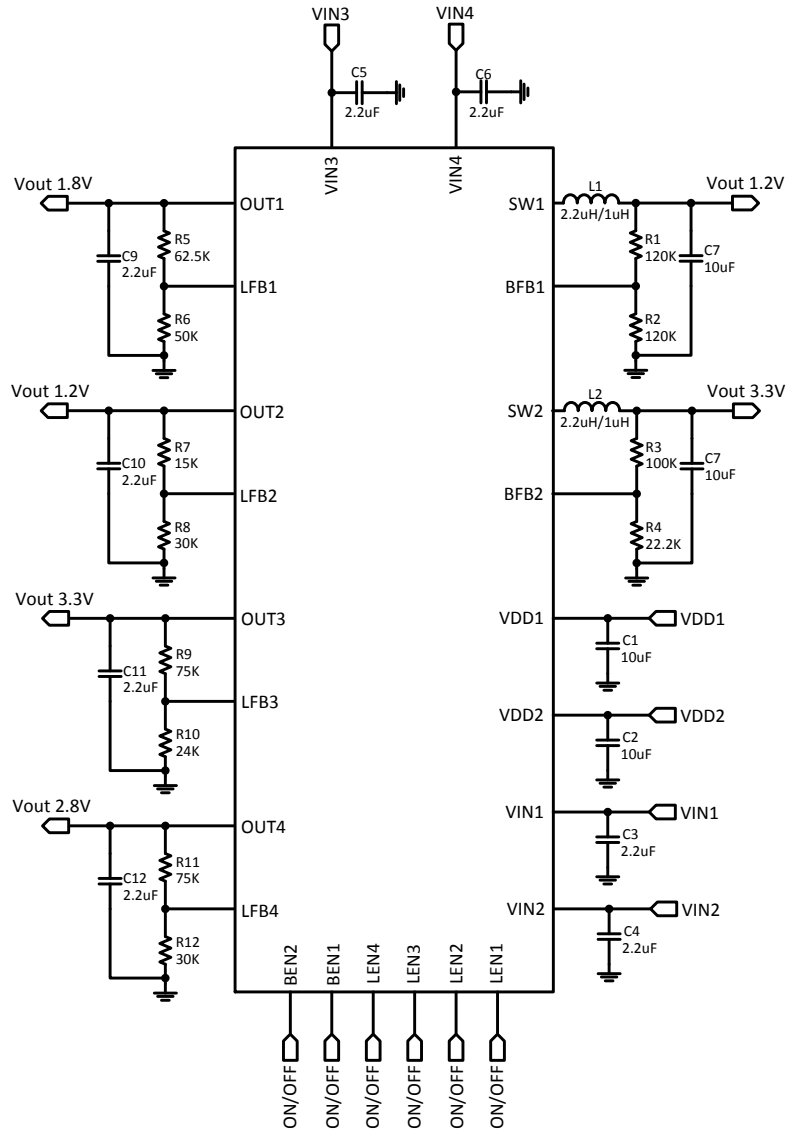
### LDO

- Low power consumption: 40uA (Typ.)
- Maximum output current: 600mA
- Low dropout voltage:
  - 180mV@ $I_{OUT}=300mA, V_{OUT}=3.3V$
  - 360mV@ $I_{OUT}=600mA, V_{OUT}=3.3V$
- Build-in chip enable and discharge circuit
- Input voltage range: 2.5~6V
- Adjustable output from 0.8V to 5.0V
- Output voltage accuracy:  $\pm 2\%$
- Output current limit
- Short circuit protection
- Over temperature protection

## APPLICATIONS

- Distributed power systems
- Digital set top boxes
- Flat panel television and monitors
- Wireless and DSL modems
- Power source for cellular phones and various kind of PCSs
- Battery powered equipment

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Mark explanation  |             | <table border="1"> <thead> <tr> <th colspan="2">Ordering information</th> </tr> </thead> <tbody> <tr> <td>DFN5x5-32<br/>3000pcs/reel</td> <td>LC9226CJMTR</td> </tr> </tbody> </table> | Ordering information |  | DFN5x5-32<br>3000pcs/reel | LC9226CJMTR |
|---|-------------|--|----------------------|--|---------------------------|-------------|
| Ordering information  |             |  |                      |  |                           |             |
| DFN5x5-32<br>3000pcs/reel                                       | LC9226CJMTR |  |                      |  |                           |             |
| <p>LC9226: Product code<br/>XXXX: Lot No.<br/>YW: Date code</p> |             |  |                      |  |                           |             |

## ABSOLUTE MAXIMUM RATING

| Parameter   |           | Value         |
|---|-----------|---------------|
| Max input voltage (VDD1, VDD2)                      |           | 8V            |
| Max input voltage (VIN1, VIN2, VIN3, VIN4)          |           | 8V            |
| Max operating junction temperature(T <sub>j</sub> ) |           | 125°C         |
| Ambient temperature(T <sub>A</sub> )                |           | -40°C – 85°C  |
| Maximum power dissipation                           | DFN5x5-32 | 1.8W          |
| Package thermal resistance (θ <sub>JC</sub> )       |           | 13°C / W      |
| Package thermal resistance (θ <sub>JA</sub> )       |           | 50°C / W      |
| Storage temperature(T <sub>S</sub> )                |           | -40°C - 150°C |
| Lead temperature & time                             |           | 260°C, 10S    |

**Note:** Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.

## PIN DESCRIPTION

| Pin # | Name | Description       | Pin # | Name | Description       |
|-------|------|-------------------|-------|------|-------------------|
| 1     | OUT1 | LDO output pin    | 17    | OUT3 | LDO output pin    |
| 2     | VIN1 | LDO input pin     | 18    | VIN3 | LDO input pin     |
| 3     | LFB1 | LDO feedback pin  | 19    | LFB3 | LDO feedback pin  |
| 4     | G1   | Ground pin        | 20    | G3   | Ground pin        |
| 5     | LEN1 | LDO enable pin    | 21    | LEN3 | LDO enable pin    |
| 6     | BEN1 | Buck enable pin   | 22    | BEN2 | Buck enable pin   |
| 7     | BFB1 | Buck feedback pin | 23    | BFB2 | Buck feedback pin |
| 8     | VDD1 | Buck input pin    | 24    | VDD2 | Buck input pin    |
| 9     | GND1 | Ground pin        | 25    | GND2 | Ground pin        |
| 10    | SW1  | Switch pin        | 26    | SW2  | Switch pin        |
| 11    | GND  | Ground pin        | 27    | GND  | Ground pin        |
| 12    | G2   | Ground pin        | 28    | G4   | Ground pin        |
| 13    | VIN2 | LDO input pin     | 29    | VIN4 | LDO input pin     |
| 14    | LEN2 | LDO enable pin    | 30    | LEN4 | LDO enable pin    |
| 15    | OUT2 | LDO output pin    | 31    | OUT4 | LDO output pin    |
| 16    | LFB2 | LDO feedback pin  | 32    | LFB4 | LDO feedback pin  |

## ELECTRICAL CHARACTERISTICS

(VDD=5V, T<sub>A</sub>=25°C)

| Symbol                | Parameter                   | Conditions                                   | Min   | Typ | Max   | Unit |
|-----------------------|-----------------------------|--|-------|-----|-------|------|
| <b>BUCK</b>           |                             |  |       |     |       |      |
| VDD                   | Input voltage range         |  | 2.6   |     | 5.5   | V    |
| V <sub>OV</sub> P     | Input overvoltage threshold |  |       | 6.1 |       | V    |
| V <sub>REF</sub>      | Feedback voltage            | VDD=5V                                       | 0.588 | 0.6 | 0.612 | V    |
| I <sub>FB</sub>       | Feedback leakage current    |  |       | 0.1 | 1     | uA   |
| I <sub>Q</sub>        | Quiescent current           | Active, V <sub>FB</sub> =0.65V, No Switching |       | 80  |       | uA   |
| I <sub>SHUTDOWN</sub> | Shutdown input current      | BEN=0V                                       |       |     | 1     | uA   |
| LNR                   | Line regulation             | VDD=2.6V to 5.5V                             |       | 0.1 | 0.2   | %/V  |
| LDR                   | Load regulation             | I <sub>OUT</sub> =0.01 to 1A                 |       | 0.1 | 0.2   | %/A  |
| F <sub>SOC</sub>      | Switching frequency         |  | 1.6   | 2   | 2.4   | MHz  |
| R <sub>DSON_P</sub>   | PMOS R <sub>DSON</sub>      |  |       | 250 | 350   | mΩ   |

|   |  |   |       |           |                 |                         |
|---|--|---|-------|-----------|-----------------|-------------------------|
| $R_{\text{DSON\_N}}$  | NMOS $R_{\text{DSON}}$                 |   |       | 150       | 250             | m $\Omega$              |
| $V_{\text{UVLO}}$   | Under voltage lockout                  |   | 1.9   | 2.1       | 2.3             | V                       |
| $V_{\text{UVLO\_HY}}$   | UVLO hysteresis                        |   |       | 100       |                 | mV                      |
| $I_{\text{LIMIT}}$  | Peak current limit                     |   | 1.8   | 2.3       | 2.8             | A                       |
| $I_{\text{NOLOAD}}$   |  | VDD=5V, $V_{\text{OUT}}=3.3\text{V}$ , $I_{\text{OUT}}=0\text{A}$   |       | 80        |                 | $\mu\text{A}$           |
| $I_{\text{SWLK}}$   | SW leakage current                     | VDD=6V, $V_{\text{SW}}=0$ or 6V, BEN=0V   |       |           | 1               | $\mu\text{A}$           |
| $I_{\text{BENLK}}$  | BEN leakage current                    |   |       |           | 1               | $\mu\text{A}$           |
| $V_{\text{H\_BEN}}$   | BEN input high voltage                 |   | 1.2   |           |                 | V                       |
| $V_{\text{L\_BEN}}$   | BEN input low voltage                  |   |       |           | 0.5             | V                       |
| $T_{\text{SD}}$   | Thermal shutdown temp                  |   |       | 160       |                 | $^{\circ}\text{C}$      |
| $T_{\text{SH}}$   | Thermal shutdown hysteresis            |   |       | 15        |                 | $^{\circ}\text{C}$      |
| <b>LDO</b>  |  |   |       |           |                 |                         |
| $V_{\text{IN}}$   | Input voltage                          |   | 2.5   |           | 6               | V                       |
| $V_{\text{FB}}$   | Regulated feedback voltage             | $V_{\text{IN}}=3.3\text{V}$ , $I_{\text{OUT}}=10\text{mA}$  | 0.784 | 0.8       | 0.816           | V                       |
| $V_{\text{DROP}}$   | Dropout voltage <sup>(1)</sup>         | $V_{\text{OUT}}=1.8\text{V}$ , $I_{\text{OUT}}=600\text{mA}$  |       | 1030      | 1200            | mV                      |
|   |  | $V_{\text{OUT}}=2.5\text{V}$ , $I_{\text{OUT}}=600\text{mA}$  |       | 500       | 600             | mV                      |
|   |  | $V_{\text{OUT}}=3.3\text{V}$ , $I_{\text{OUT}}=600\text{mA}$  |       | 360       | 430             | mV                      |
| $\frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}} \cdot V_{\text{out}}}$ | Line regulation                        | $I_{\text{OUT}}=10\text{mA}$ , $2.5\text{V} \leq V_{\text{IN}} \leq 6\text{V}$                                    |       | 0.05      | 0.2             | %/V                     |
| $\Delta V_{\text{out}}$   | Load regulation                        | $V_{\text{IN}}=4.3\text{V}$ , $V_{\text{OUT}}=3.3\text{V}$<br>$10\text{mA} \leq I_{\text{OUT}} \leq 600\text{mA}$ |       | 50        | 80              | mV                      |
| $I_{\text{Q}}$  | Supply current                         | $V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$ , $V_{\text{IN}} = V_{\text{EN}}$                                    |       | 40        | 100             | $\mu\text{A}$           |
| $I_{\text{STANDBY}}$  | Supply current (standby)               | $V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$ , $V_{\text{EN}} = \text{GND}$                                       |       | 0.1       | 1.0             | $\mu\text{A}$           |
| $\frac{\Delta V_{\text{out}}}{\Delta T \cdot V_{\text{out}}}$             | Output voltage temperature coefficient | $I_{\text{OUT}}=10\text{mA}$  |       | $\pm 100$ |                 | ppm/ $^{\circ}\text{C}$ |
| PSRR  | Ripple rejection                       | F=1KHz, Ripple=1Vp-p<br>$V_{\text{IN}} = V_{\text{OUT}} + 1\text{V}$  |       | 60        |                 | dB                      |
| $I_{\text{LIM}}$  | Current limit                          | $V_{\text{IN}}=4.3\text{V}$ , $V_{\text{OUT}}=3.3\text{V}$  |       | 1         |                 | A                       |
| $I_{\text{SHORT}}$  | Short current limit                    | $V_{\text{OUT}}=0\text{V}$  |       | 200       |                 | mA                      |
| $R_{\text{DISCHARGE}}$  | Discharge resistor                     | EN=0, $V_{\text{OUT}}=3\text{V}$  |       | 280       |                 | $\Omega$                |
| $V_{\text{LENH}}$   | LEN input voltage "H"                  |   | 1.5   |           | $V_{\text{IN}}$ | V                       |
| $V_{\text{LENL}}$   | LEN input Voltage "L"                  |   | 0     |           | 0.3             | V                       |
| $T_{\text{SD}}$   | Thermal shutdown temp                  |   |       | 160       |                 | $^{\circ}\text{C}$      |
| $T_{\text{SH}}$   | Thermal shutdown hysteresis            |   |       | 30        |                 | $^{\circ}\text{C}$      |

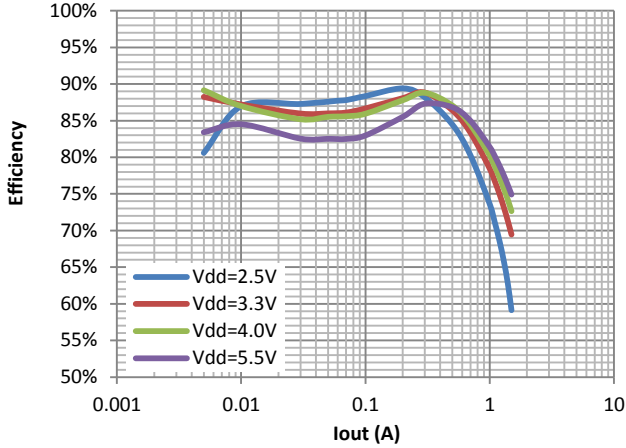
**Note:** 1)  $V_{\text{DROP}} = V_{\text{IN}} - V_{\text{OUT}}$  when  $V_{\text{OUT}}$  drops below 98% of the normal  $V_{\text{OUT}}$ .

## ELECTRICAL PERFORMANCE

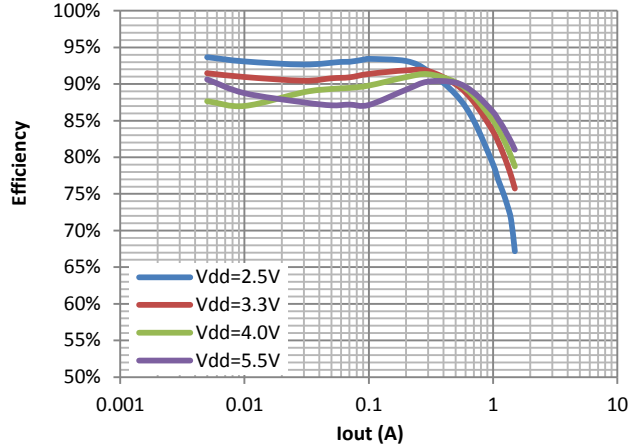
Tested under  $T_A=25^\circ\text{C}$ , unless otherwise specified

### BUCK

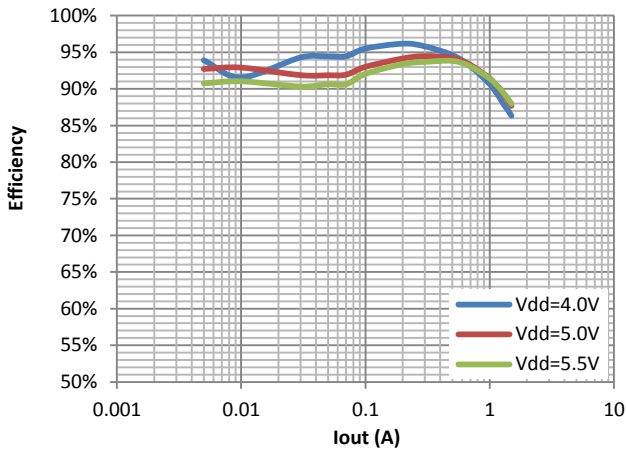
**Efficiency vs. Output Current  
(Vout=1.2V)**



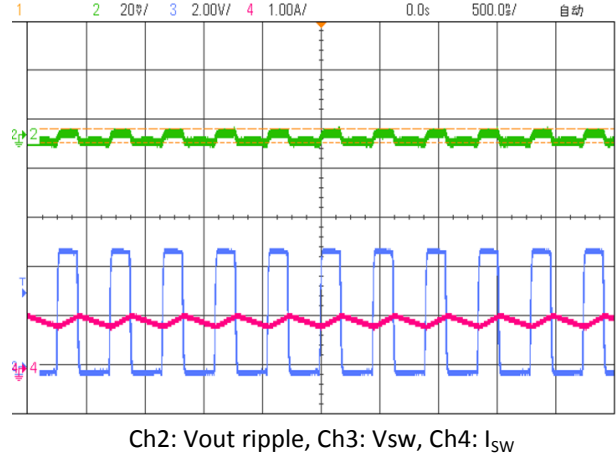
**Efficiency vs. Output Current  
(Vout=1.8V)**



**Efficiency vs. Output Current  
(Vout=3.3V)**

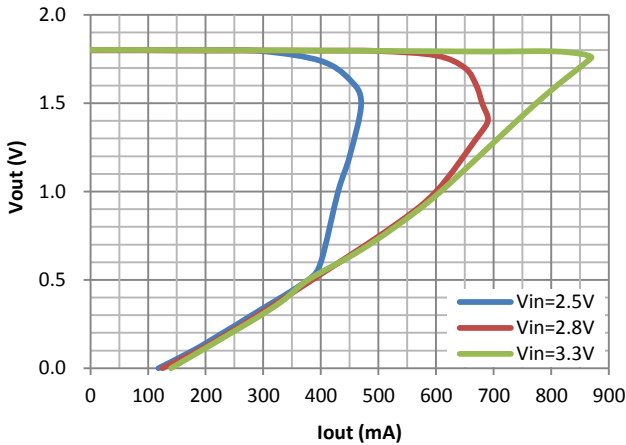


**Output Ripple and SW at 1A load  
(VDD=5V / Vout=1.8V)**

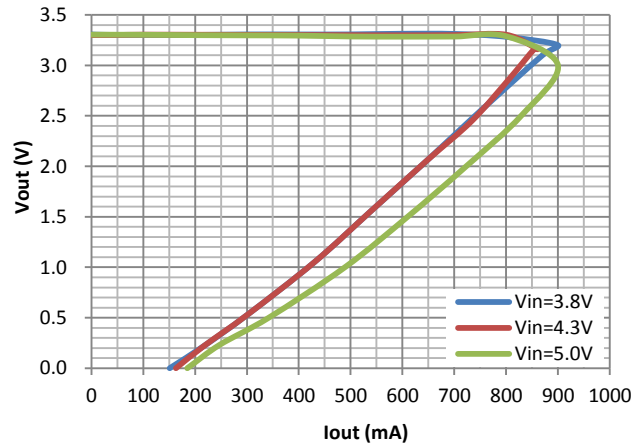


### LDO

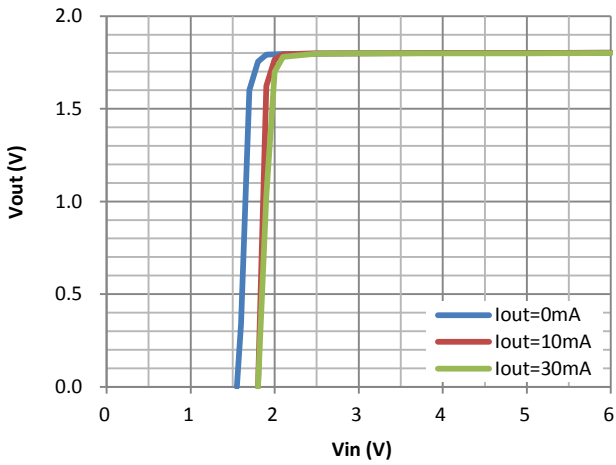
**Load Regulation  
(Vout=1.8V)**



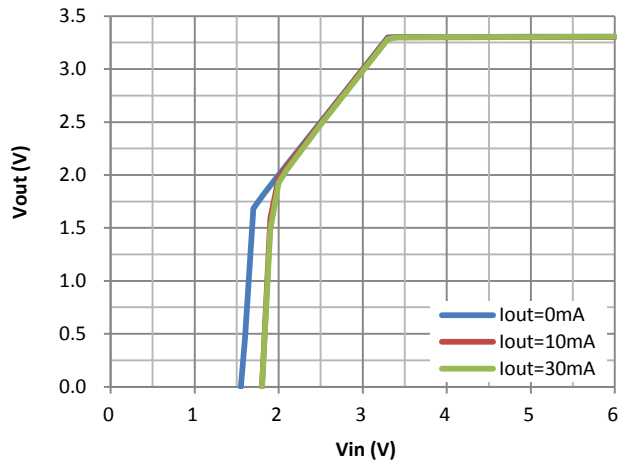
**Load Regulation  
(Vout=3.3V)**



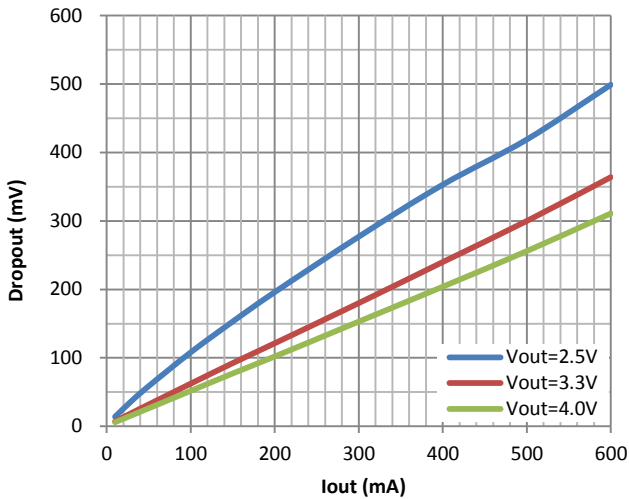
**Line Regulation**  
(Vout=1.8V)



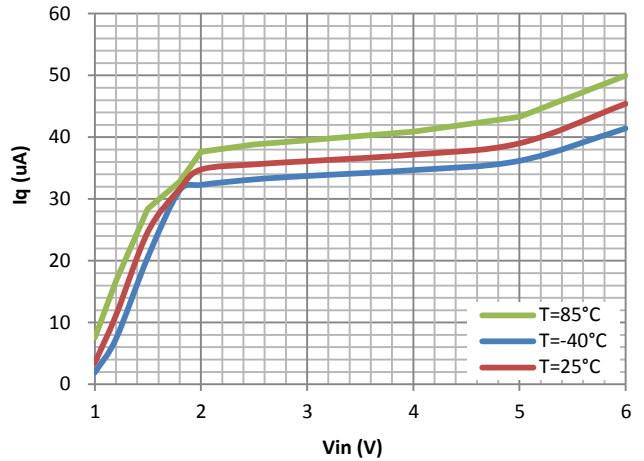
**Line Regulation**  
(Vout=3.3V)



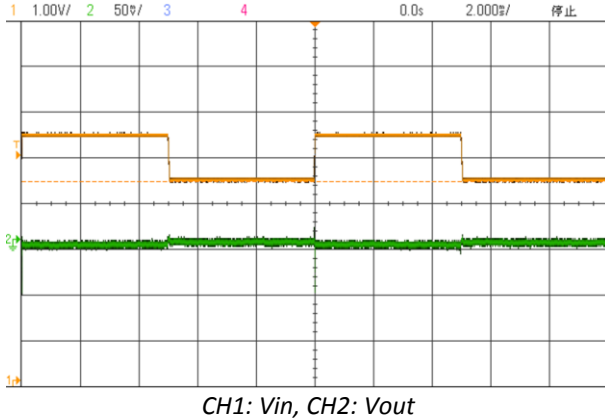
**Dropout Voltage**



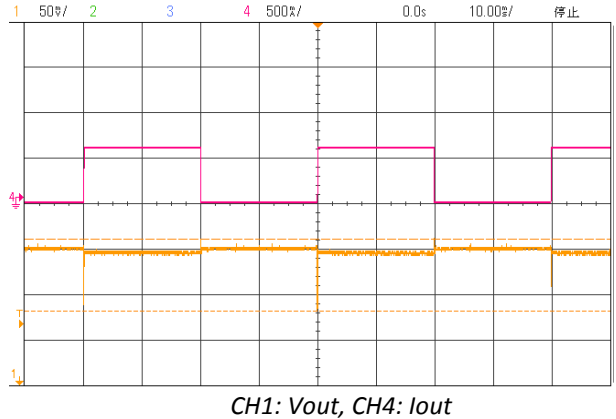
**Iq**  
(Vout=1.8V)



**Line Transient Response**  
(Vout=3.3V, Iout=10mA)  
(Vin=4.3-5.3V, Vout p-p=78mV)



**Load Transient Response**  
(Vin=4.3V, Vout=3.3V, Iout=10-600mA)  
(TRISE=1uS, TFALL=1uS, Vout p-p=74mV)



## DETAILED DESCRIPTION

### BUCK

The LC9226 high-efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 1.5A of output current. The device operates in pulse-width modulation (PWM) at 2MHz from a 2.6V to 5.5V input voltage and provides an output voltage from 0.6V to VDD, making the LC9226 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

### Loop operation

LC9226 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

### Current sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

### Current limit

There is a cycle-by-cycle current limit on the high-side MOSFET of 2.3A (typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on.

LC9226 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 100mV, limiting the current to 2.3A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

### Soft-start

LC9226 has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal shutdown event, the soft-start circuitry slowly ramps up current available at SW.

### UVLO

If VDD drops below 2.1V, the UVLO circuit inhibits switching. Once VDD rises above 2.2V, the UVLO clears, and the soft-start sequence activates.

### Thermal shutdown

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature exceeds  $T_J = +160^\circ\text{C}$ , a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by  $15^\circ\text{C}$ , resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

### Setting output voltages

Output voltages are set by external resistors. The FB threshold is 0.6V.

$$R_{TOP} = R_{BOTTOM} \times \left( \frac{V_{OUT}}{0.6} - 1 \right)$$

### Input capacitor selection

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum

capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_S} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

## THERMAL CONSIDERATIONS

Thermal consideration has to be taken account into to ensure proper function of the device. Power dissipation of LC9226 can be calculated as

$$\text{LDO Power Dissipation: } P_L = (V_{IN} - V_{OUT}) \times I_{OUT}$$

## APPLICATION INFORMATION

Layout is critical to achieve clean and stable operation. The switching power stage and heat dissipation requires particular attention. Follow these guidelines for good PC board layout:

- 1) Place decoupling capacitors as close to the IC as possible
- 2) Connect input and output capacitors to the same power ground node with a star ground configuration then to IC ground.
- 3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (CIN to VDD and CIN to GND) short. Avoid vias in the switching paths.
- 4) If possible, connect VIN, VOUT, VDD, SW, and GND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
- 5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
- 6) Route high-speed switching nodes away from sensitive analog areas.

## LDO

The device has built-in modules including high accuracy voltage reference, error amplifier, current limit, power transistors and driver circuit. Current limit functions ensure reliability of device and power system.

The bandgap module provides stable reference voltage whose temperature coefficient is compensated by careful design considerations. The temperature coefficient is under 100 ppm/°C. It has excellent load and line transient response and good temperature characteristics, which can assure the stability of chip and power system. The accuracy of output voltage is guaranteed by trimming technique.

For proper function and safe operation of the device, total power dissipation is recommended to be limited within 1.6W.



## PACKAGE OUTLINE

