

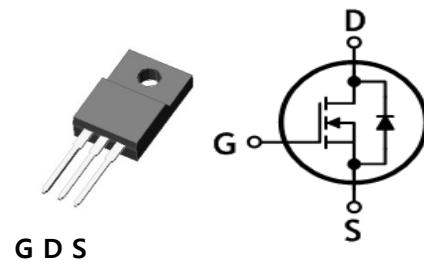
## SWITCHING REGULATOR APPLICATIONS

### Features

- High Voltage :  $BV_{DSS}=650V$ (Min.)
- Low  $C_{rss}$  :  $C_{rss}=16pF$ (Typ.)
- Low gate charge :  $Q_g=35nC$ (Typ.)
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=0.85\Omega$ (Max.)

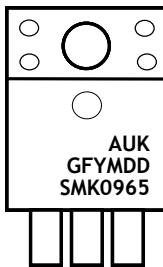
### Ordering Information

Part Number	Marking	Package
SMK0965AF	SMK0965	TO-220F-3L



TO-220F-3L

### Marking Diagram



Column 1 : Manufacturer  
 Column 2 : Production Information  
 e.g.) GFYMDD  
 -.. G : Option Code (H : Halogen Free)  
 -.. F : Factory Management Code  
 -.. YMDD : Date Code (Year, Month, Date)  
 Column 3 : Device Code

### Absolute maximum ratings ( $T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	$V_{DSS}$		650	V
Gate-source voltage	$V_{GSS}$		$\pm 30$	V
Drain current (DC) *	$I_D$	$T_c=25^\circ C$	9	A
		$T_c=100^\circ C$	5.5	A
Drain current (Pulsed) *	$I_{DM}$		36	A
Power dissipation	$P_D$		40	W
Avalanche current (Single) ②	$I_{AS}$		9	A
Single pulsed avalanche energy ②	$E_{AS}$		250	mJ
Avalanche current (Repetitive) ①	$I_{AR}$		9	A
Repetitive avalanche energy ①	$E_{AR}$		11.6	mJ
Junction temperature	$T_J$		150	$^\circ C$
Storage temperature range	$T_{stg}$		-55~150	

\* Limited by maximum junction temperature

Characteristic	Symbol		Typ.	Max.	Unit
Thermal resistance	Junction-case	$R_{th(J-C)}$	-	3.1	$^\circ C/W$
	Junction-ambient	$R_{th(J-A)}$	-	62.5	

**Electrical Characteristics ( $T_c=25^\circ\text{C}$  unless otherwise noted)**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$\text{BV}_{\text{DSS}}$	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	650	-	-	V
Gate threshold voltage	$V_{GS(\text{th})}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2.0	-	4.0	V
Drain-source cut-off current	$I_{\text{DSS}}$	$V_{DS}=650\text{V}, V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance <sup>(4)</sup>	$R_{DS(\text{on})}$	$V_{GS}=10\text{V}, I_D=4.5\text{A}$	-	0.72	0.85	$\Omega$
Forward transfer conductance <sup>(4)</sup>	$g_{fs}$	$V_{DS}=10\text{V}, I_D=4.5\text{A}$	-	11	-	S
Input capacitance	$C_{iss}$	$V_{GS}=0\text{V}, V_{DS}=25\text{V}$ $f=1\text{ MHz}$	-	2040	2550	pF
Output capacitance	$C_{oss}$		-	153	192	
Reverse transfer capacitance	$C_{rss}$		-	16	20	
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD}=300\text{V}, I_D=9\text{A}$ $R_G=25\Omega$	-	23	-	ns
Rise time	$t_r$		-	69	-	
Turn-off delay time	$t_{d(\text{off})}$		-	144	-	
Fall time	$t_f$		-	77	-	
Total gate charge	$Q_g$	$V_{DS}=520\text{V}, V_{GS}=10\text{V}$ $I_D=9\text{A}$	-	35	57	nC
Gate-source charge	$Q_{gs}$		-	10	-	
Gate-drain charge	$Q_{gd}$		-	9	-	

**Source-Drain Diode Ratings and Characteristics ( $T_c=25^\circ\text{C}$  unless otherwise noted)**

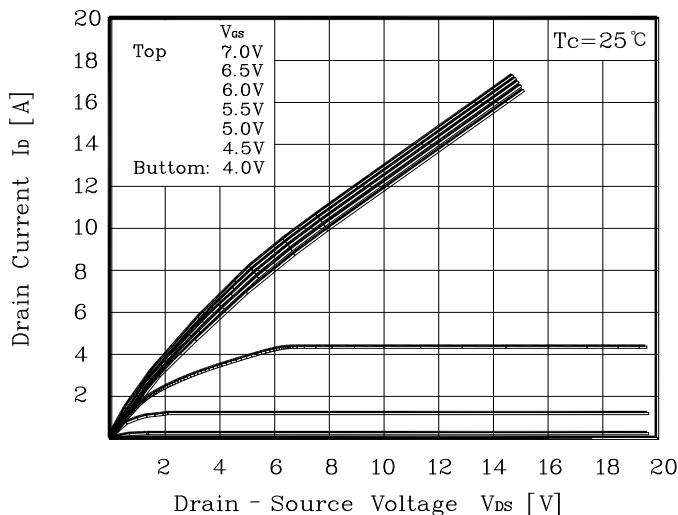
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_s$	Integral reverse diode in the MOSFET	-	-	9	A
Source current (Pulsed) <sup>(1)</sup>	$I_{sM}$		-	-	36	
Forward voltage <sup>(4)</sup>	$V_{SD}$	$V_{GS}=0\text{V}, I_s=9\text{A}$	-	-	1.4	V
Reverse recovery time	$t_{rr}$	$I_s=9\text{A}, V_{GS}=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	420	-	ns
Reverse recovery charge	$Q_{rr}$		-	4.2	-	$\mu\text{C}$

Note ;

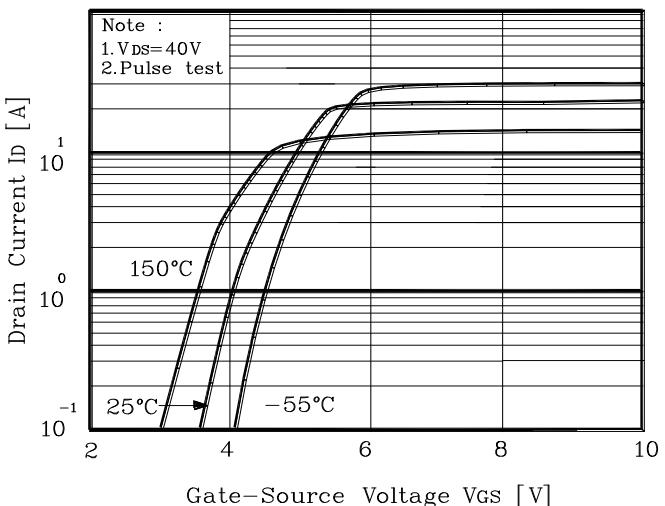
- ① Repetitive rating : Pulse width limited by maximum junction temperature
- ②  $L=5.7\text{mH}, I_{AS}=9\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
- ③ Pulse Test : Pulse width $\leq 300\text{us}$ , Duty cycle $\leq 2\%$
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

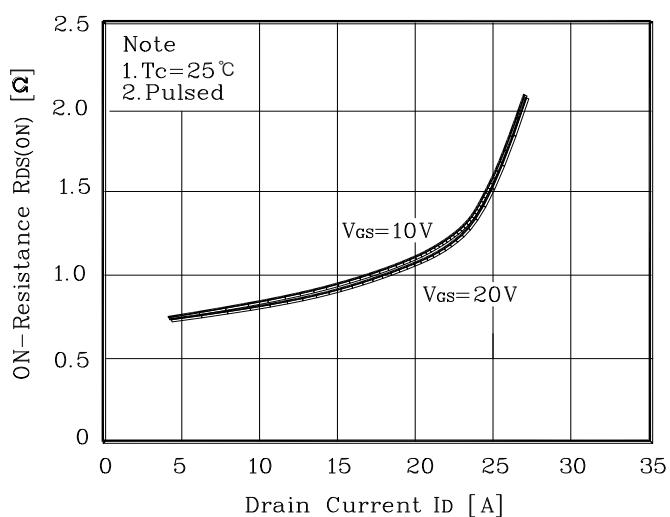
**Fig. 1  $I_D$  -  $V_{DS}$**



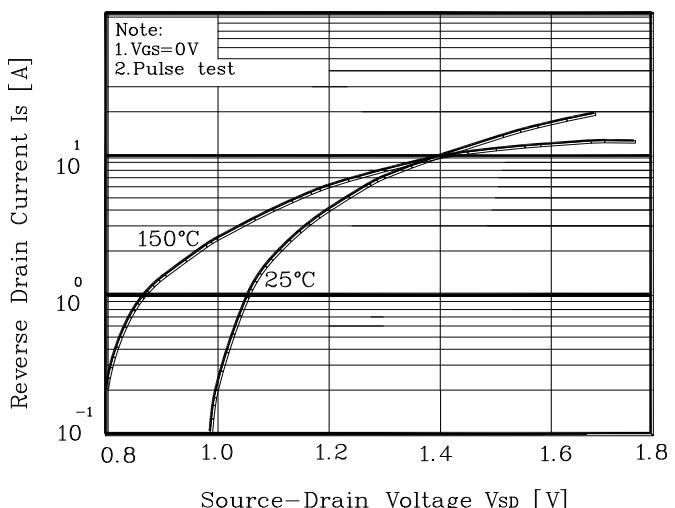
**Fig. 2  $I_D$  -  $V_{GS}$**



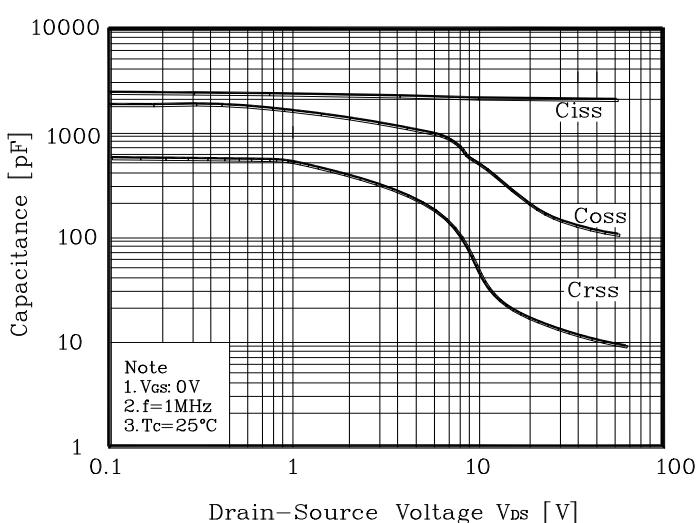
**Fig. 3  $R_{DS(on)}$  -  $I_D$**



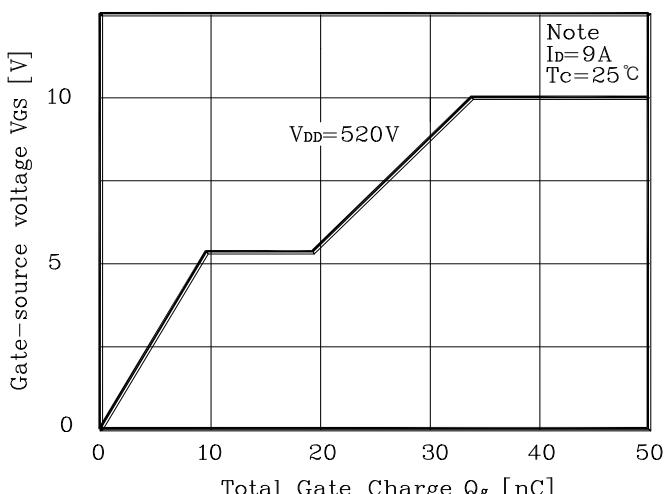
**Fig. 4  $I_S$  -  $V_{SD}$**



**Fig. 5 Capacitance -  $V_{DS}$**

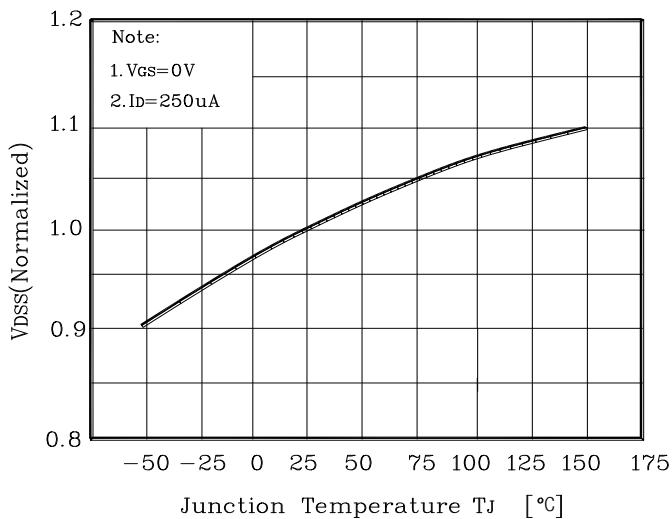


**Fig. 6  $V_{GS}$  -  $Q_G$**

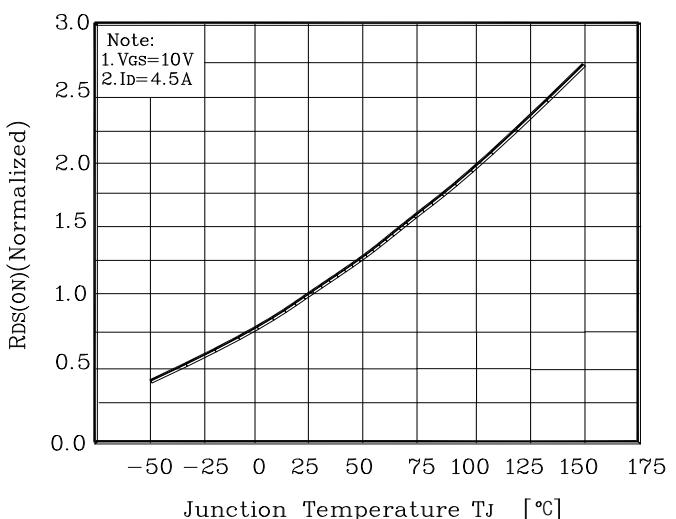


## Electrical Characteristic Curves

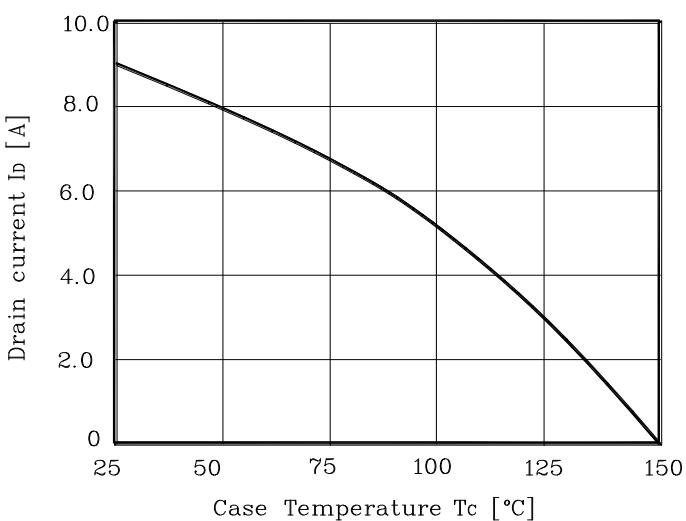
**Fig. 7  $V_{DSS}$  -  $T_J$**



**Fig.8  $R_{DS(on)}$  -  $T_J$**



**Fig. 9  $I_D$  -  $T_c$**



**Fig. 10 Safe Operating Area**

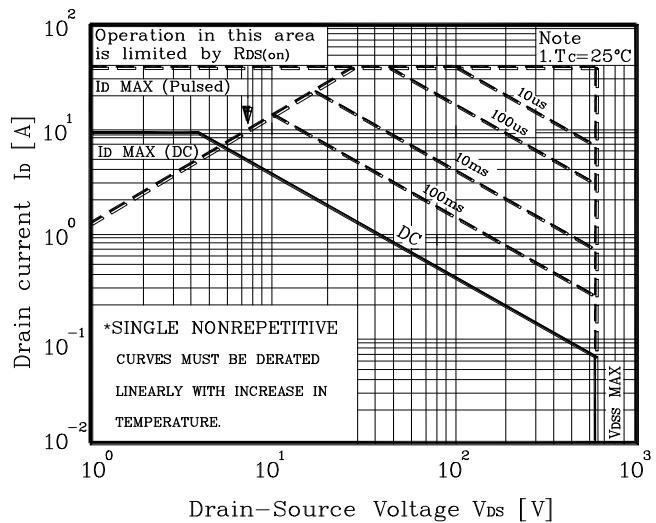


Fig. 11 Gate Charge Test Circuit & Waveform

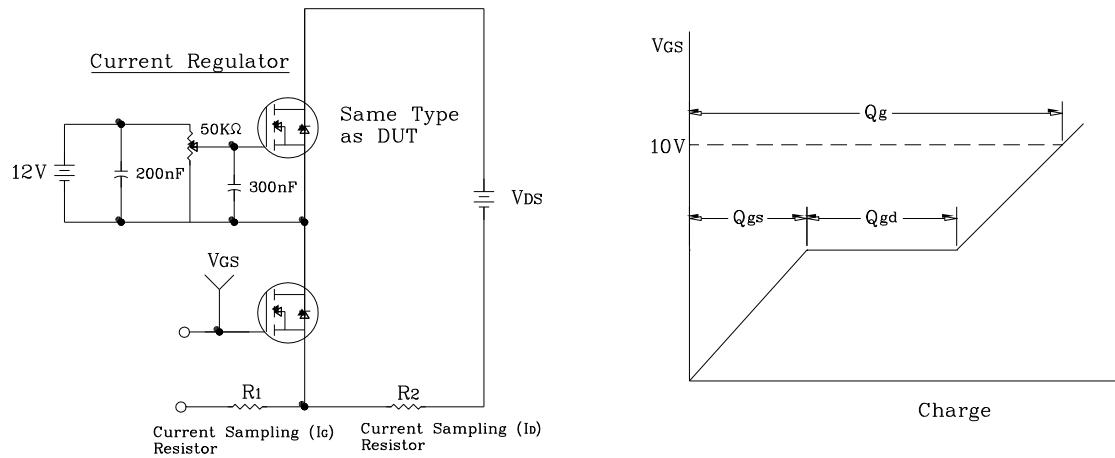


Fig. 12 Resistive Switching Test Circuit & Waveform

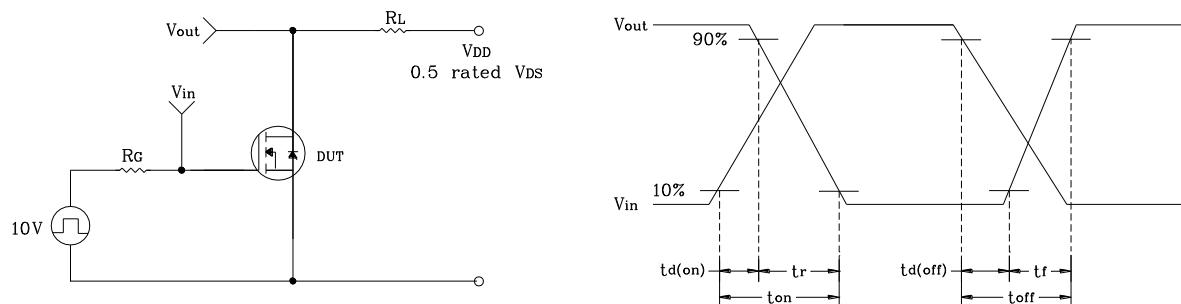


Fig. 13 E<sub>AS</sub> Test Circuit & Waveform

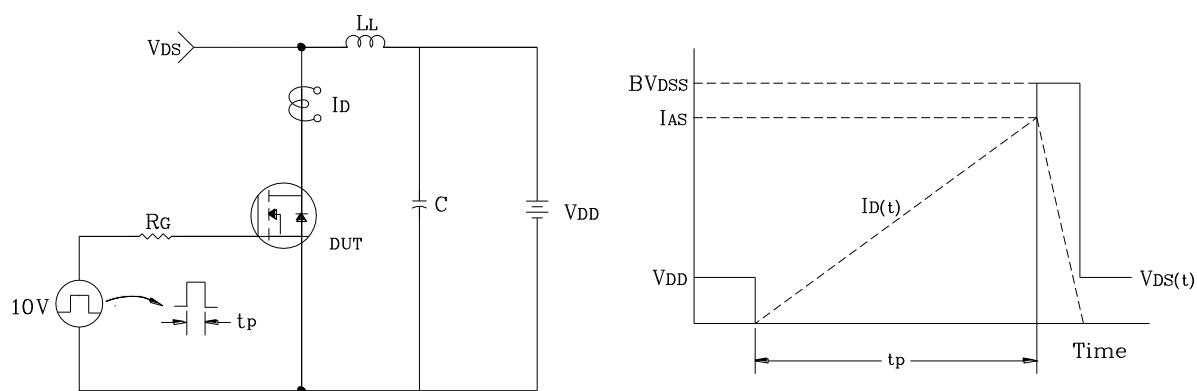
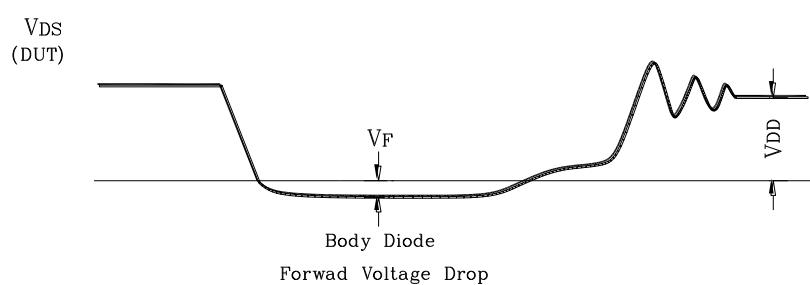
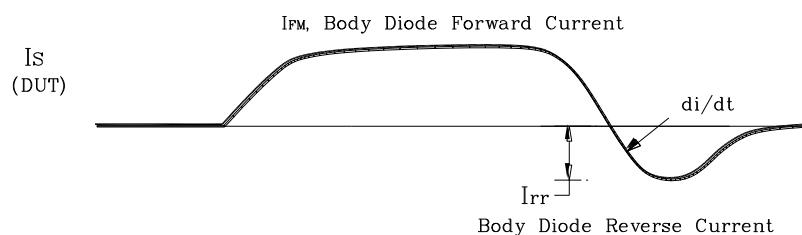
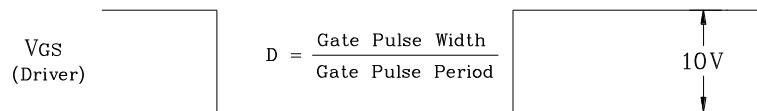
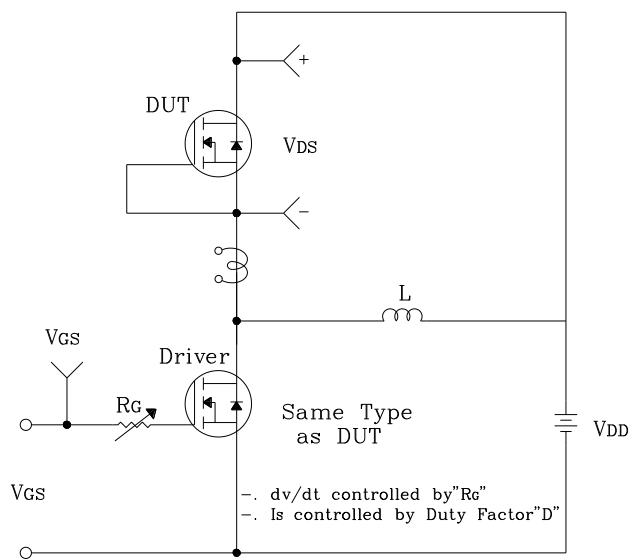
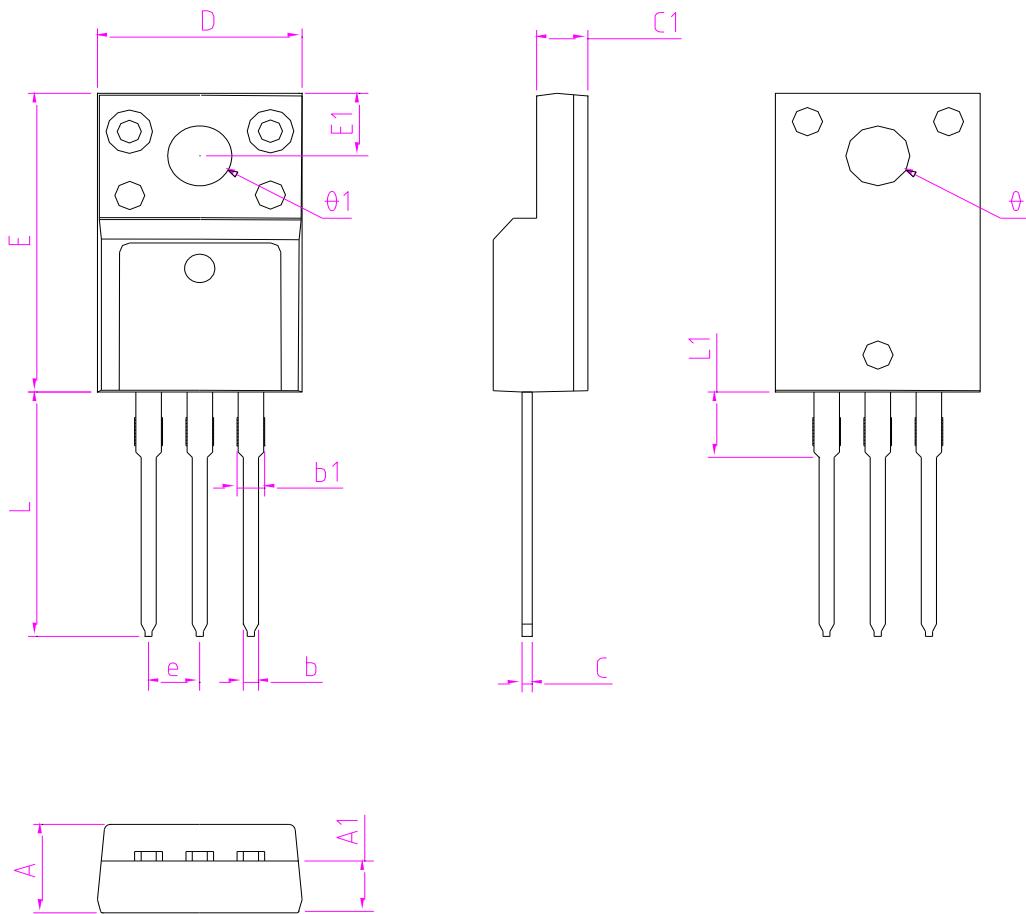


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



**Package Outline Dimension**

SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	4.65	4.70	4.75	
A1	2.71	2.76	2.81	
b	0.70	0.80	0.90	
b1	1.28	1.38	1.43	
C	0.40	0.50	0.60	
C1	2.04	2.54	3.04	
D	10.06	10.16	10.26	
e	2.54 REF			
E	15.77	15.87	15.97	
E1	3.05	3.30	3.55	
L	12.68	12.98	13.28	
L1	3.18 REF			
θ	3.30	3.40	3.50	
θ1	3.08	3.18	3.28	

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