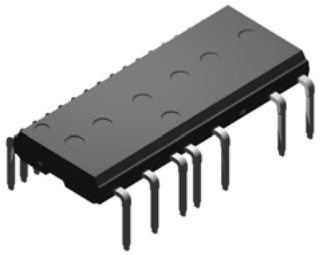
SPE02M50T-AN/CN

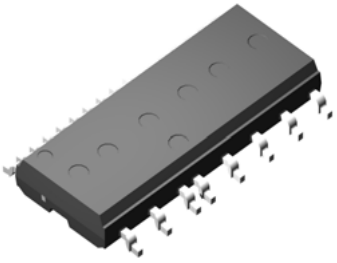
主要参数 MAIN CHARACTERISTICS

500V/2A 3 相全桥驱动	
V_{DSS}	500V
I_D	1.2A
I_{DM}	2A
V_{ISO}	1500V

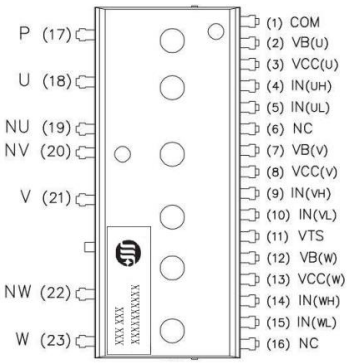
封装 Package



DIP23-FP



SOP23-FP



PIN1-PIN23

用途 APPLICATIONS

- 风扇 / Electric fan
- 电动工具 / Electrical tools

产品特性 FEATURES

- 信号高电平有效，兼容 3.3V 和 5V 的 MCU / Signal high level valid, compatible with 3.3v and 5V MCU
- 下臂 MOSFET 源极输出 / Lower arm MOSFET source electrode output
- 内置自举二极管 / Built-in bootstrap diode
- 内置防直通保护 / Built-in straight through protection
- 内置欠压保护 / Built-in undervoltage protection
- 内部集成温度检测输出 / Internal integrated temperature detection output
- 绝缘耐压 1500V / Resistant to high voltage 1500V

订货信息 ORDER MESSAGE

订货料号 Order number	产品信息 Product information			
	无卤-条管 Halogen-Free-Tube	无卤-编带 Halogen-Free-Reel	印记 Marking	封装 Package
2A01-0498-16	SPE02M50T-AN	N/A	SPE02M50T-AN	DIP23-FP
2A01-0469-16	SPE02M50T-CN	N/A	SPE02M50T-CN	SOP23-FP

模块分布示意图 Module distribution diagram

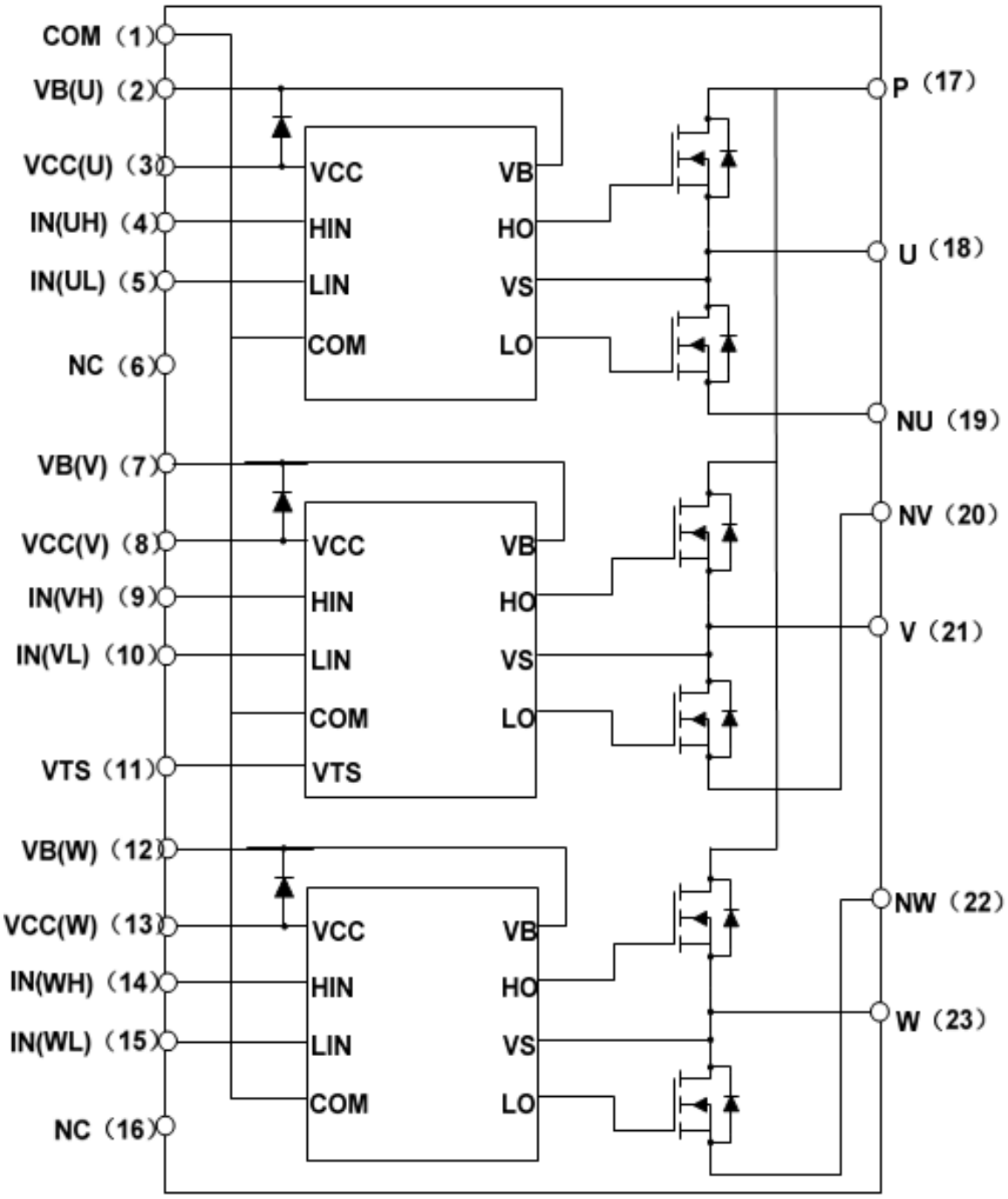


图 1：模块内部电路示意图

Fig 1: Internal circuit

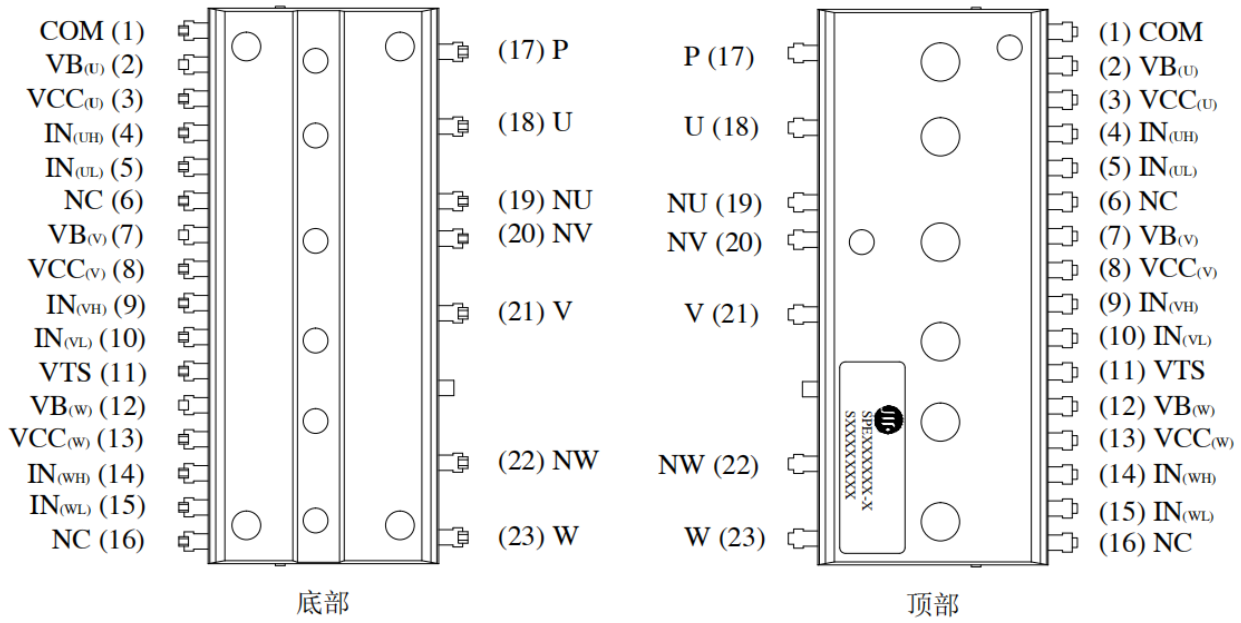


图 2：模块引脚分布示意图

Fig 2: Distribution of pin

引脚编号 Number	引脚名称 Name	引脚描述 Description
1	COM	控制电源 GND 端子 IC Common Supply Ground
2	VB(U)	U 相上臂驱动电源端子 Bias Voltage for U-Phase High-Side MOSFET Driving
3	VCC(U)	U 控制电源端子 Bias Voltage for U-Phase IC and Low-Side MOSFET Driving
4	IN(UH)	U 相上臂控制信号输入端子 Signal Input for U-Phase High-Side
5	IN(UL)	U 相下臂控制信号输入端子 Signal Input for U-Phase Low-Side
6	NC	无连接 No Connection
7	VB(V)	V 相上臂驱动电源端子 Bias Voltage for V-Phase High Side MOSFET Driving
8	VCC(V)	V 控制电源端子 Bias Voltage for V-Phase IC and Low Side MOSFET Driving
9	IN(VH)	V 相上臂控制信号输入端子 Signal Input for V-Phase High-Side
10	IN(VL)	V 相下臂控制信号输入端子 Signal Input for V-Phase Low-Side
11	NC	无连接 No Connection
12	VB(W)	W 相上臂驱动电源端子 Bias Voltage for W-Phase High-Side MOSFET Driving
13	VCC(W)	W 控制电源端子 Bias Voltage for W-Phase IC and Low-Side MOSFET Driving
14	IN(WH)	W 相上臂控制信号输入端子 Signal Input for W-Phase High-Side
15	IN(WL)	W 相下臂控制信号输入端子 Signal Input for W-Phase Low-Side
16	NC	无连接 No Connection
17	P	逆变器直流输入端子 Positive DC-Link Input
18	U	U 相输出端子 Output for U-Phase & Bias Voltage Ground for High-Side MOSFET Driving
19	NU	U 相下臂 MOSFET 源极端子 Negative DC-Link Input for U-Phase
20	NV	V 相下臂 MOSFET 源极端子 Negative DC-Link Input for V-Phase
21	V	V 相输出端子 Output for V-Phase & Bias Voltage Ground for High-Side MOSFET Driving
22	NW	W 相下臂 MOSFET 源极端子 Negative DC-Link Input for W-Phase
23	W	W 相输出端子 Output for W Phase & Bias Voltage Ground for High-Side MOSFET Driving

图 3：模块引脚功能定义表

Fig 3: Pin function

最大额定值（T_j= 25℃,除非特殊说明）
Absolute Maximum Ratings （T_j= 25℃, Unless otherwise Specified）

逆变部分 Inverter Part

记号 Symbol	参数 Parameter	条件 Condition	额定值 Ratings	单位 Units
V_{DSS}	漏-源电压 Drain-Source Voltage of Each MOSFET	/	500	V
I_D	漏极连续电流 Each MOSFET Current, Continuous	Tc=25℃（Tc 测量参考图 5） Tc=25℃（Tc refer to Fig:5）	1.2	A
I_{DM}	漏极电流（峰值） Each MOSFET Pulse Current, Peak	Tc=25℃, 脉冲宽度小于 100us Tc=25℃, less than 100us	3	A
I_{Drms}	漏极电流（有效值） Each MOSFET Current, Rms	Tc=25℃, F_{PWM}＜20KHz	0.85	Arms
P_D	最大功耗 Maximum Power Dissipation	Tc=25℃，每个 MOSFET Tc=25℃，For Each MOSFET	14.2	W

控制部分 Control Part

记号 Symbol	参数 Parameter	条件 Condition	额定值 Ratings	单位 Units
V_{CC}	控制电源电压 Control Supply Voltage	VCC-COM 之间 Applied between VCC and COM	20	V
V_{BS}	高侧控制电压 High-side Bias Voltage	VB-VS 之间 Applied between VB and VS	20	V
V_{IN}	输入信号电压 Input Signal Voltage	VIN-COM 之间 Applied between VIN and COM	-0.3~V_{CC}+0.3	V

整个系统 Total System

记号 Symbol	参数 Parameter	条件 Condition	额定值 Ratings	单位 Units
T_j	结温 Operating Junction Temperature	/	-40~150	℃
T_{STG}	贮存温度 Storage Temperature	Tc=25℃	-40~125	℃
V_{ISO}	绝缘耐压 Isolation Voltage	60Hz，正弦，AC 1 分钟，连接管脚到散热器 60Hz, Sinusoidal, AC 1 min, between pins and heat-sink plate	1500	V

备注 1：为了确保 IPM 正常工作，模块的结温应该小于 150℃(@Tc ≤ 100° C)。

NOTE 1：To insure safe operation of the IPM， the average junction temperature should be limited to TJ ≤ 150° C (@Tc ≤100° C).

热阻 Thermal Resistance

记号 Symbol	参数 Parameter	条件 Condition	额定值 Ratings	单位 Units
Rth(j-c)	结到外壳的热阻 Junction to Case Thermal resistance	每个 MOSFET For Each MOSFET	8.8	℃/W

电气特性 (Tj=25℃, 除非特殊说明)
Electrical Characteristics (TJ=25℃, Unless Otherwise Specified)

逆变部分 Inverter Part

记号 Symbol	参数 Parameter	条件 Condition	最小值 Min.	典型值 Typ.	最大值 Max.	单位 Unit
BV_{DSS}	漏-源击穿电压 Drain-Source Breakdown Voltage	V_{IN}=0V, I_D=1mA(备注 2) (Note2)	500	-	-	V
I_{DSS}	零栅极电压漏极电流 Zero Gate Voltage Drain Current	V_{IN}=0V, V_{DS}=500V	-	-	0.25	mA
V_{SD}	源-漏二极管正向电压 Drain-Source Diode Forward Voltage	V_{CC}=V_{BS}=15V, V_{IN}=0V, I_D=-0.5A	-	0.8	-	V
$R_{DS(on)}$	漏-源导通电 Drain-Source Turn-On Resistance	V_{CC}=V_{BS}=15V, V_{IN}=5V, I_D=0.5A	-	2.5	3.3	ohm
t_{ON}	开关时间 Switching Times	V_{PN}=300V, V_{CC}=V_{BS}=15V, ID=0.5A, VIN=0/5V, 感性负载(Inductive Load) L=3mH (备注 3) (Note3)	-	800	-	nS
t_{OFF}			-	450	-	nS
t_{rr}			-	200	-	nS
E_{ON}			-	38	-	uJ
E_{OFF}			-	8	-	uJ
$RBSOA$	反向偏置安全工作区 Reverse Bias Safe Operating Area	V_{PN}=400V, V_{CC}=V_{BS}=15V, I_D=I_{DP}, V_{DS}=BV_{DSS}, T=150℃	全直角 Full Square			

备注 2: BV_{DSS} 是单个 MOSFET 漏源最大电压。V_{PN} 应小于该值，考虑到杂散电感，V_{DS} 在任何情况下都不应超过 BV_{DSS} 。

NOTE 2: BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM®. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.

备注 3: t_{ON} 和 t_{OFF} 包含驱动 IC 传输延迟。列表值是在实验条件下测得，不同的 PCB 及连线会改变数值。请参考图 4 的开关时间定义。

NOTE 3: t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applcations due to the effect of different printed circuit boards and wirings. Please see Fig 4 for the switching time definition.

控制部分 Control Part

记号 Symbol	参数 Parameter	条件 Condition		最小值 Min.	典型值 Typ.	最大值 Max.	单位 Unit
I_{QCC}	V_{CC} 静态电流 Quiescent V_{CC} Supply Current	V_{CC}=15V V_{IN}=5V	V_{CC}-COM 之间 Applied between V_{CC} and COM	-	-	510	uA
I_{QB}	V_{BS} 静态电流 Quiescent V_{BS} Supply Current	V_{DB}=15V V_{IN}=5V	VB(U)-U, VB(V)-V, VB(W)-W 之间 Applied between VB(U)-U, VB(V)-V, VB(W)-W	-	-	210	uA
UV_{CCD}	低侧欠压保护 Low-Side Under-Voltage Protection	检测电平 V_{CC} Under-Voltage Protection Detection Level		7.4	8.4	9.4	V
UV_{CCR}		复位电平 V_{CC} Under-Voltage Protection Reset Level		8.0	8.9	9.8	V
UV_{BSD}	高侧欠压保护 High-Side Under-Voltage Protection	检测电平 V_{BS} Under-Voltage Protection Detection Level		7.4	8.4	9.4	V
UV_{BSR}		复位电平 V_{BS} Under-Voltage Protection Reset Level		8.0	8.9	9.8	V

V_{IH}	输入开启阈值电压 ON Threshold Voltage	逻辑高电平，加在 VIN 与 COM 之间 Logic HIGH Level, Applied between VIN and COM	-	-	2.9	V
V_{IL}	输入关闭阈值电压 OFF Threshold Voltage	逻辑低电平，加在 VIN 与 COM 之间 Logic Low Level, Applied between VIN and COM	0.8	-	-	V

推荐工作条件 Recommended Operating Conditions

记号 Symbol	参数 Parameter	记号 Symbol	最小值 Min.	典型值 Typ.	最大值 Max.	单位 Unit
V_{PN}	电源电压 Supply Voltage	P-N 之间 Applied between P and N	-	300	400	V
V_{CC}	控制电源电压 Control Supply Voltage	VCC-COM 之间 Applied between VCC and COM	13.5	15.0	16.5	V
V_{BS}	高侧控制电源电压 High-Side Bias Voltage	VB-VS 之间 Applied between VB and VS	13.5	15.0	16.5	V
$V_{IN(ON)}$	输入开启阈值电压 Input ON Threshold Voltage	VIN-COM 之间 Applied between VIN and COM	3.0	-	VCC	V
$V_{IN(OFF)}$	输入关闭阈值电压 Input OFF Threshold Voltage		0	-	0.6	V
t_{dead}	死区时间 Blanking Time for Preventing Arm-Shor	VCC=VBS=13.5~16.5V, Tj＜150℃	1.0	-	-	us
F_{PWM}	PWM 开关频率 PWM Switching Frequency	Tj＜150℃	-	15	-	KHz

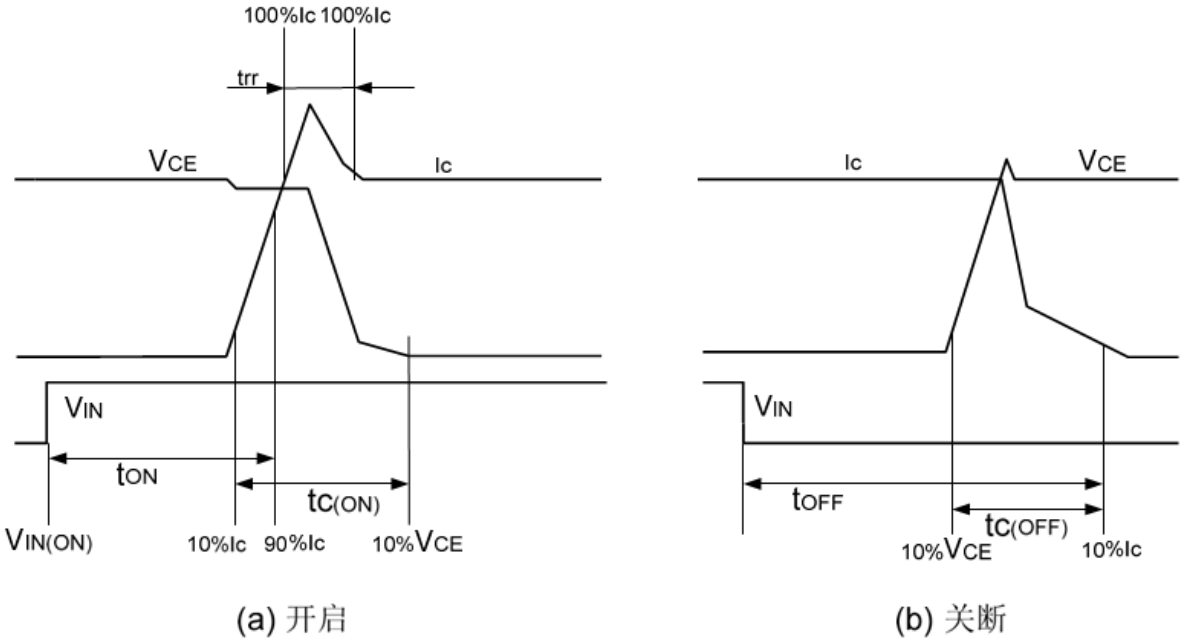


图 4：开关时间定义

Fig 4: Switching Time Definition

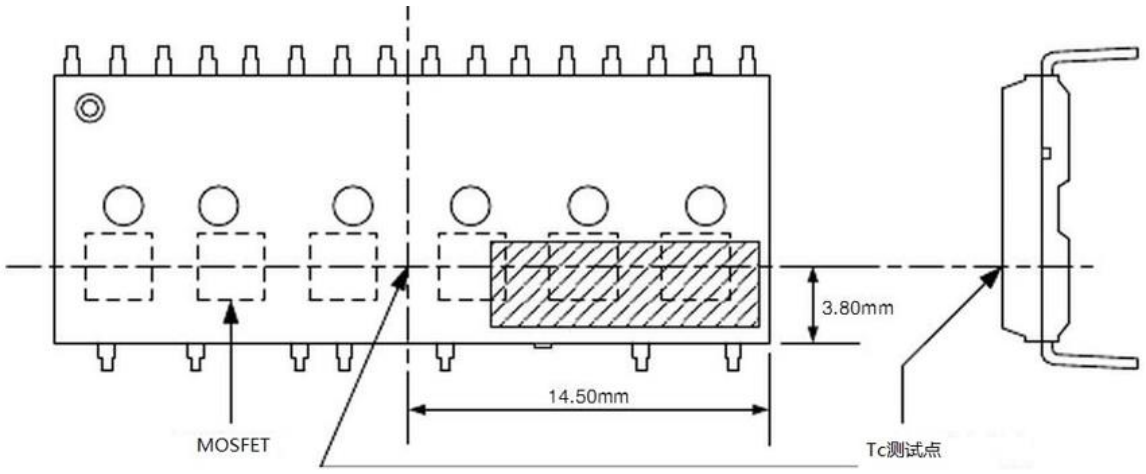


图 5：壳温 Tc 测试点

Fig 5：Case Temperature Measurement

保护功能时序图 Time Charts of Protective Function

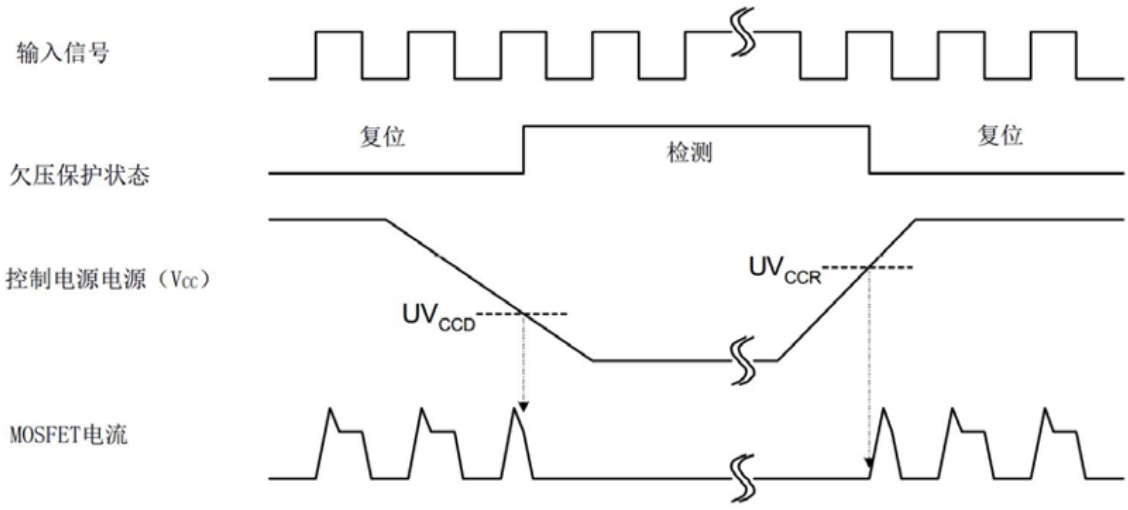


图 6：欠压保护时序图(低侧)

Fig 6：Undervoltage protection sequence diagram (low side)

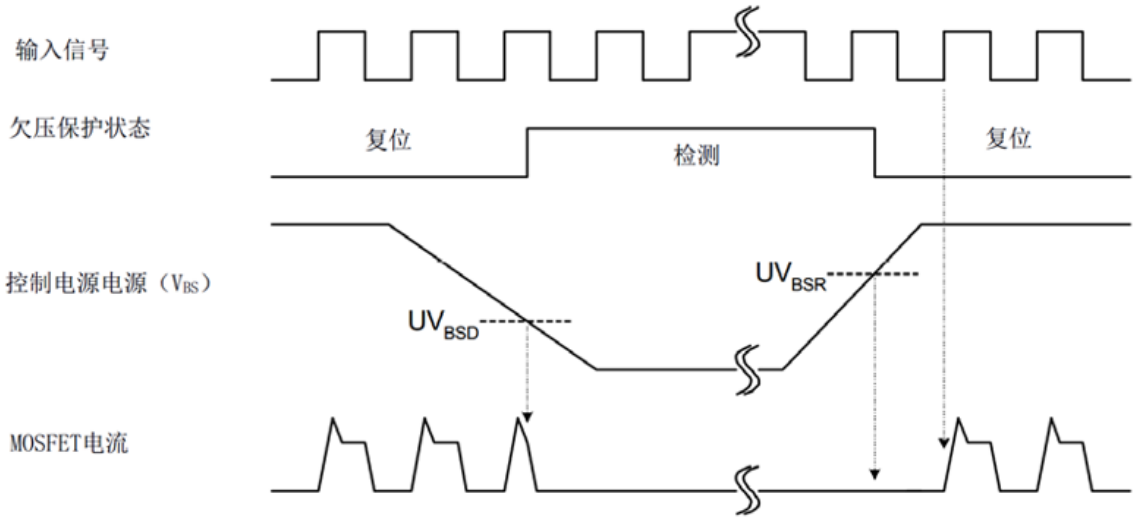
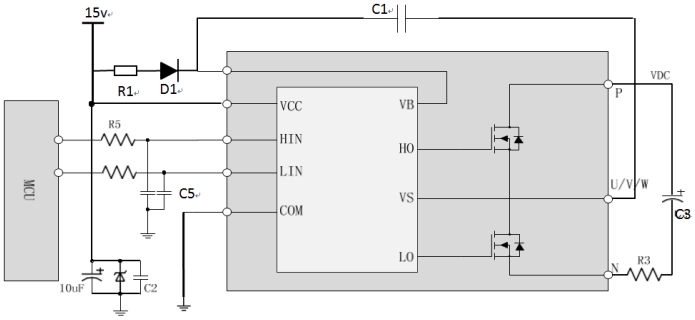


图 7：欠压保护时序图(高侧)

Fig 7：Undervoltage protection sequence diagram (High side)

应用电路 Application Circuit



HIN	LIN	逆变器输出	备注
0	0	高阻	上下桥MOS关闭
0	1	0	下桥MOS开通
1	0	VDC	上桥MOS开通
1	1	禁止	直通
开路	开路	高阻	上下桥MOS关闭

图 8：MCU 接口和自举推荐电路

Fig 8：Recommended CPU Interface and Bootstrap Circuit with Parameters

备注 4：在模块的每个输入端和 MCU 输出端之间加入 RC 去耦电路，如 R5、C5 和高频滤波电容。

NOTE 4：RC coupling(R5 and C5) at each input of SPM® and MCU may be used to prevent improper signal due to surge noise. Signal input of SPM® is compatible with standard CMOS or LSTTL outputs.

图 9：典型应用电路图

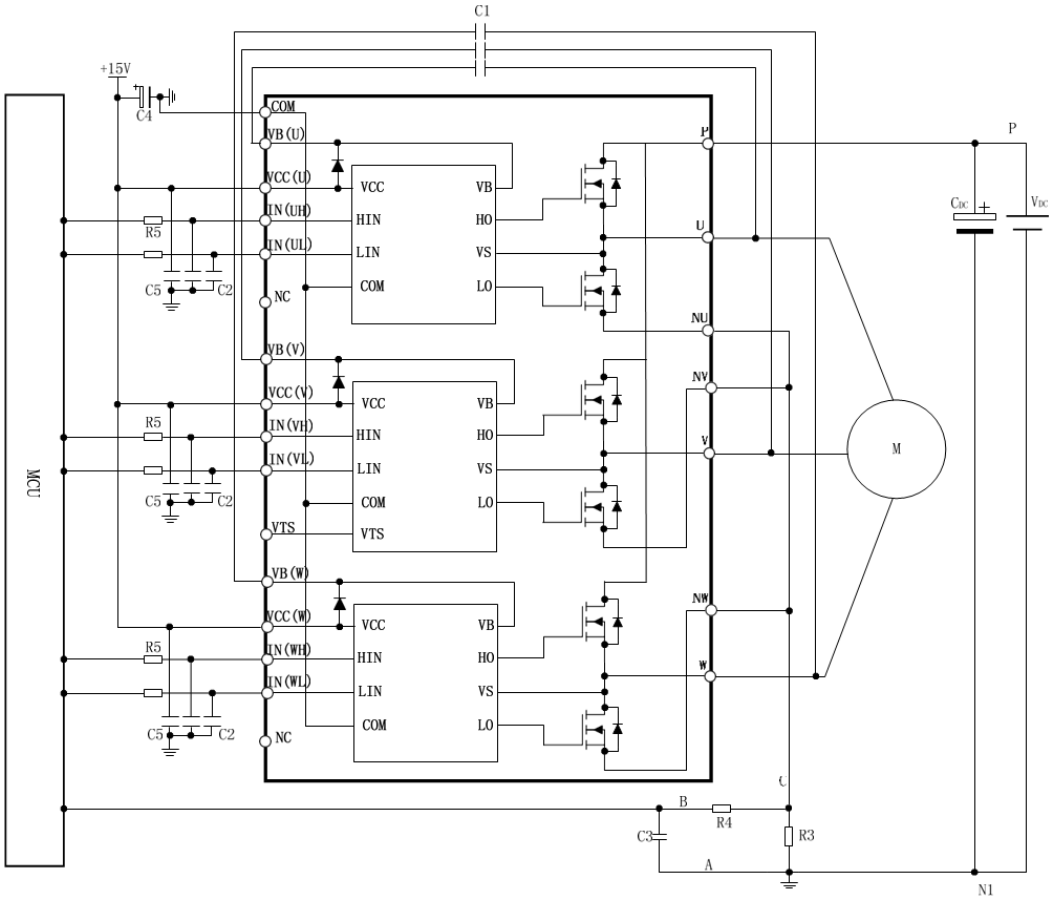


Fig 9：Example of Application Circuit

备注 5：输入驱动高有效；IC 内部集成有一个 500K（典型值)下拉电阻；为防止发生误动作， 输入布线应尽可能短；当用 RC 去耦线路时，须确保输入信号达到开启和关断阈值电压范围。

NOTE 5：Input drive is High-Active type. There is a 500kΩ(typ.) pull-down resistor integrated in the IC input circuit.To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

备注 6：由于 R3 位于 MOSFET 源极与 COM 之间，R3 的压降会影响到下侧 MOSFET 的开关特性以及自举电路的特性因此 R3 的稳态压降应小于 1V。

NOTE 6：The voltage drop across R3 affects the low side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low side MOSFET. For this reason, the voltage drop across R3 should be less than 1V in the steady-state.

备注 7：由于模块内置了专用 HVIC，其控制端子可与 CPU 端子直接相连，而不需要任何光耦或变压器等隔离电路。

NOTE 7：Thanks for HVIC inside modules, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

备注 8：为防止误保护，A、B、C 连线应尽可能短。

NOTE 8：To prevent erroneous protection, the wiring of A,B,C should be as short as possible.

备注 9：保护线路 R4、C3 的时间常数建议选取在 1~2uS。关断时间可能随着布线的不同而多少有些变化。建议 R4、C3 选择小容差，温度补偿类型。

NOTE 9：The time constant R4、C3 of the protection circuit should be selected in the range of 1.0-2 μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R4, C3.

备注 10：所有电容的位置尽可能的靠近 IPM。

NOTE 10：All capacitors should be mounted as close to the terminals of the IPM as possible.

备注 11：为了防止噪声干扰，储能电容与 P&N1 之间的引线应尽可能的短，推荐在 P&N1 端子之间加约 0.1～0.22uF 的 MLCC 低频滤波电容。

NOTE 11：To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally, a 0.1-0.22μF snubber between the P-N1 terminals is recommended.

外形封装图 Detailed Package Outline Drawings

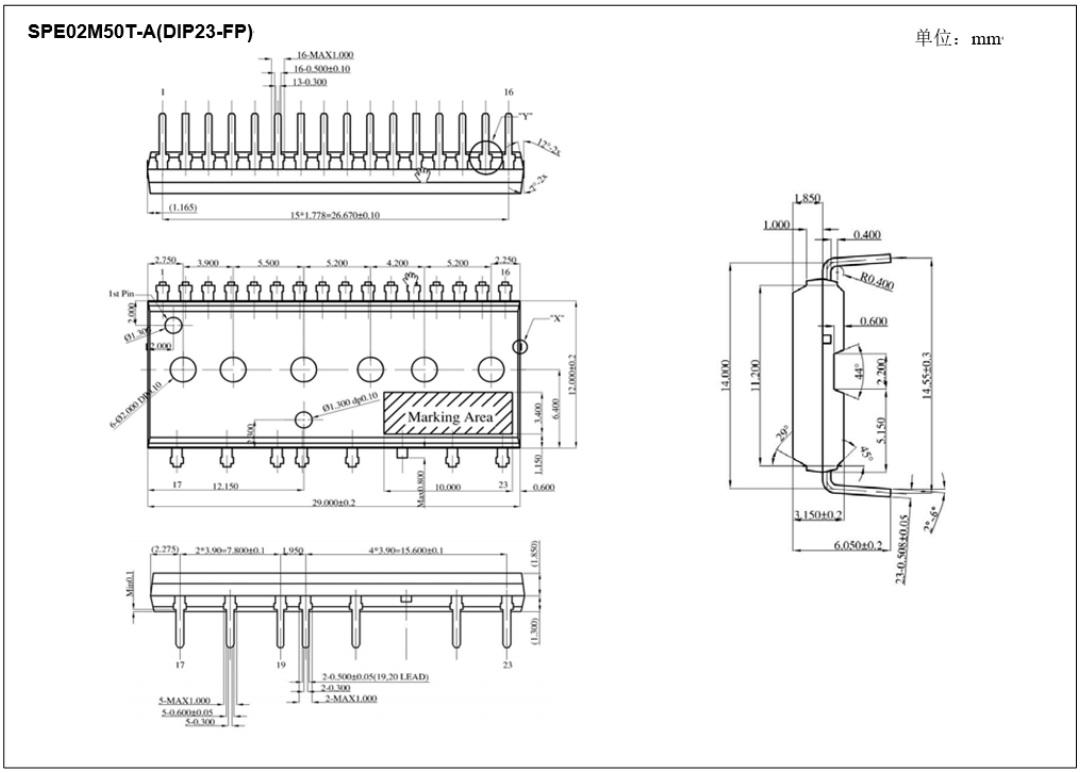


图 10：SPE02M50T-A 封装外形图　　Fig10：SPE02M50T-A Package Outline Drawings

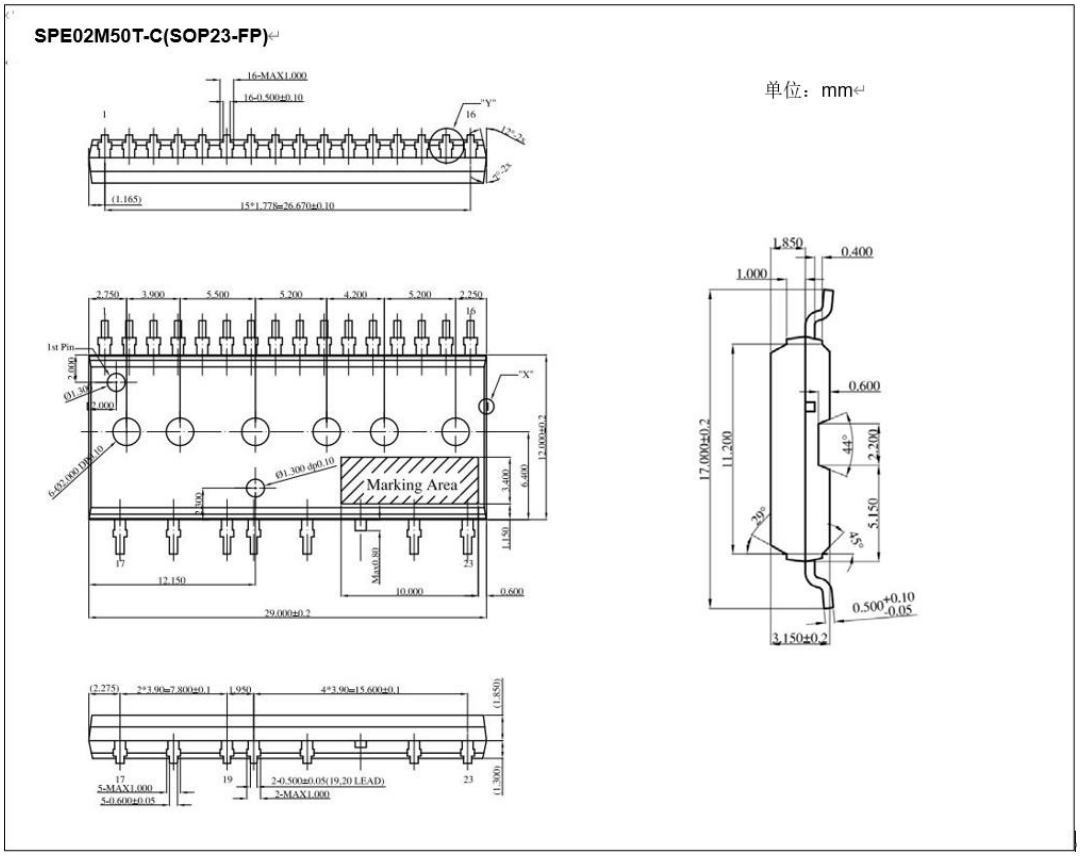


图 11：SPE02M50T-C 封装外形图　　Fig 11：SPE02M50T-C Package Outline Drawings

注意事项

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2. 购买时请认清公司商标，如有疑问请与公司本部联系。
3. 在电路设计时请不要超过器件的绝对最大额定值，否则会影响整机的可靠性。
4. 本说明书如有版本变更不另外告知。

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2. We strongly recommend customers check carefully on the trademark when buying our product, if there is any question, please don't be hesitate to contact us.
3. Please do not exceed the absolute maximum ratings of the device when circuit designing.
4. Jilin Sino-microelectronics co., Ltd reserves the right to make changes in this. specification sheet and is subject to change without prior notice.

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