512Kx8 Monolithic SRAM, CMOS

FEATURES

- 512Kx8 bit CMOS Static
- Random Access Memory
  - Access Times of 70, 85, 100ns
  - Data Retention Function (LP version)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- 32 lead JEDEC Approved Evolutionary Pinout
  - Ceramic Sidebrazed 600 mil DIP (Package 9)
  - Ceramic SOJ (Package 140)
- Single +5V (±10%) Supply Operation

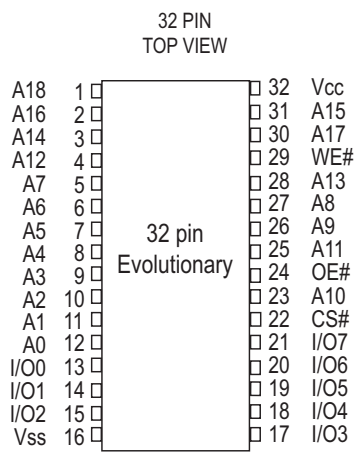
The EDI88512C is a 4 megabit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the four megabit device. Both the DIP and CSOJ packages are pin for pin upgrades for the single chip enable 128K x 8, the EDI88128C. Pins 1 and 30 become the higher order addresses.

A Low Power version with Data Retention (EDI88512LP) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

* This product is subject to change without notice.

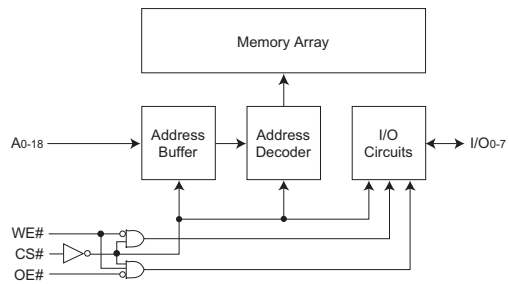
FIGURE 1 – PIN CONFIGURATION



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-18	Address Inputs
WE#	Write Enables
CS#	Chip Selects
OE#	Output Enable
V_{CC}	Power (+5V ±10%)
V_{SS}	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature T_A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

OE#	CS#	WE#	Mode	Output	Power
X	H	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	Output Deselect	High Z	I_{CC1}
L	L	H	Read	Data Out	I_{CC1}
X	L	L	Write	Data In	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.5	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Address Lines	C_I	V_{IN} = Vcc or Vss, f = 1.0MHz	12	pF
Data Lines	C_O	V_{OUT} = Vcc or Vss, f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

V_{CC} = 5V, -55°C ≤ *T_A ≤ +125°C

Parameter	Symbol	Conditions		Min	Typ*	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		—	—	±10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}		—	—	±10	µA
Operating Power Supply Current	I_{CC1}	WE#, CS# = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle (70-100ns)		—	45	75	mA
Standby (TTL) Power Supply Current	I_{CC2}	CS# ≥ V_{IH}, V_{IN} ≤ V_{IL}, V_{IN} ≥ V_{IH}		—	3	10	mA
Full Standby Power Supply Current	I_{CC3}	CS# ≥ V_{CC} -0.2V	C	—	—	5	mA
		V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V	LP	—	—	2	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4	—	—	V

NOTE: DC test conditions: Vil = 0.3V, Vih = Vcc -0.3V

AC TEST CONDITIONS

Figure 1

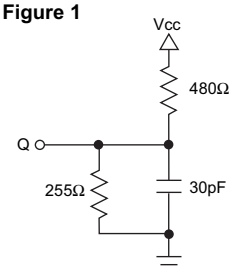
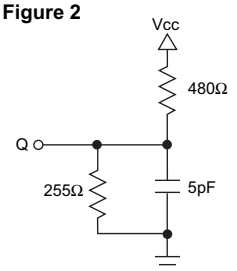


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2

AC CHARACTERISTICS – READ CYCLE

V_{CC} = 5.0V, Vss = 0V, -55°C ≤ T_A ≤ +125°C

	Symbol		70ns		85ns		100ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	t_{AVAV}	t_{RC}	70		85		100		ns
Address Access Time	t_{AVQV}	t_{AA}		70		85		100	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		70		85		100	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	10		10		10		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		25		30		30	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	10		10		10		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		35		45		50	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	5		5		5		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}	0	25	0	30	0	30	ns

1. This parameter is guaranteed by design but not tested.

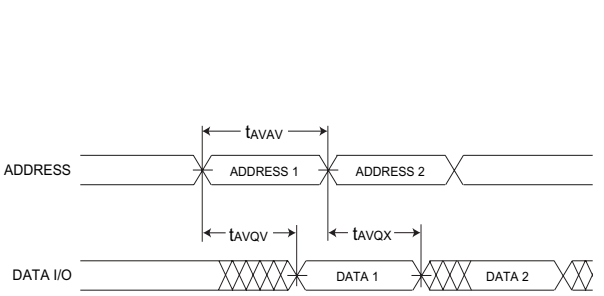
AC CHARACTERISTICS – WRITE CYCLE

V_{CC} = 5.0V, V_{SS} = 0V, -55°C≤ T_A ≤ +125°C

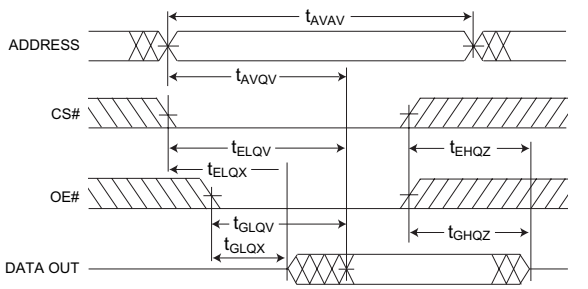
	Symbol		70ns		85ns		100ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	t_{AVAV}	t_{WC}	70		85		100		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	60		70		80		ns
	t_{ELEH}	t_{CW}	60		70		80		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	65		70		80		ns
	t_{AVEH}	t_{AW}	65		70		80		ns
Write Pulse Width	t_{WLWH}	t_{WP}	50		55		60		ns
	t_{WLEH}	t_{WP}	50		55		60		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		ns
	t_{EHAX}	t_{WR}	0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	25	0	30	0	30	ns
Data to Write Time	t_{DVWH}	t_{DW}	40		40		40		ns
	t_{DVEH}	t_{DW}	30		35		40		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	5		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIGURE 2 – TIMING WAVEFORM - READ CYCLE

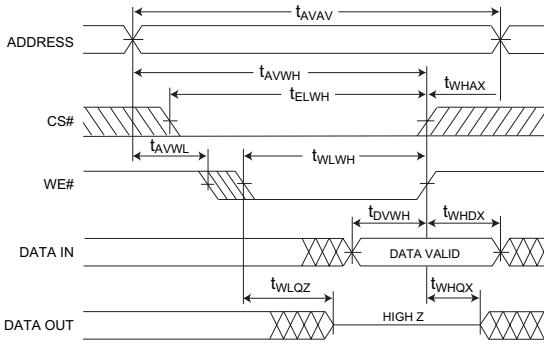


READ CYCLE 1 (WE# HIGH; OE#, CS# LOW)



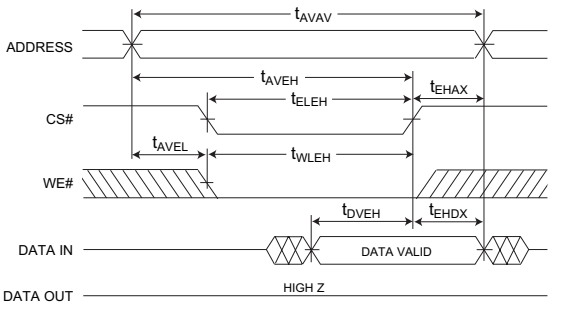
READ CYCLE 2 (WE# HIGH)

FIGURE 3 – WRITE CYCLE - WE# CONTROLLED



WRITE CYCLE 1, WE# CONTROLLED

FIGURE 4 – WRITE CYCLE - CS# CONTROLLED



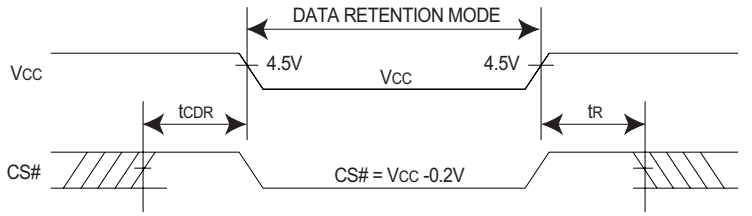
WRITE CYCLE 2, CS# CONTROLLED

DATA RETENTION CHARACTERISTICS (EDI88512LP ONLY)

-55°C ≤ T_A ≤ +125°C

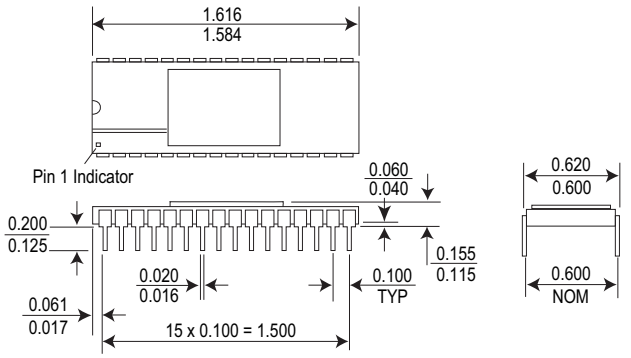
Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{CC}	V_{CC} = 2.0V	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	CS# ≥ V_{CC} -0.2V	–	–	185	µA
Chip Disable to Data Retention Time	t_{CDR}	V_{IN} ≥ V_{CC} -0.2V	0	–	–	ns
Operation Recovery Time	T_R	or V_{IN} ≤ 0.2V	t_{AVAV}	–	–	ns

FIGURE 5 – DATA RETENTION - CS# CONTROLLED



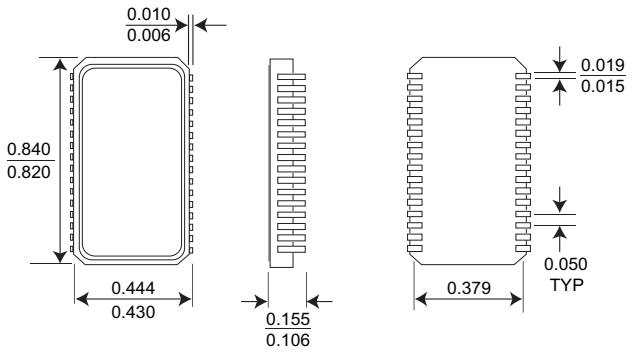
DATA RETENTION, CS# CONTROLLED

PACKAGE 9: 32 LEAD SIDEBRAZED CERAMIC DIP



ALL DIMENSIONS ARE IN INCHES

PACKAGE 140: 32 LEAD CERAMIC SOJ



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8512 C X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 512Kx8

TECHNOLOGY:
- C = CMOS Standard Power
- LP = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
- C = 32 lead Sidebrazed DIP, 600 mil (Package 9)
- N = 32 lead Ceramic SOJ (Package 140)

DEVICE GRADE:
- B = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C