CSD19538Q3A 100V、N 通道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 无铅
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

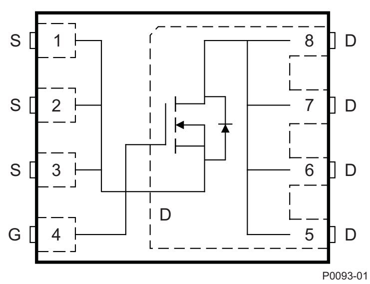
2 应用范围

- 以太网供电 (PoE)
- 电源设备 (PSE)
- 电机控制

3 说明

这款 100V、49mΩ、SON 3.3mm × 3.3mm NexFET™功率金属氧化物半导体场效应晶体管 (MOSFET) 旨在以最大限度降低导通损耗并减小以太网供电 (PoE) 应用中的电路板 尺寸。

俯视图



产品概要

T_A=25°C		典型值		单位
V_{DS}	漏源电压	100		V
Q_g	栅极电荷总量 (10V)	4.3		nC
Q_{gd}	栅极电荷 栅极到漏极	0.8		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	58	mΩ
		V_{GS} = 10V	49	
$V_{GS(th)}$	阈值电压	3.2		V

器件信息(1)

器件	包装介质	数量	封装	运输
CSD19538Q3A	13 英寸卷带	3000	小外形尺寸无引线 (SON) 3.30mm × 3.30mm 塑料封装	卷带封装
CSD19538Q3AT	7 英寸卷带	250		

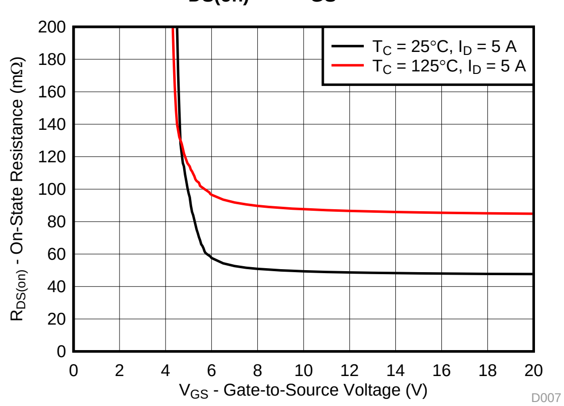
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

绝对最大额定值

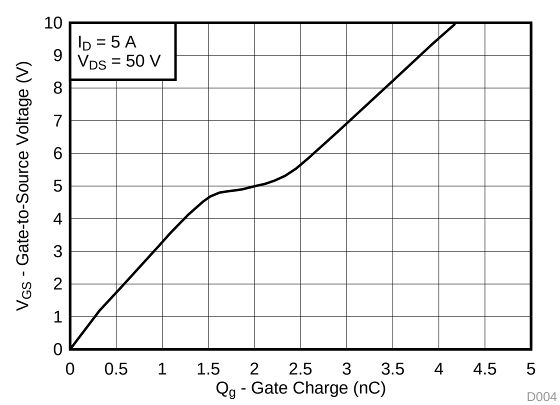
T_A=25°C		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	15	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	14	
	持续漏极电流(1)	4.9	
I_{DM}	脉冲漏极电流(2)	37	A
P_D	功率耗散(1)	2.8	W
	功率耗散，T_C = 25°C	23	
T_J，T_{stg}	工作结温，储存温度	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 12.7A，L = 0.1mH，R_G = 25Ω	8.1	mJ

(1) $R_{\theta JA}$ = 45°C/W，这是一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司铜焊盘上测得的典型值。
(2) 最大 $R_{\theta JC}$ = 5.5°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



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4 修订历史记录

Changes from Original (May 2016) to Revision A **Page**

- 已更改 把栅极电荷曲线中的测试电压 V_{DS}从 100V 更改为 50V 1
- Changed the test voltage V_{DS} in Figure 4 from 100 V : to 50 V 5
- 已添加 *接收文档更新通知*部分添加到*器件和文档支持*部分 7

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C

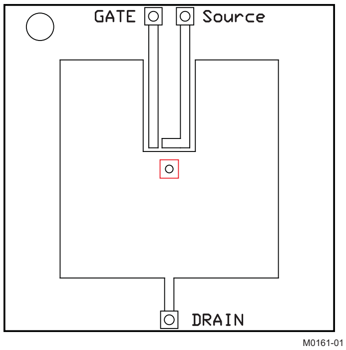
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 80 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.8	3.2	3.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 6 V, I_D = 5 A		58	72	mΩ
		V_{GS} = 10 V, I_D = 5 A		49	59	mΩ
g_{fs}	Transconductance	V_{DS} = 10 V, I_D = 5 A		6.1		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V, ƒ = 1 MHz		349	454	pF
C_{oss}	Output capacitance			69	90	pF
C_{rss}	Reverse transfer capacitance			12.6	16.4	pF
R_G	Series gate resistance			4.6	9.2	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 50 V, I_D = 5 A		4.3		nC
Q_{gd}	Gate charge gate-to-drain			0.8		nC
Q_{gs}	Gate charge gate-to-source			1.6		nC
$Q_{g(th)}$	Gate charge at V_{th}			1		nC
Q_{oss}	Output charge	V_{DS} = 50 V, V_{GS} = 0 V		12.3		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 50 V, V_{GS} = 10 V, I_{DS} = 5 A, R_G = 0 Ω		5		ns
t_r	Rise time			3		ns
$t_{d(off)}$	Turnoff delay time			7		ns
t_f	Fall time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 5 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50 V, I_F = 5 A, di/dt = 300 A/μs		94		nC
t_{rr}	Reverse recovery time			32		ns

5.2 Thermal Information

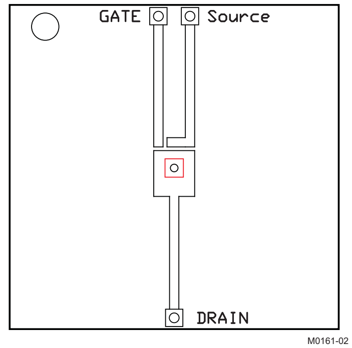
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJC}$	Junction-to-case thermal resistance(1)			5.5	°C/W
$R_{θJA}$	Junction-to-ambient thermal resistance(1)(2)			55	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 55°C/W when mounted on 1-in^2 (6.45-cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 195°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

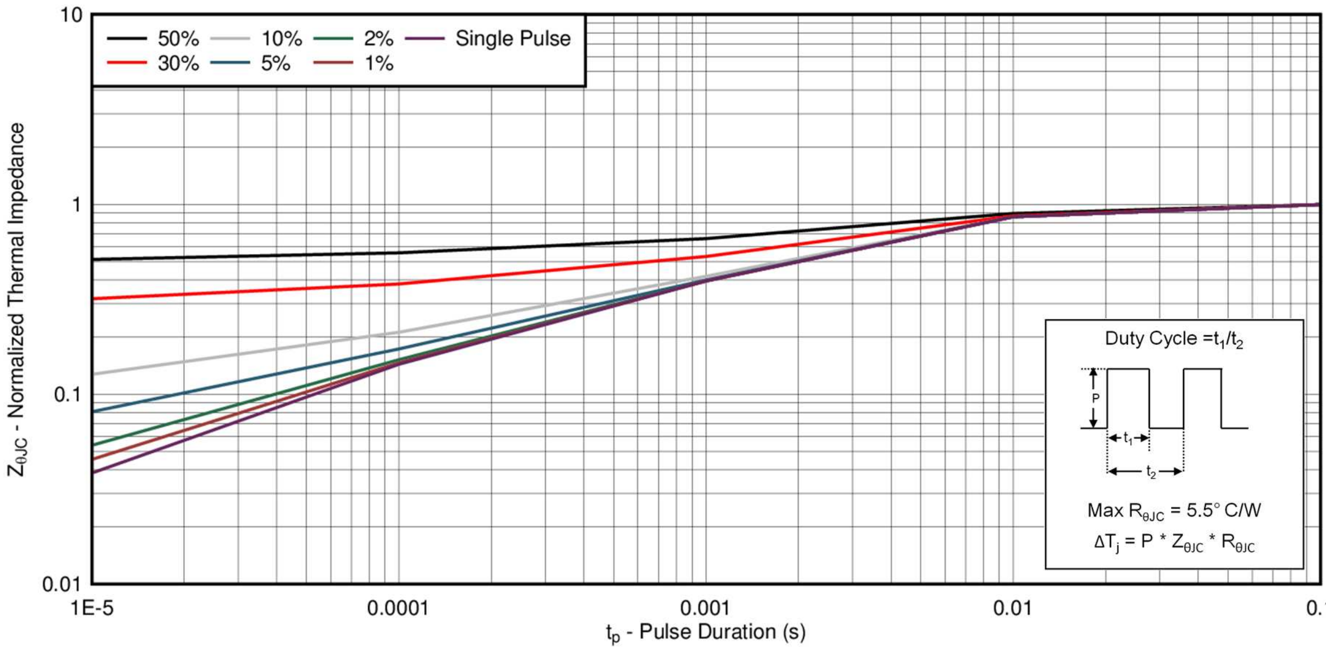


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

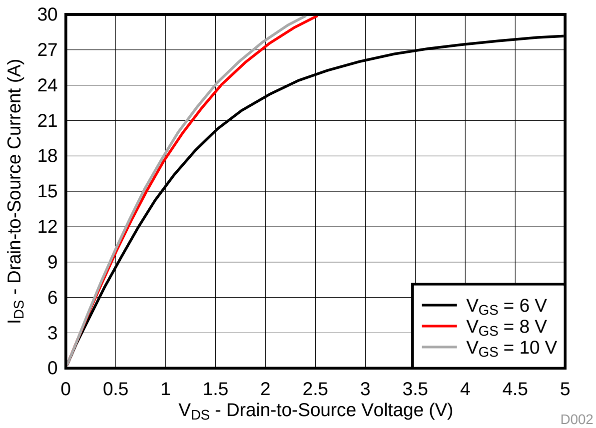


Figure 2. Saturation Characteristics

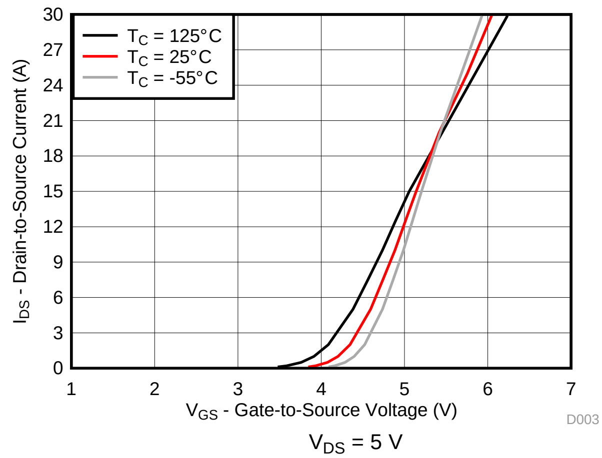


Figure 3. Transfer Characteristics

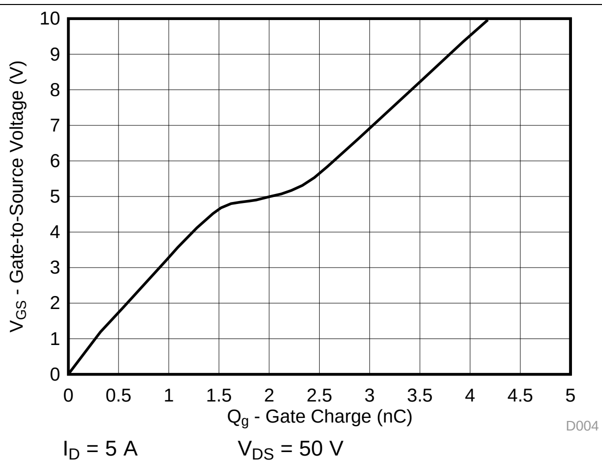


Figure 4. Gate Charge

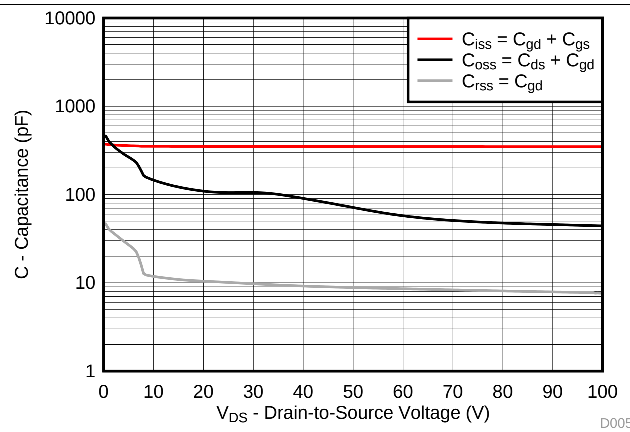


Figure 5. Capacitance

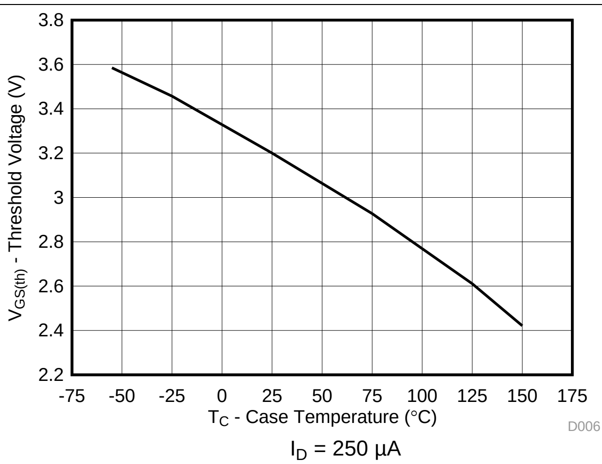


Figure 6. Threshold Voltage vs Temperature

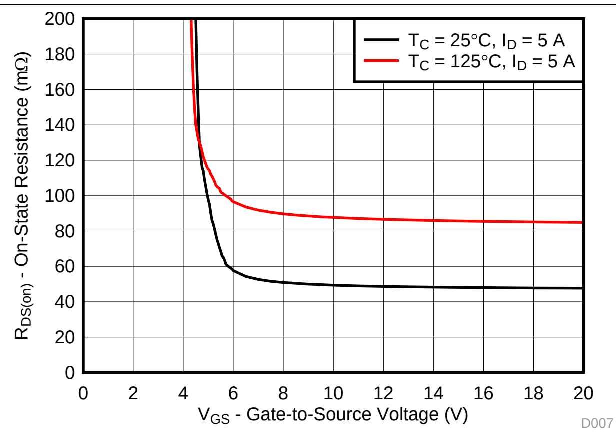
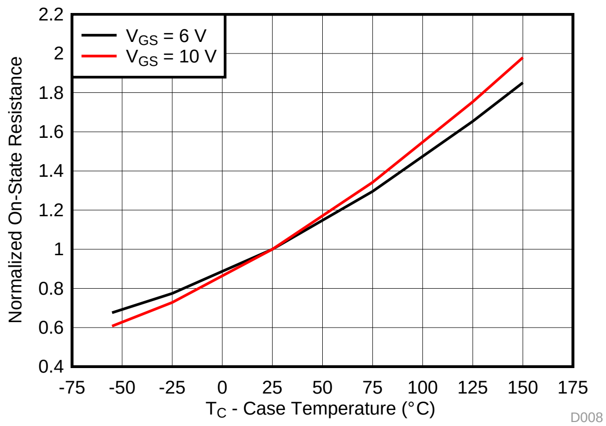


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = 5 A

Figure 8. Normalized On-State Resistance vs Temperature

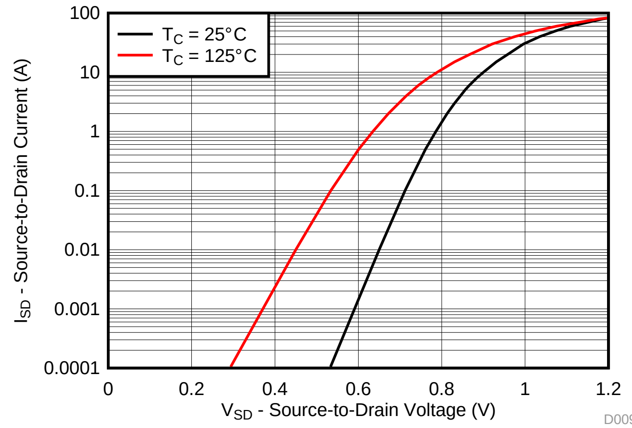
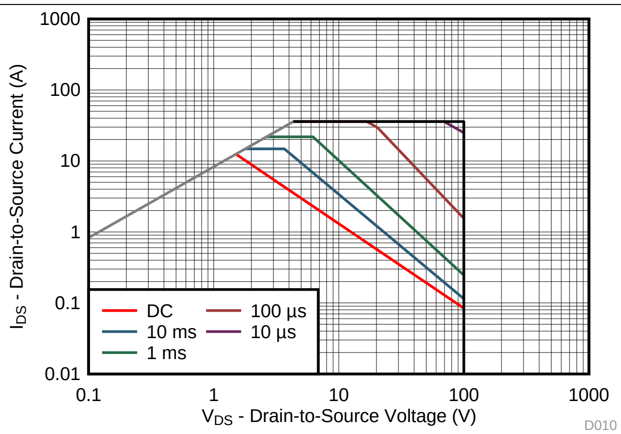


Figure 9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 5.5°C/W

Figure 10. Maximum Safe Operating Area

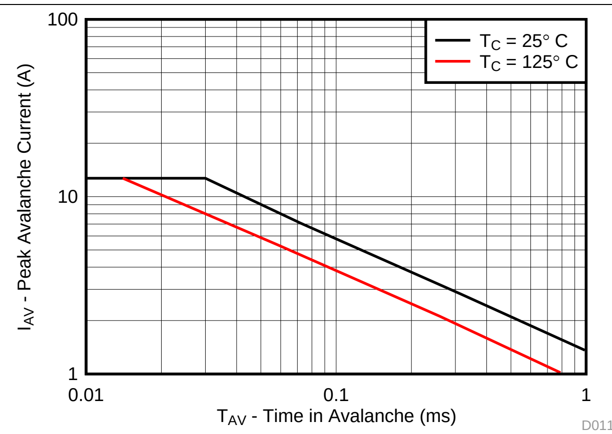


Figure 11. Single Pulse Unclamped Inductive Switching

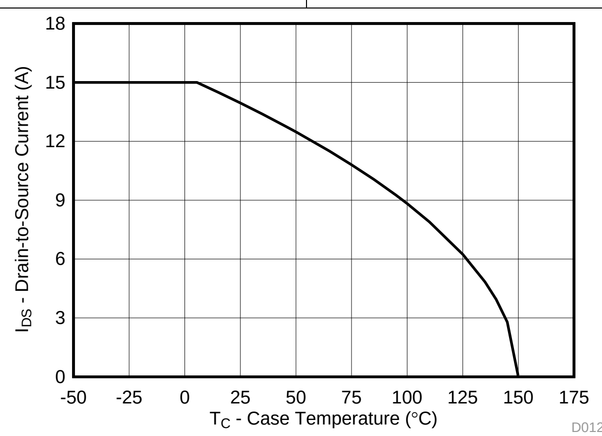


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

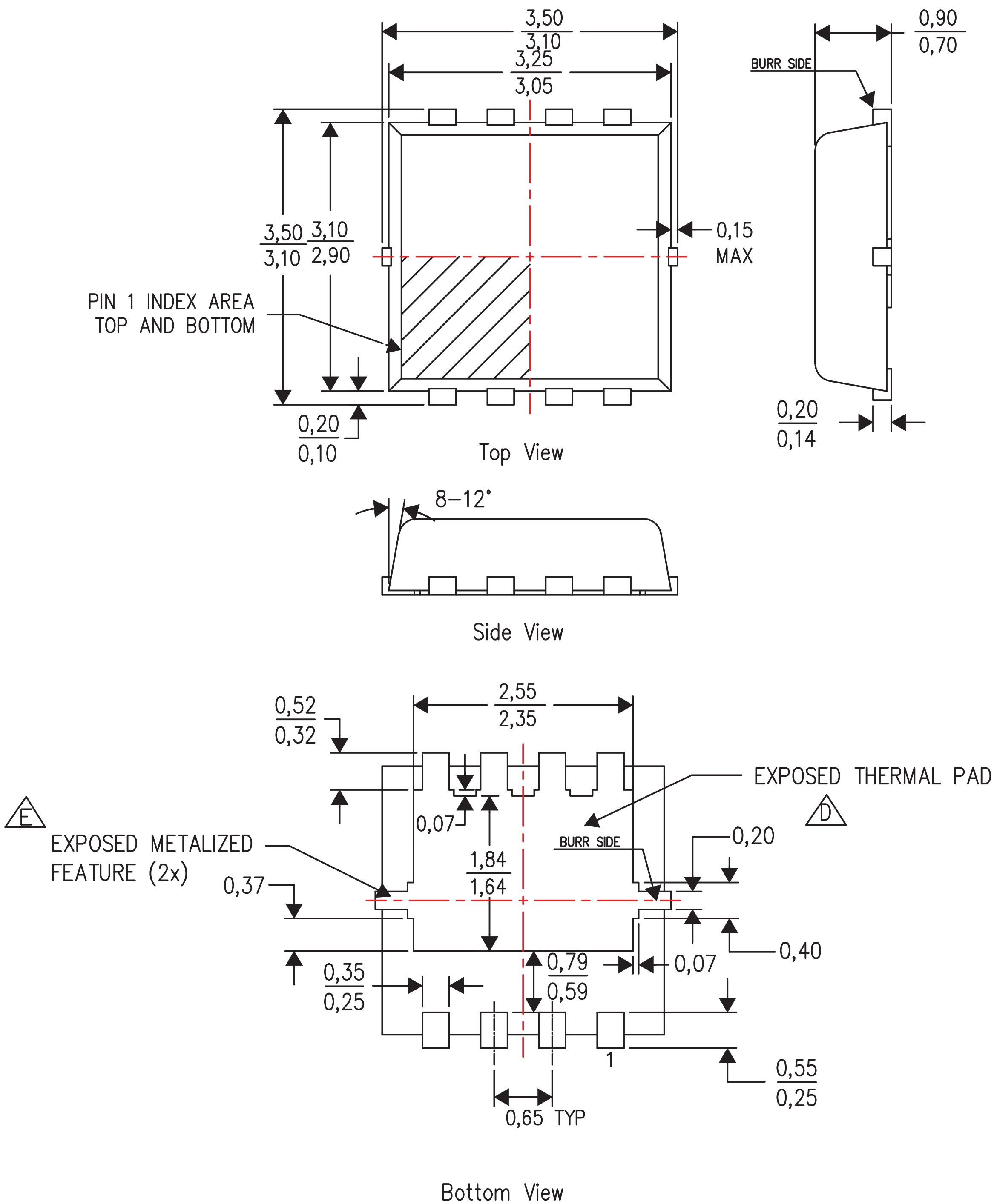
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

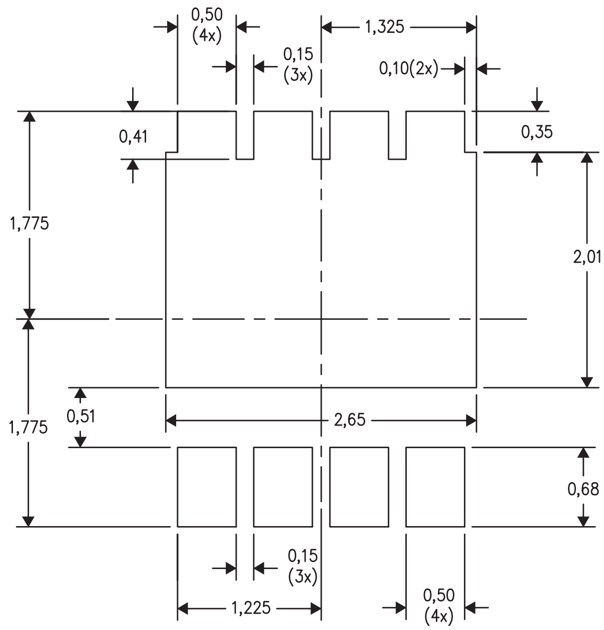
7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q3A 封装尺寸

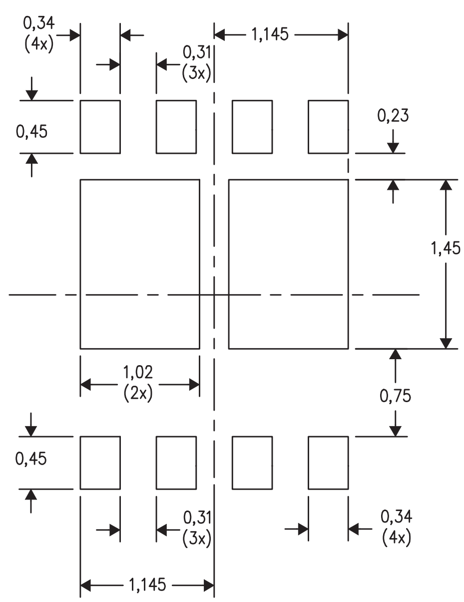


7.2 Q3A 建议的 PCB 布局

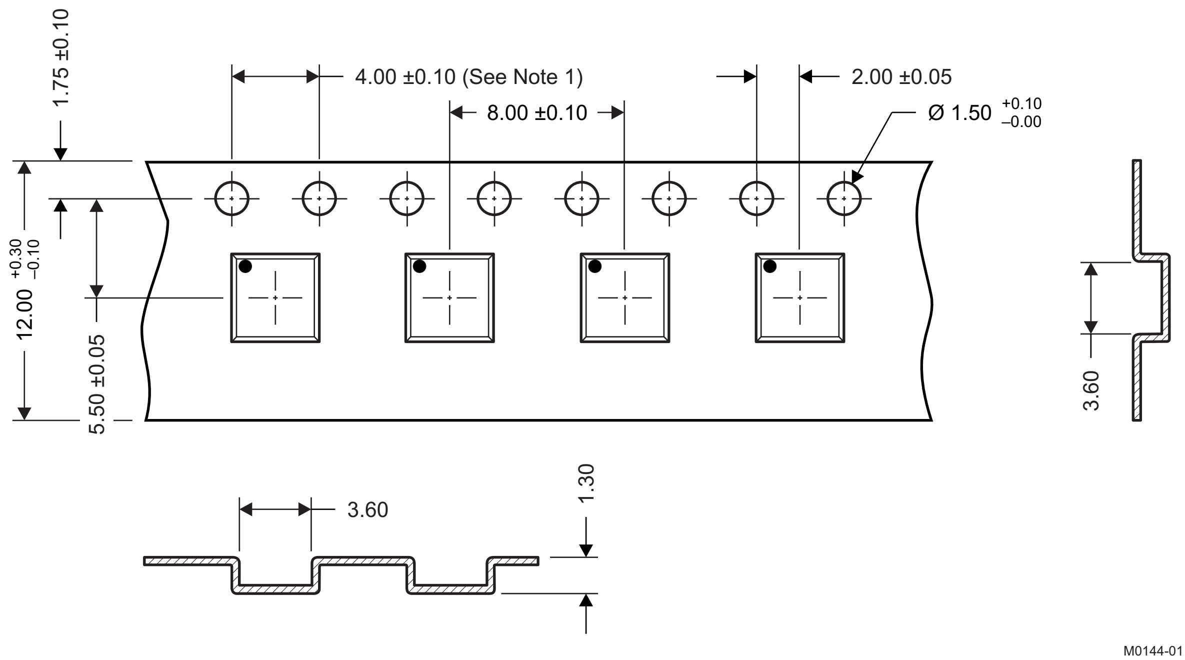


有关针对 PCB 设计的建议电路布局布线，请参见*《通过 PCB 布局布线技巧来减少振铃》*（文献编号：SLPA005）。

7.3 Q3A 建议的模板布局



7.4 Q3A 卷带信息



Notes: 1. 10 链轮孔距累积容差为 ±0.2

2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。

3. 材料：黑色抗静电聚苯乙烯。

4. 所有尺寸单位均为 mm，除非另外注明。

5. 厚度：0.3 ± 0.05mm。

6. MSL1 260°C（红外和对流）PbF 回流焊兼容。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19538Q3A	ACTIVE	VSONP	DNH	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	19538	Samples
CSD19538Q3AT	ACTIVE	VSONP	DNH	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	19538	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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