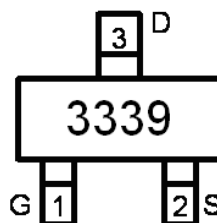
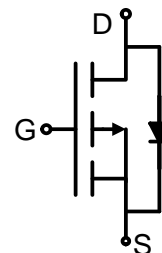


Main Product Characteristics:

V_{DSS}	-30V
$R_{DS(on)}$	37m Ω (typ.)
I_D	-4.1A ①


SOT-23

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating: @ $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	-4.1 ①	A
I_D @ TC = 70°C	Continuous Drain Current, V_{GS} @ 10V	-3.5 ①	
I_{DM}	Pulsed Drain Current ②	-20	
P_D @TC = 25°C	Power Dissipation ③	1.4	W
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

Thermal Resistance

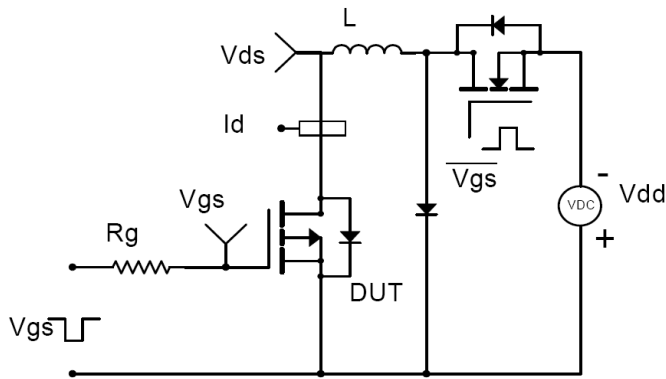
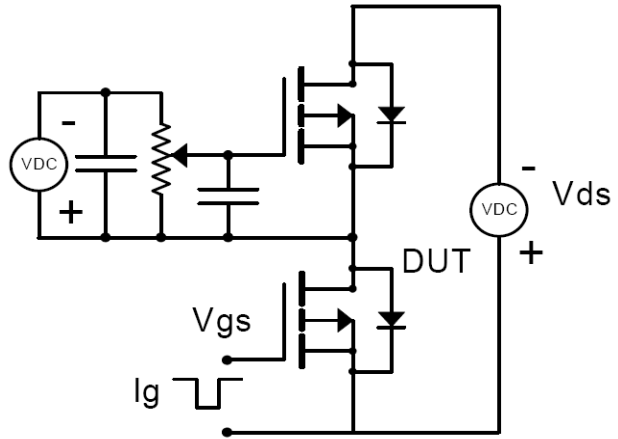
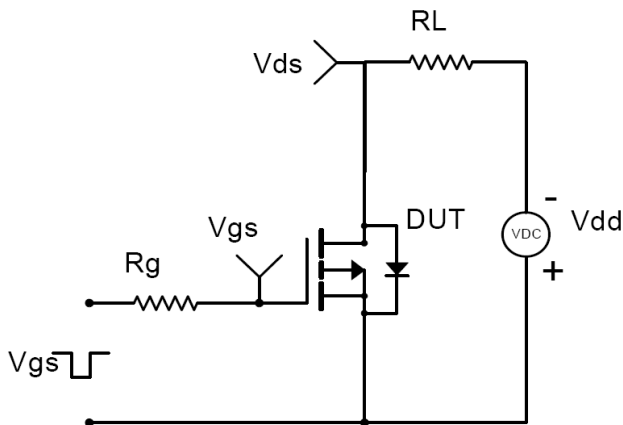
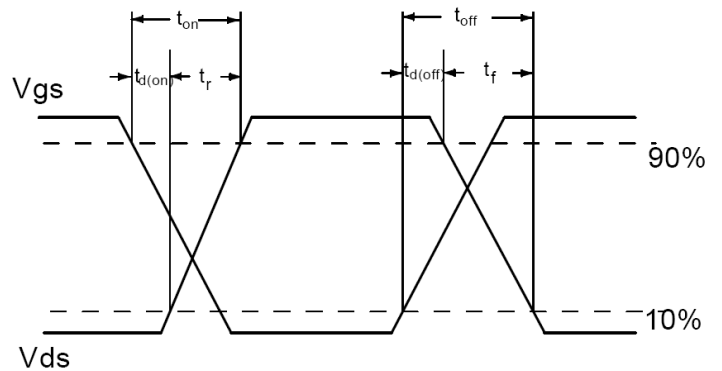
Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-ambient (t \leq 10s) ④	—	90	°C/W

Electrical Characterizes @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	37	52	m Ω	$V_{GS}=-10V, I_D = -4.1A$
		—	54	87		$V_{GS}=-4.5V, I_D = -3A$
$V_{GS(th)}$	Gate threshold voltage	-1	—	-3	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
		—	-1.4	—		$T_J = 125^{\circ}\text{C}$
I_{DSS}	Drain-to-Source leakage current	—	—	-1	μA	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-50		$T_J = 125^{\circ}\text{C}$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
Q_g	Total gate charge	—	17	—	nC	$I_D = -6A,$ $V_{DS}=-25V,$ $V_{GS} = -10V$
Q_{gs}	Gate-to-Source charge	—	2.5	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	5.0	—		
$t_{d(on)}$	Turn-on delay time	—	7.2	—	ns	$V_{GS}=-10V, V_{DS}=-25V,$ $R_{GEN}=3\Omega,$
t_r	Rise time	—	4.8	—		
$t_{d(off)}$	Turn-Off delay time	—	24	—		
t_f	Fall time	—	11	—		
C_{iss}	Input capacitance	—	665	—	pF	$V_{GS} = 0V,$ $V_{DS} = -15V,$ $f = 1\text{MHz}$
C_{oss}	Output capacitance	—	108	—		
C_{riss}	Reverse transfer capacitance	—	83	—		

Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-4.1 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)	—	—	-20	A	
V_{SD}	Diode Forward Voltage	—	-0.79	-1.0	V	$I_S=1A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	9.7	—	ns	$T_J = 25^{\circ}\text{C}, I_F = -6A,$
Q_{rr}	Reverse Recovery Charge	—	3.8	—	nC	$di/dt = 100A/\mu s$

Test circuits and Waveforms
EAS test circuit:

Gate charge test circuit:

Switching time test circuit:

Switch Waveforms:

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical electrical and thermal characteristics

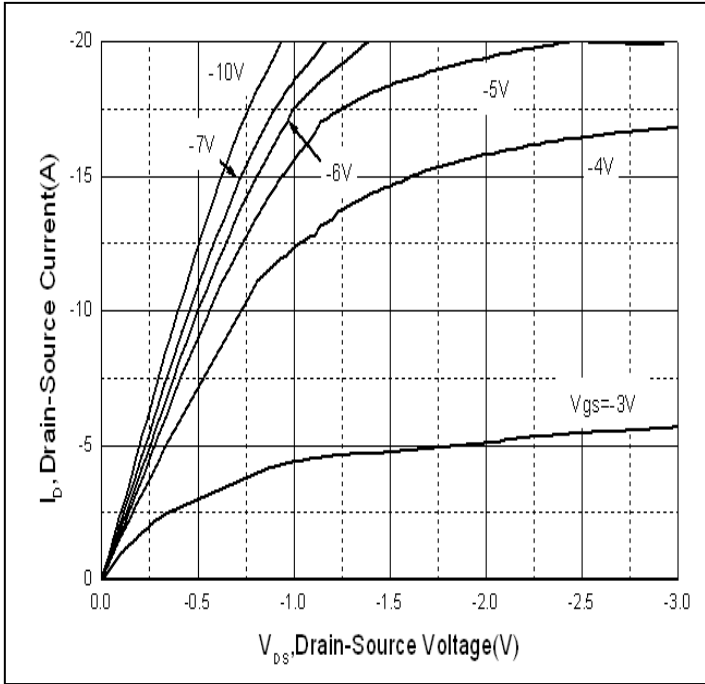


Figure 1: Typical Output Characteristics

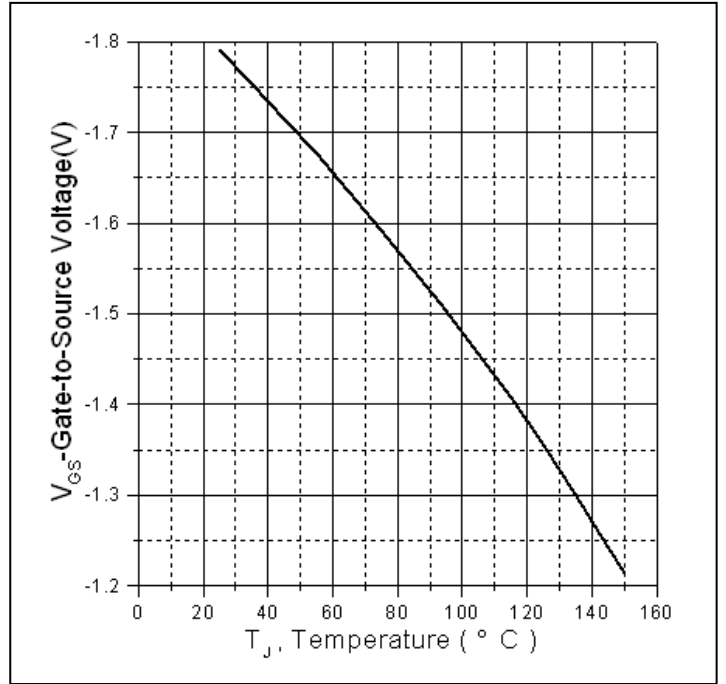


Figure 2. Gate to source cut-off voltage

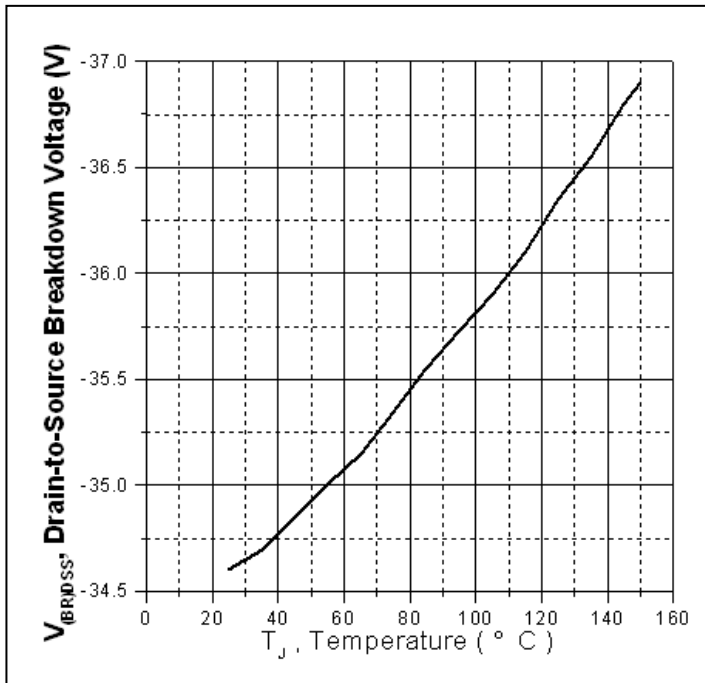


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

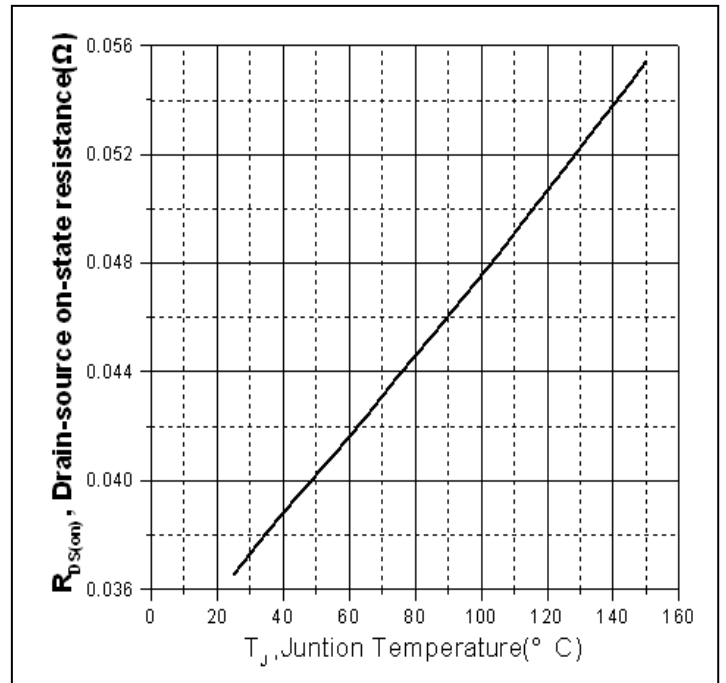


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

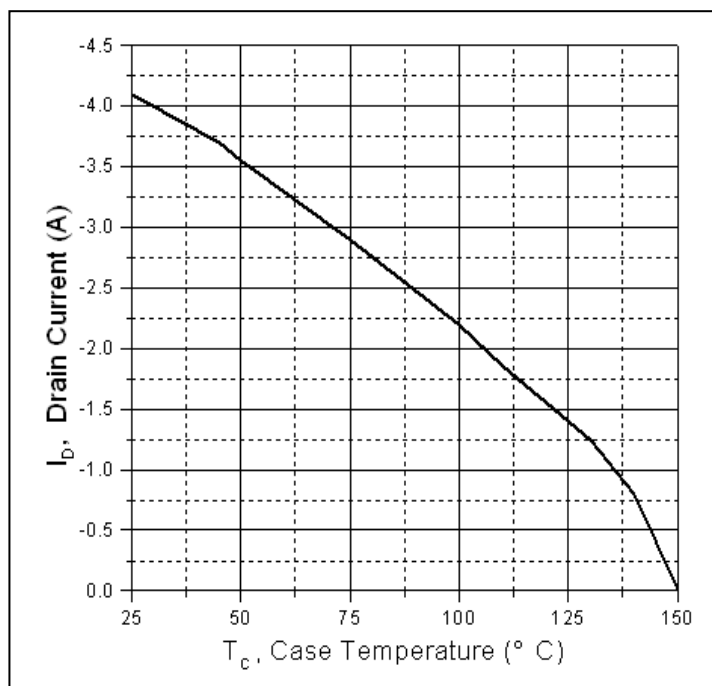


Figure 5. Maximum Drain Current Vs. Case Temperature

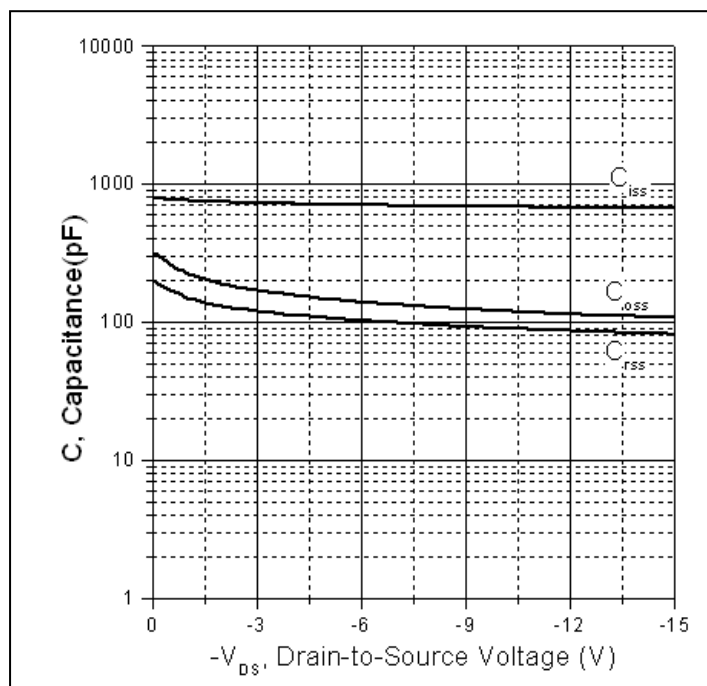


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

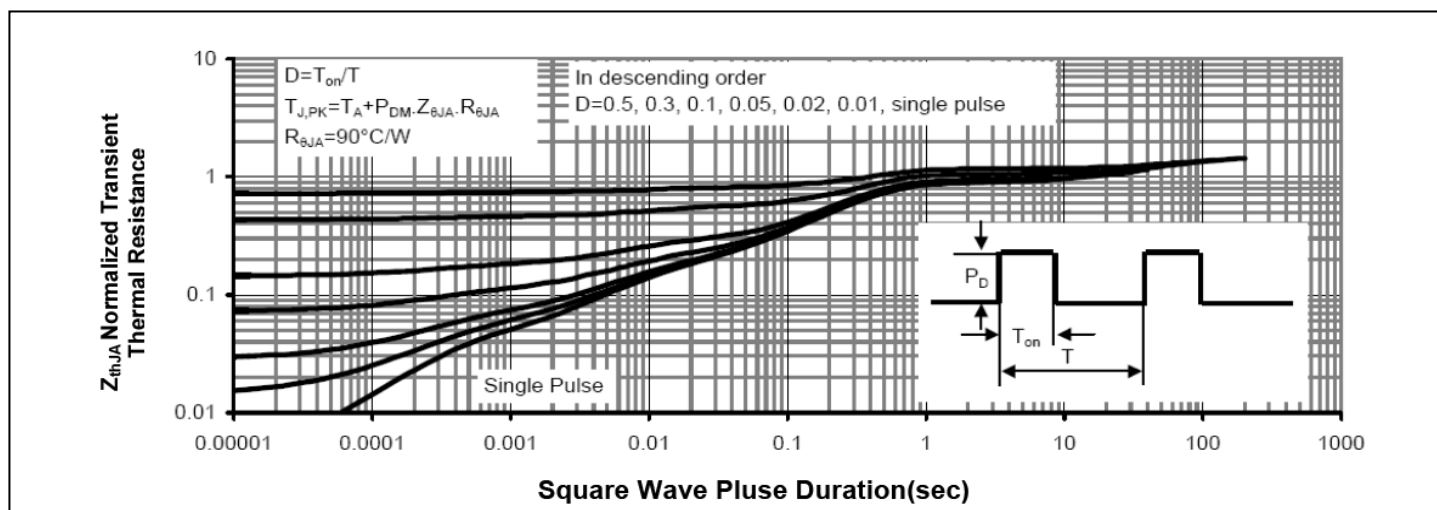
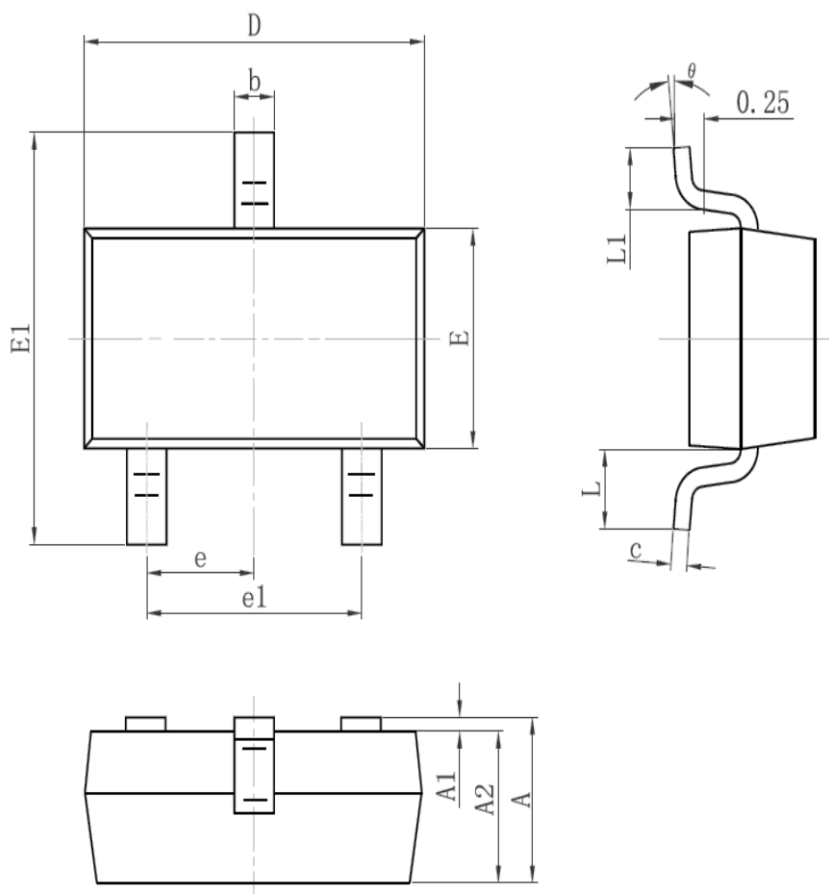


Figure7. Maximum Effective Transient Thermal Impedance Junction-to-Case

Mechanical Data:

SOT-23 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters		Dimension In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.95TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.55REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Ordering and Marking Information
Device Marking: 3339

Package (Available)
SOT-23
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/Tape	Tapes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
SOT23	3000	10	30000	4	120000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T _j =125°C to 150°C @ 80% of Max V _{DSS} /V _{CES} /V _R	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T _j =150°C @ 100% of Max V _{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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Customer Service**Worldwide Sales and Service:**

Sales@silikron.com

Technical Support:

Technical@silikron.com

Suzhou Silikron Semiconductor Corp.

11A, 428 Xinglong Street, Suzhou Industrial Park, P.R.China

TEL: (86-512) 62560688

FAX: (86-512) 65160705

E-mail: Sales@silikron.com