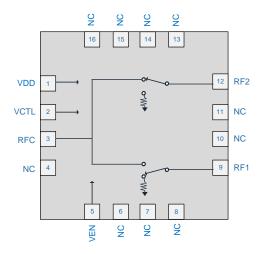


RFSW6024

Absorptive High Isolation SPDT Switch 5MHz to 6000MHz

The RFSW6024 is a Silicon on Insulator (SOI) single-pole, double throw (SPDT) switch designed for use in cellular, 3G, LTE, and other high performance communications systems. It offers a high isolation symmetric topology with excellent linearity and power handling capability. No blocking caps are necessary on the RF ports. The design is non-reflective such that RF ports 1 and 2 are terminated in the off-state. The enable pin allows for a terminated "all-off state". The RFSW6024 is 1.8V positive logic compatible.



Functional Block Diagram

Ordering Information

RFSW6024SQ	Sample bag with 25 pieces
RFSW6024SR	7" Reel with 100 pieces
RFSW6024TR13	13" Reel with 2500 pieces
RFSW6024PCK-410	5MHz to 6000MHz PCBA with 5-piece sample bag



Package: QFN, 16-pin, 4.0mm x 4.0mm

Features

- 5MHz to 6000MHz Operation
- Symmetric SPDT
- Non-Reflective (RF1, RF2)
- Terminated All-off State
- No Blocking Caps Necessary Unless Voltage on RF Line
- High Isolation: 60dB at 2GHz
- High Input IP3: 66dBm
- 2kV ESD
- 1.8V Logic Compatible

Applications

- Cellular, 3G, LTE Infrastructure
- WiBro, WiMAx. LTE
- Wireless Backhaul
- High Performance Communications Systems
- Test Equipment



Absolute Maximum Ratings

Parameter	Rating	Unit
Control Voltage (V _{CTL} , V _{EN})	6.0	V
Supply Voltage (V _{DD})	6.0	V
Maximum CW Input Power	36	dBm
Storage Temperature Range	-40 to +150	°C
ESD Rating - Human Body Model (HBM)	2000	V
Moisture Sensitivity Level	MSL2	



Caution! ESD sensitive device.



RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Recommended Operating Condition

Parameter	S	Unit		
r ai ailletei	Min	Тур	Max	Oilit
Operating Temperature Range	-40		+105	°C
Operating Junction Temperature			125	°C
Supply Voltage	2.5	3	5.5	V

Nominal Operating Parameters

Parameter	Specification			Unit	
Faranietei	Min	Тур	Max	Onit	Condition
General Performance ^{1 & 2}					Electrical Specifications, TA = 25°C, V_{CRTL} = 0/+5 V_{DC} , V_{DD} = +5 V_{DC} , 50 Ω system.
Operating Frequency Range	5		6000	MHz	
		0.55		dB	0.3GHz
		0.6		dB	1GHz
Insertion Loss (PEC to PE1/PE2)		0.75	1	dB	2GHz
Insertion Loss (RFC to RF1/RF2)		0.9		dB	3GHz
		0.9		dB	4GHz
		1.1		dB	5GHz
		75		dB	0.3GHz
		63		dB	1GHz
location (DEC to DE1/DE2)	53	60		dB	2GHz
Isolation (RFC to RF1/RF2)		60		dB	3GHz
		60		dB	4GHz
		48		dB	5GHz



B	Specification				
Parameter	Min	Тур	Max	Unit	Condition
General Performance - Continued					Electrical Specifications, TA = 25°C, V_{CRTL} = 0/+5 V_{DC} , V_{DD} = +5 V_{DC} , 50 Ω system.
		80		dB	0.3GHz
		70		dB	1GHz
Isolation (RF1 to RF2)	53	60		dB	2GHz
130/4/10/11/10/11/2)		53		dB	3GHz
		48		dB	4GHz
		49		dB	5GHz
		28		dB	0.3GHz
		27		dB	1GHz
Return Loss (RF1/RF2 On-state)		20		dB	2GHz
Neturi Loss (N. 1/N. 2 On-state)		20		dB	3GHz
		22		dB	4GHz
		17		dB	5GHz
		37		dB	0.3GHz
Return Loss (RF1/RF2 Off-state)		36		dB	1GHz
		30		dB	2GHz
		27		dB	3GHz
		23		dB	4GHz
		20		dB	5GHz
Input IP3	55	65		dBm	1GHz + 12dBm input power per tone, 1MHz tone spacing
input ii 5	55	65		dBm	2GHz + 12dBm input power per tone, 1MHz tone spacing
Input 0.1dB Compression Point		36		dBm	1GHz
Input 1dB Compression Point		36		dBm	101/2
Settling Time		1.5	3	μs	50% V _{CTRL} to optimum functionality
Start-up Time		25	50	μs	90% V _{DD} to full functionality
Switching Speed		250		ns	50% control to 10/90% RF
Switching Speed		360	600	ns	50% control to 2/98% RF
Power Supply					
Supply Current (I _{DD})		140	200	μΑ	$V_{DD} = 5.0V$
Control Current (I _{CTL} , I _{EN})		0.5	5	μΑ	V _{CTL} = 5.0V
Low Control Voltage (V _{CTL})	0		0.63	V	1.9V/Logic competible
High Control Voltage (V _{CTL})	1.1		VDD	V	1.8V Logic compatible

Notes: S-parameters have the PCB de-embedded. RF ports need to be at 0V DC. If > 0.5V is present on RF lines, blocking caps are required.



Maximum Operating Power at 85°C, CW, > 300MHz

Input	State	VEN	Power	Theta-J (°C/W)
RFC, RF1/2	On	Low	33dBm ¹	97 ²
RFC	Both Off	High	31.3dBm	N/A
RF1/2	Off	Low or High	26dBm	100
RF1/2 (Simultaneous)	Both Off	High	27.8dBm ³	65

Notes:

- 1. Assuming load VSWR < 3:1, for high VSWR loads this value reduces to 30.5dBm
- 2. Applies to resistive loss from insertion loss not including mismatch loss
- 3. Total power in both loads being driving simultaneously
- 4. For < 300MHz, it is recommended to operate at least 4dB below 1dB compression point

Truth Tables

Control	Input	Signal Path State		
VCTL	VEN	RFC-RF1	RFC-RF2	
0	0	Off	On	
1	0	On	Off	
0	1	Off	Off	
1	1	Off	Off	

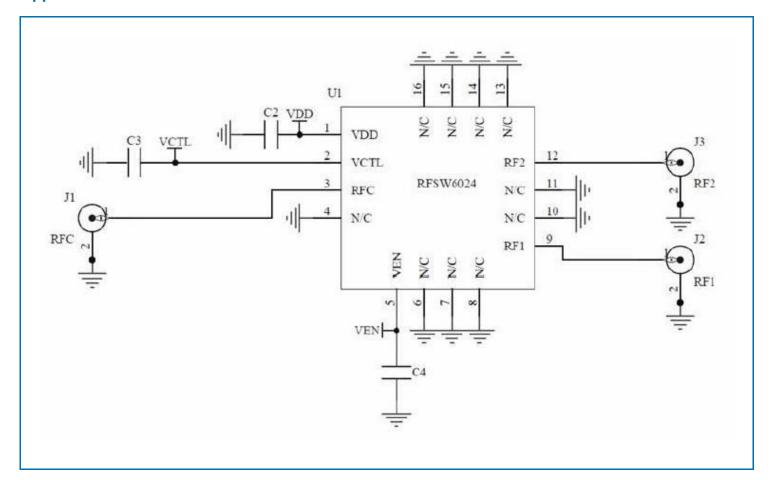
[&]quot;0" = 0V to 0.63V

 V_{DD} = 2.5 to 5.5V, must be applied for all valid states

[&]quot;1" = 1.1V to $V_{\rm DD}$



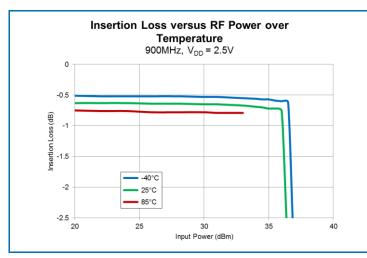
Application Schematic

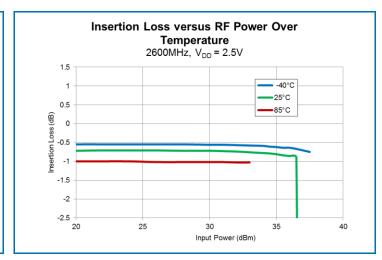


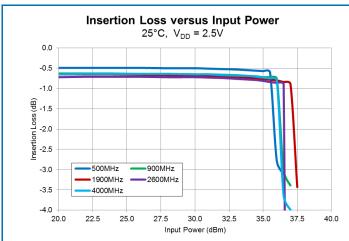
5 of 16



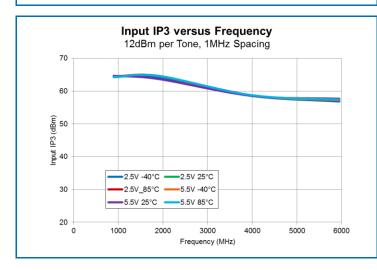
Typical Performance: $T = 25^{\circ}C$, $V_{DD} = 3V$ unless otherwise noted

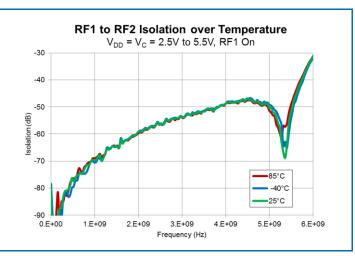






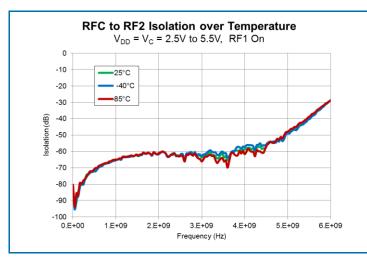


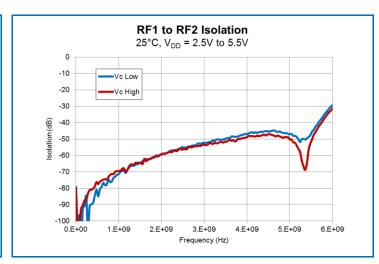


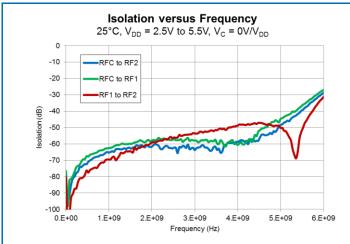


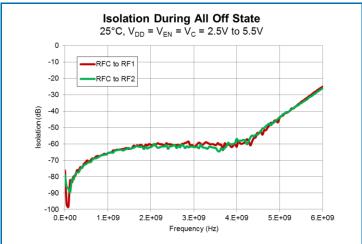


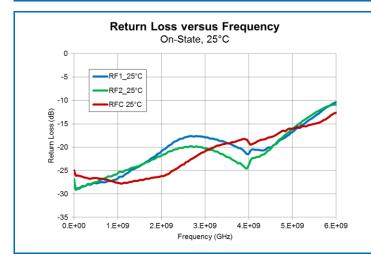
Typical Performance: T = 25°C, $V_{DD} = 3V$ unless otherwise noted

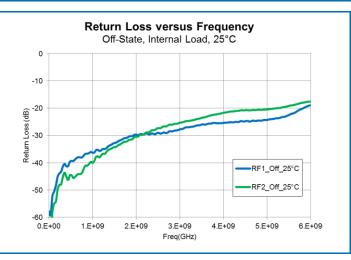






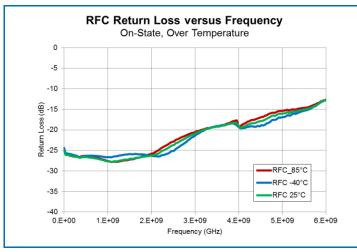


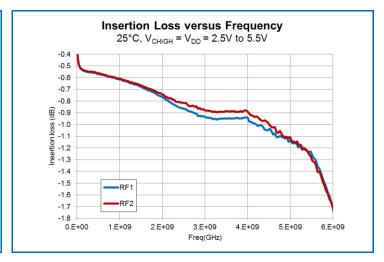


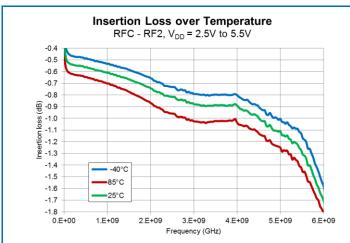


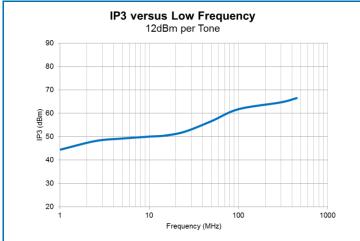


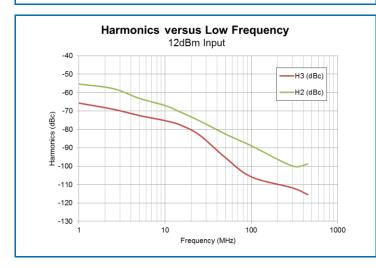
Typical Performance: $T = 25^{\circ}C$, $V_{DD} = 3V$ unless otherwise noted

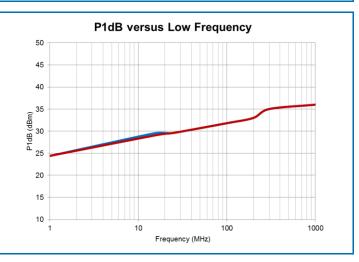














Temp = 85°C, Switching Speed (t_{OFF}) = 234ns, 50% CTL to 10%RF

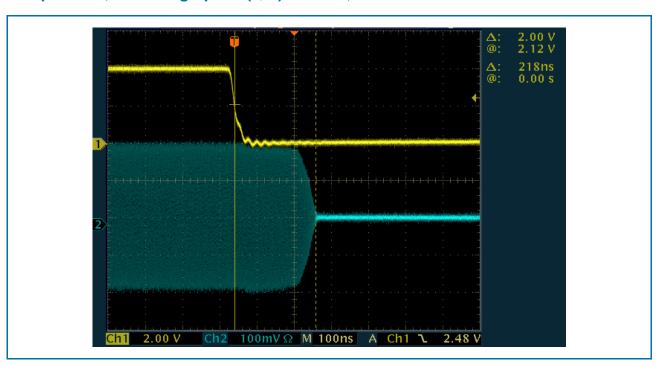


Temp = 85°C, Switching Speed (t_{ON}) = 284ns, 50% CTL to 90%RF

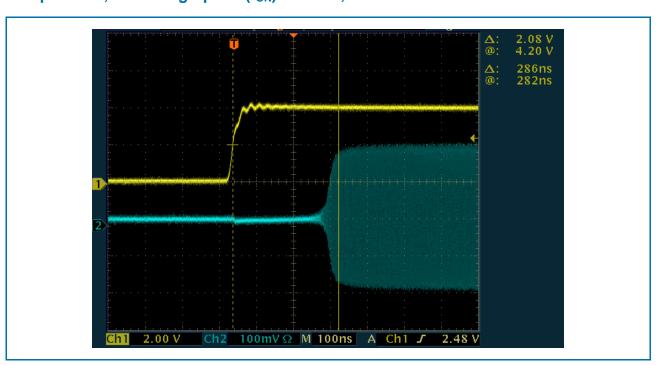




Temp = 25°C, Switching Speed (t_{OFF}) = 218ns, 50% CTL to 10%RF

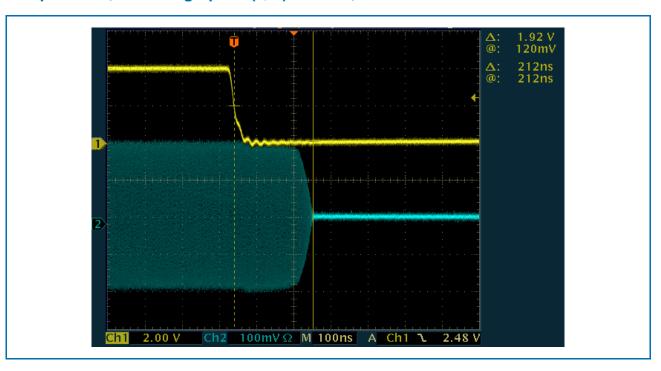


Temp = 25°C, Switching Speed (t_{ON}) = 286ns, 50% CTL to 90%RF





Temp = -40°C, Switching Speed (t_{OFF}) = 212ns, 50% CTL to 10%RF

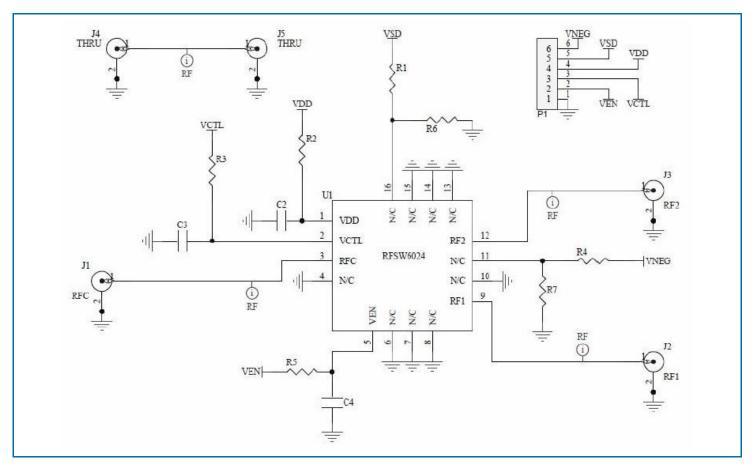


Temp = -40°C, Switching Speed (t_{ON}) = 280ns, 50% CTL to 90%RF





Evaluation Board Schematic



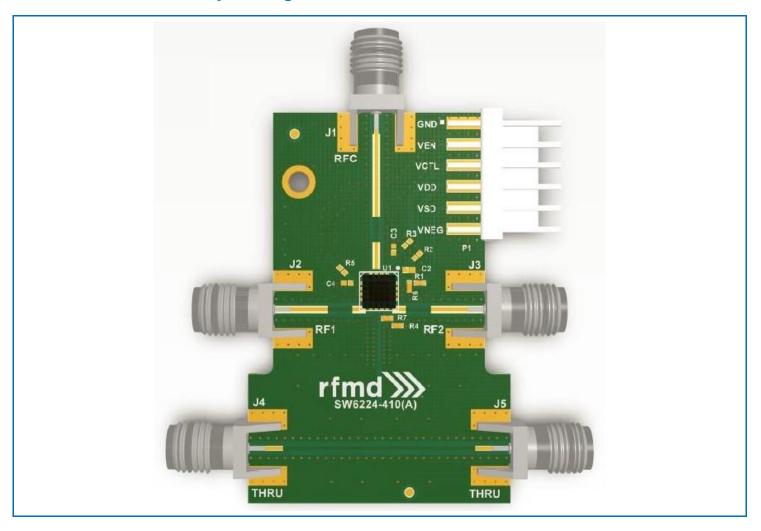
Note: V_{SD} and V_{NEG} are not used.

Evaluation Board Bill of Materials (BOM)

Description	Reference Designator	Manufacturer	Manufacturer's P/N	
RFSW6024 Evaluation Board		Viasystems Sales, Inc. (Toronto)	RFSW6224-410(A)	
CAP, 100pF, 5%, 50V, C0G, 0402 (optional)	C2-C4	Taiyo Yuden (USA), Inc.	RM UMK105 CG101JV-F	
0Ω, 50mΩ MAX, 0402 LEAD FREE	R2-R3, R5-R7	KOA Speer Electronics, Inc.	RK73Z1ETTP	
Do Not Install	R1, R4			
CONN, HDR, ST, PLRZD, 6-PIN, 0.100"	P1	AMP	640454-6	
CONN, SMA EL MINI FLT 0.068" SPE- 000303	J1-J5	Aliner Industries, Inc.	20-001CF-T	
RFSW6024SB	U1	RFMD	RFSW6024	



Evaluation Board Assembly Drawing





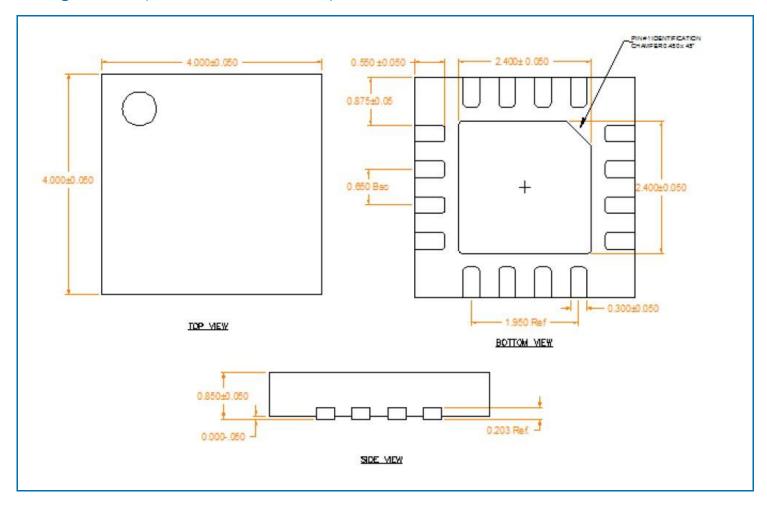
Pin Names and Descriptions

Pin	Name	Description	
1	VDD	Supply Voltage	
2	VCTL	Logic Control Input	
3	RFC	RF Common Port	
4	NC	No Internal Connection	
5	VEN	Logic input for putting switch in "all-off" state. Logic high for "all-off" state.	
6	GND or NC	Ground or No Connection	
7	GND or NC	Ground or No Connection	
8	NC	No Internal Connection	
9	RF1	RF Port 1	
10	GND or NC	Ground or No Connection	
11	GND or NC	Ground or No Connection	
12	RF2	RF Port 2	
13	NC	No Internal Connection	
14	GND or NC	Ground or No Connection	
15	GND or NC	Ground or No Connection	
16	NC	No Internal Connection	
EPAD	GND	RF and DC Ground: Must be soldered to EVB ground plane over a bed of vias	

Note: RFMD recommends that the NC pins be grounded on the EVB to maximize isolation.



Package Outline (Dimensions in millimeters)





Branding Diagram

