



PH3855L

N-channel TrenchMOS™ logic level FET

Rev. 01 — 26 January 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Surface mounted package.

1.3 Applications

- DC-to-DC converters
- Motors, lamps, solenoids
- General purpose power switching
- 12 V and 24 V loads.

1.4 Quick reference data

- $V_{DS} \leq 55 \text{ V}$
- $I_D \leq 24 \text{ A}$
- $R_{DSon} \leq 36 \text{ m}\Omega$
- $Q_{gd} = 5.5 \text{ nC (typ.)}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source	<p>Top view</p> <p>SOT669 (LFAK)</p>	<p>mbb076</p>
4	gate		
mb	mounting base; connected to drain		

3. Ordering information

Table 2: Ordering information

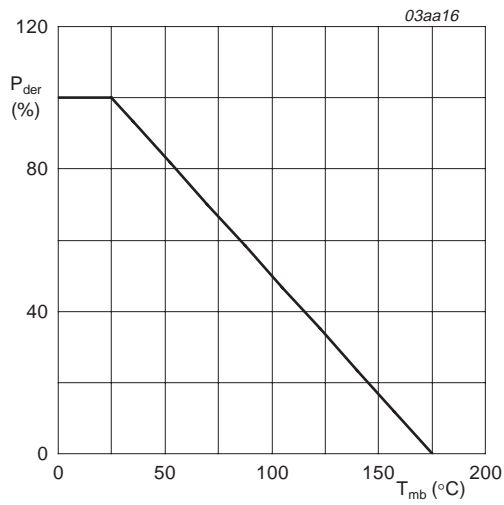
Type number	Package		Version
	Name	Description	
PH3855L	LFPAK	plastic single-ended surface mounted package; 4 leads	SOT669

4. Limiting values

Table 3: Limiting values

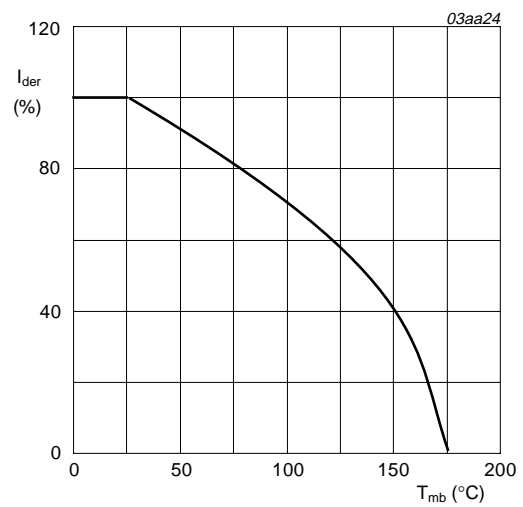
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage (DC)		-	± 15	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2 and 3	-	24	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2	-	17.2	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	45	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	50	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	24	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	45	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 30\text{ A}$; $t_p = 0.04\text{ ms}$; $V_{DD} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	40	mJ



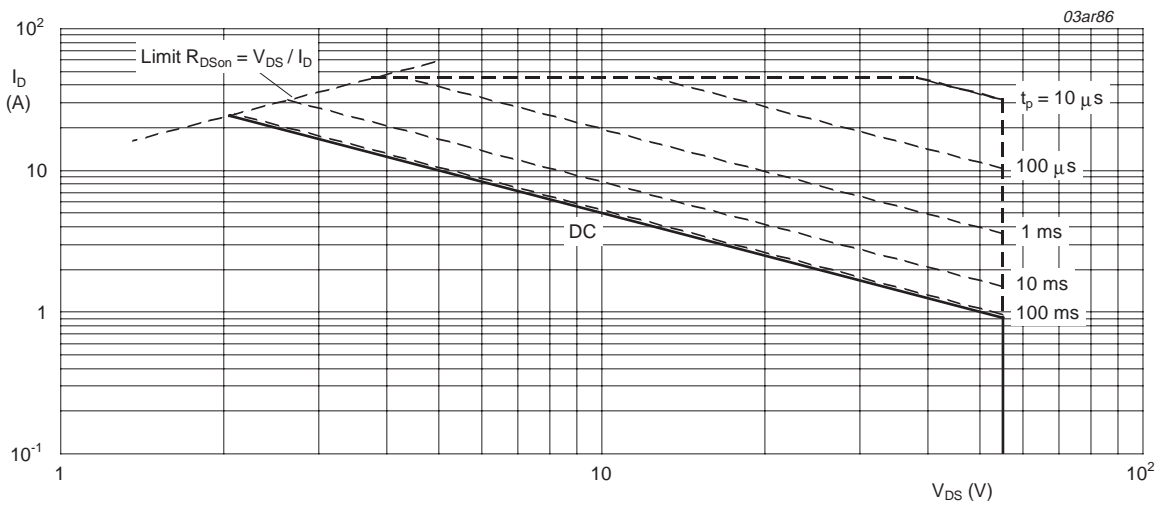
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^\circ C$; I_{DM} is single pulse; $V_{GS} = 5 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	3	K/W

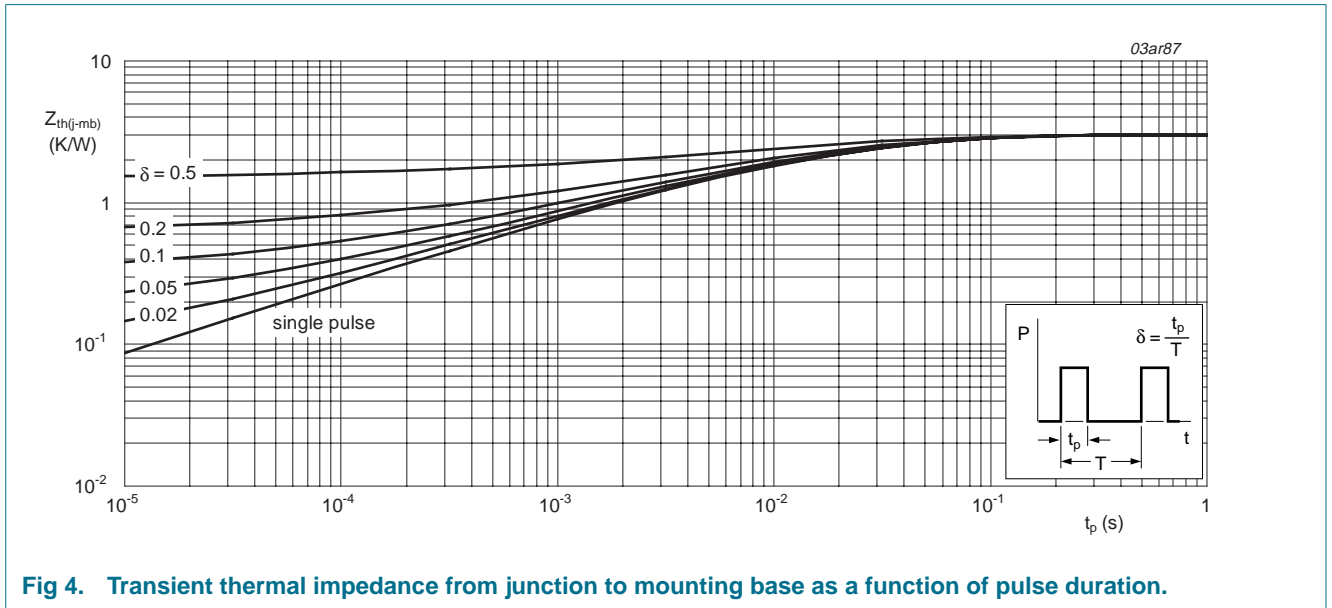
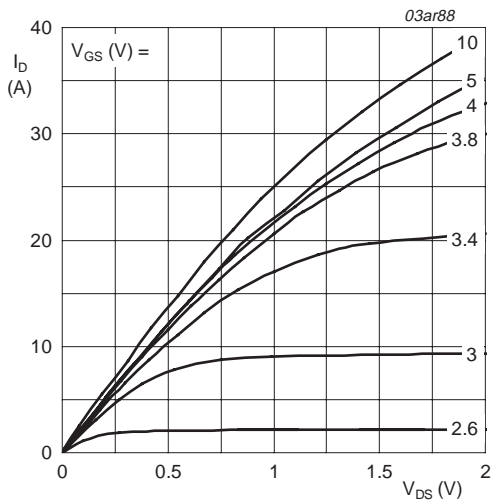


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

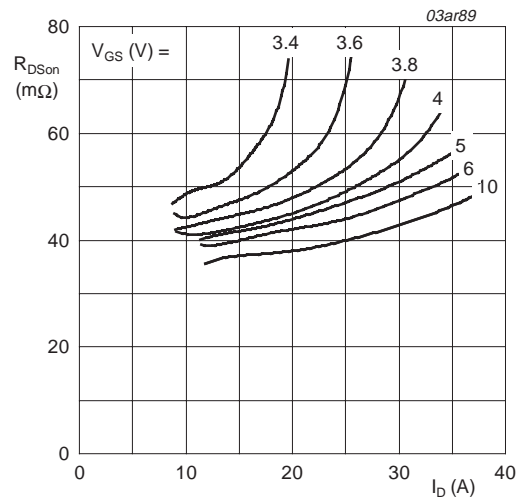
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C T _j = -55 °C	55 50	- -	- -	V V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 and 10 T _j = 25 °C T _j = 175 °C T _j = -55 °C	1 0.5 -	1.5 - -	2 - 2.2	V V V
I _{DSS}	drain-source leakage current	V _{DS} = 55 V; V _{GS} = 0 V T _j = 25 °C T _j = 175 °C	- - -	- - -	1 500	μA μA
I _{GSS}	gate-source leakage current	V _{GS} = ±15 V; V _{DS} = 0 V	-	2	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 15 A; Figure 6 and 8 T _j = 25 °C T _j = 175 °C V _{GS} = 4.5 V; I _D = 15 A; Figure 8 V _{GS} = 10 V; I _D = 15 A; Figure 6 and 8	- - - -	34 - - 32	40 84 45 36	mΩ mΩ mΩ mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 15 A; V _{DS} = 44 V; V _{GS} = 5 V; Figure 11	-	11.7	-	nC
Q _{gs}	gate-source charge		-	2.5	-	nC
Q _{gd}	gate-drain (Miller) charge		-	5.5	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 13	-	765	-	pF
C _{oss}	output capacitance		-	125	-	pF
C _{rss}	reverse transfer capacitance		-	70	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 2.2 Ω; V _{GS} = 5 V; R _G = 10 Ω	-	17	-	ns
t _r	rise time		-	93	-	ns
t _{d(off)}	turn-off delay time		-	35	-	ns
t _f	fall time		-	72	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 20 A; V _{GS} = 0 V; Figure 12	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs;	-	45	-	ns
Q _r	recovered charge	V _{GS} = 0 V; V _R = 30 V	-	25	-	nC



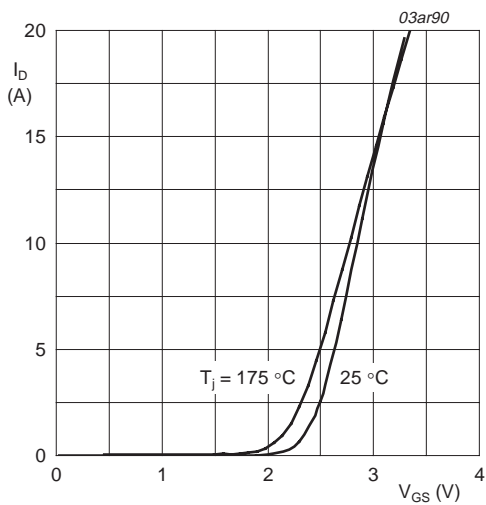
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



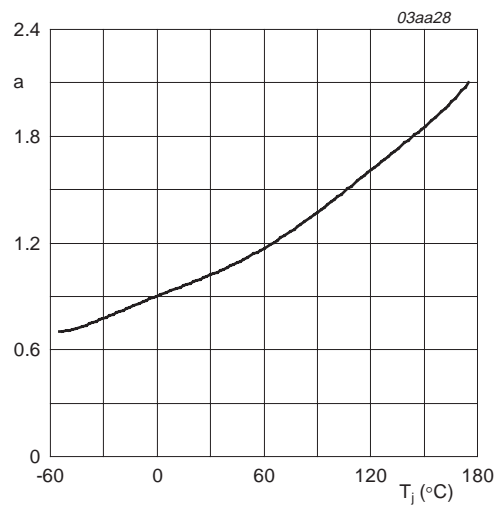
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values.



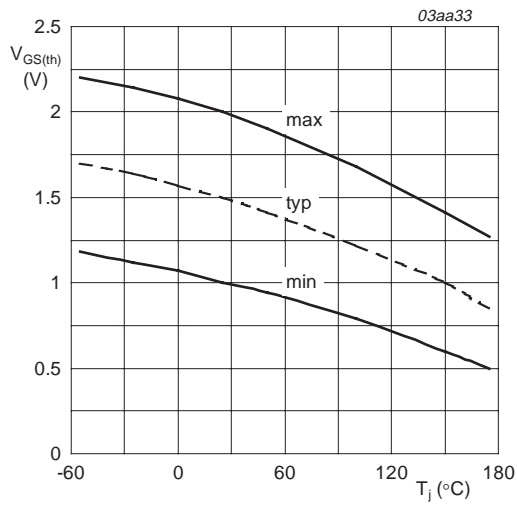
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



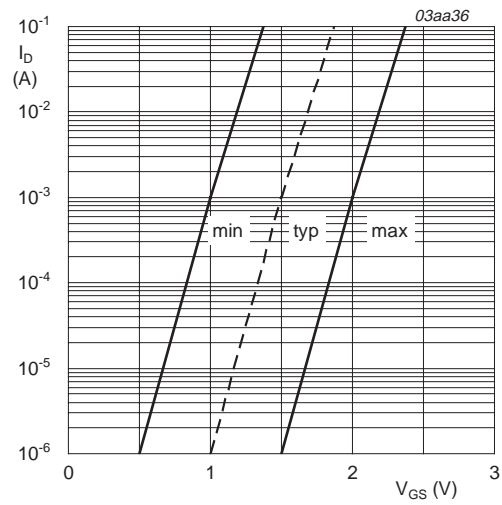
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



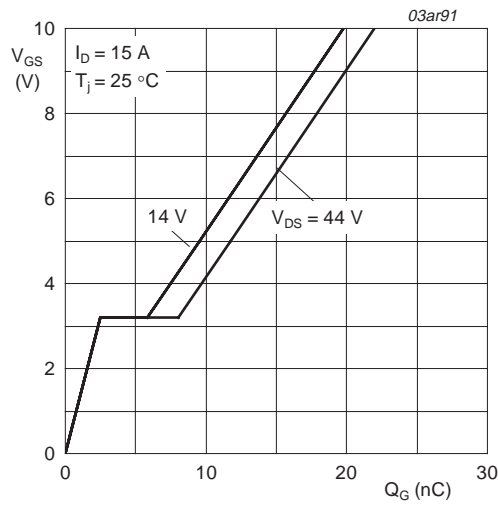
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



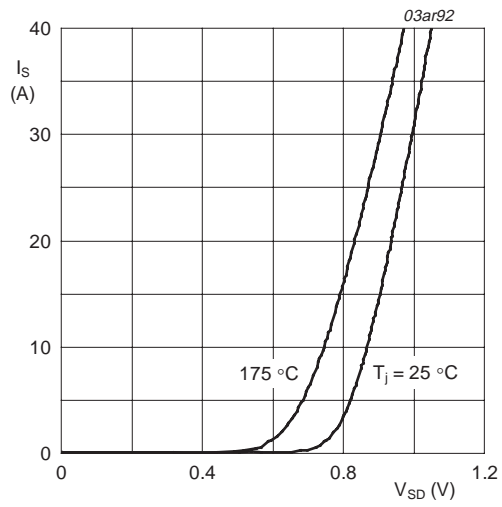
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



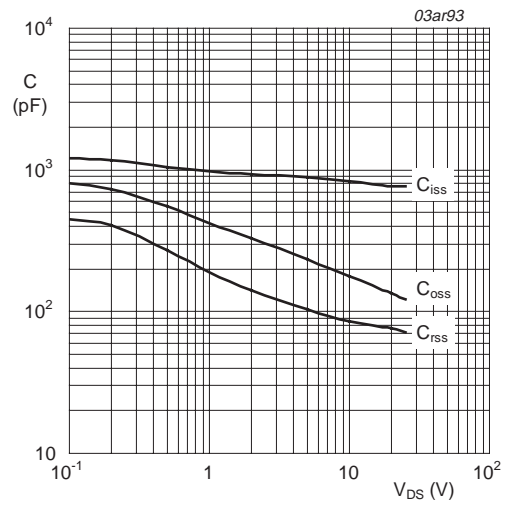
$I_D = 15 \text{ A}; V_{DS} = 14 \text{ V and } 44 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values.



$T_j = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.

7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669

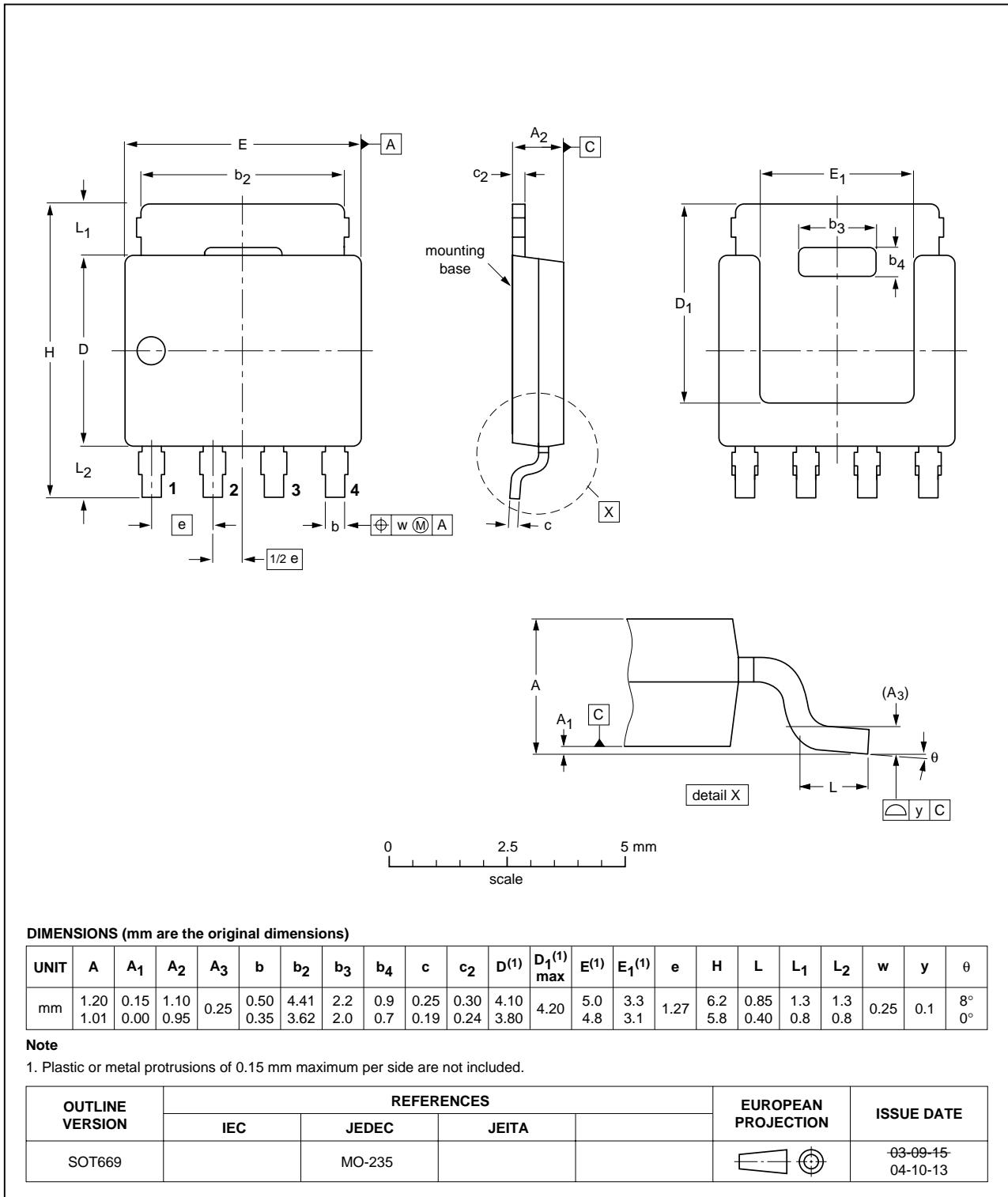


Fig 14. Package outline SOT669 (LPAK).

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH3855L_1	20050126	Product data sheet	-	9397 750 13925	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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