Preliminary

GS8132018/36CQ-333M/250M(S/Q/V)
GS868018/36CQ-333M/250M(S/Q/V)
GS836018/36CQ-333M/250M(S/Q/V)

100-Pin Ceramic QFP
Military Temp

Rad-Hard SRAM

144Mb/72Mb/36Mb PL/FT Synchronous Burst SRAMs

333 MHz–250 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- Aerospace-Level Product
- $\overline{\text{FT}}$ pin for user-configurable flow through or pipeline operation
- Single Cycle Deselect (SCD) operation
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{\text{LBO}}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write ($\overline{\text{BW}}$) and/or Global Write ($\overline{\text{GW}}$) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- 100-pin Ceramic QFP package

Radiation Performance

- Total Ionizing Dose (TID) > 300krads(Si)
- Soft Error Rate (SER) = TBR
- Neutrons = TBR
- Single Event Latchup Immunity > 80 MeV.cm^2/mg (125°C)

Functional Description

Applications

The GS8132018/36CQ (150,994,944-bit), GS868018/36CQ (75,497,472-bit), and GS836018/36CQ (37,748,736-bit) are high performance synchronous SRAMs with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{\text{E1}}$ and $\overline{\text{E3}}$), address burst control inputs ($\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$, $\overline{\text{ADV}}$), and write control inputs ($\overline{\text{Bx}}$, $\overline{\text{BW}}$, $\overline{\text{GW}}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{\text{G}}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{\text{ADV}}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{\text{LBO}}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{\text{FT}}$ mode pin (Pin 14). Holding the $\overline{\text{FT}}$ mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{\text{FT}}$ high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{\text{BW}}$) input combined with one or more individual byte write signals ($\overline{\text{Bx}}$). In addition, Global Write ($\overline{\text{GW}}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

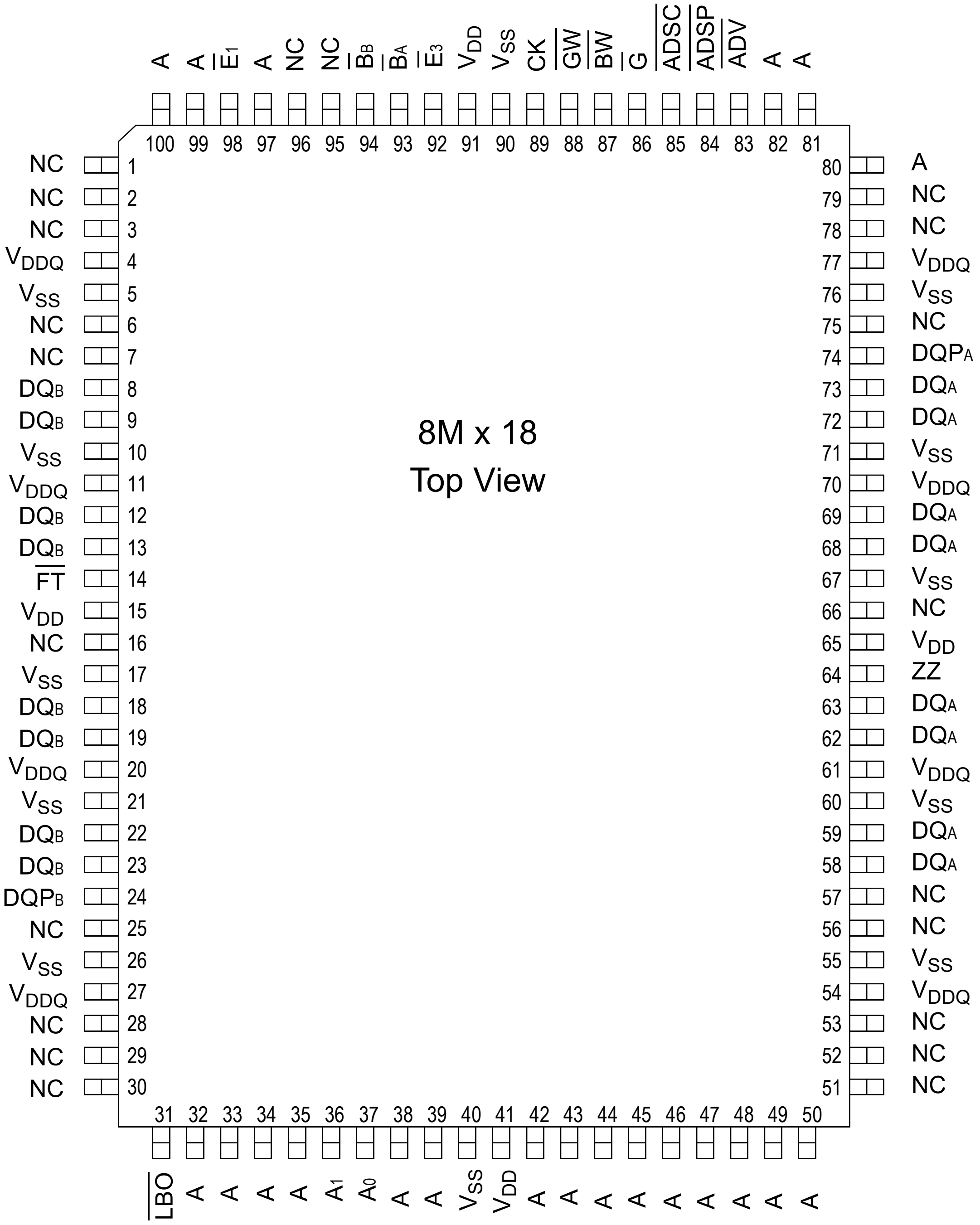
Core and Interface Voltages

The GS8132018/36CQ, GS868018/36CQ, and GS836018/36CQ operate on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

Parameter Synopsis

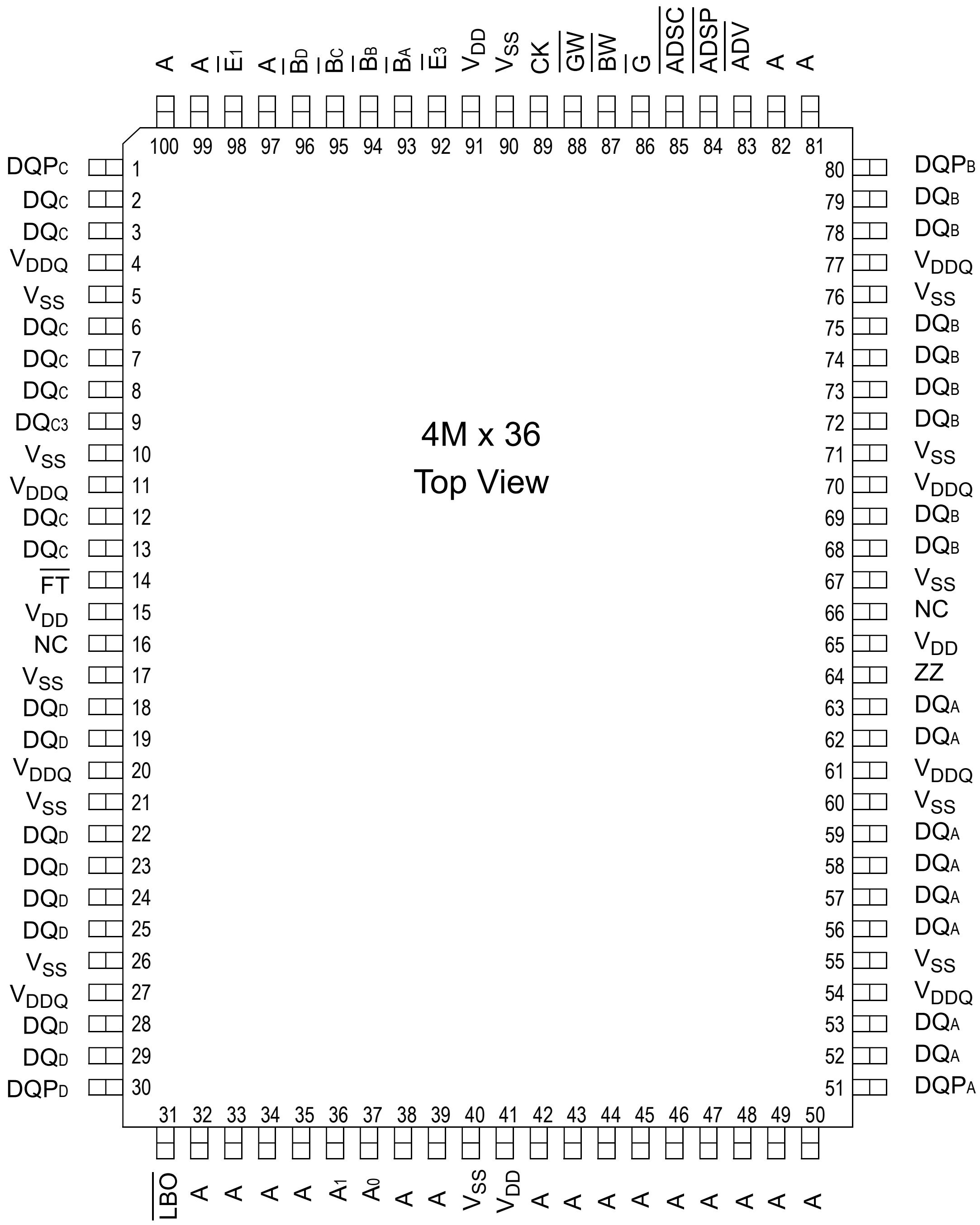
		-333M	-250M	Unit
Pipeline **3-1-1-1**	t_{KQ}	2.5	2.5	ns
	tCycle	3.0	4.0	ns
	Curr (x18)	650	550	mA
	Curr (x36)	720	590	mA
Flow Through **2-1-1-1**	t_{KQ}	4.5	5.5	ns
	tCycle	4.5	5.5	ns
	Curr (x18)	520	480	mA
	Curr (x36)	555	500	mA

GS8132018 100-Pin Ceramic QFP Pinout (144Mb)



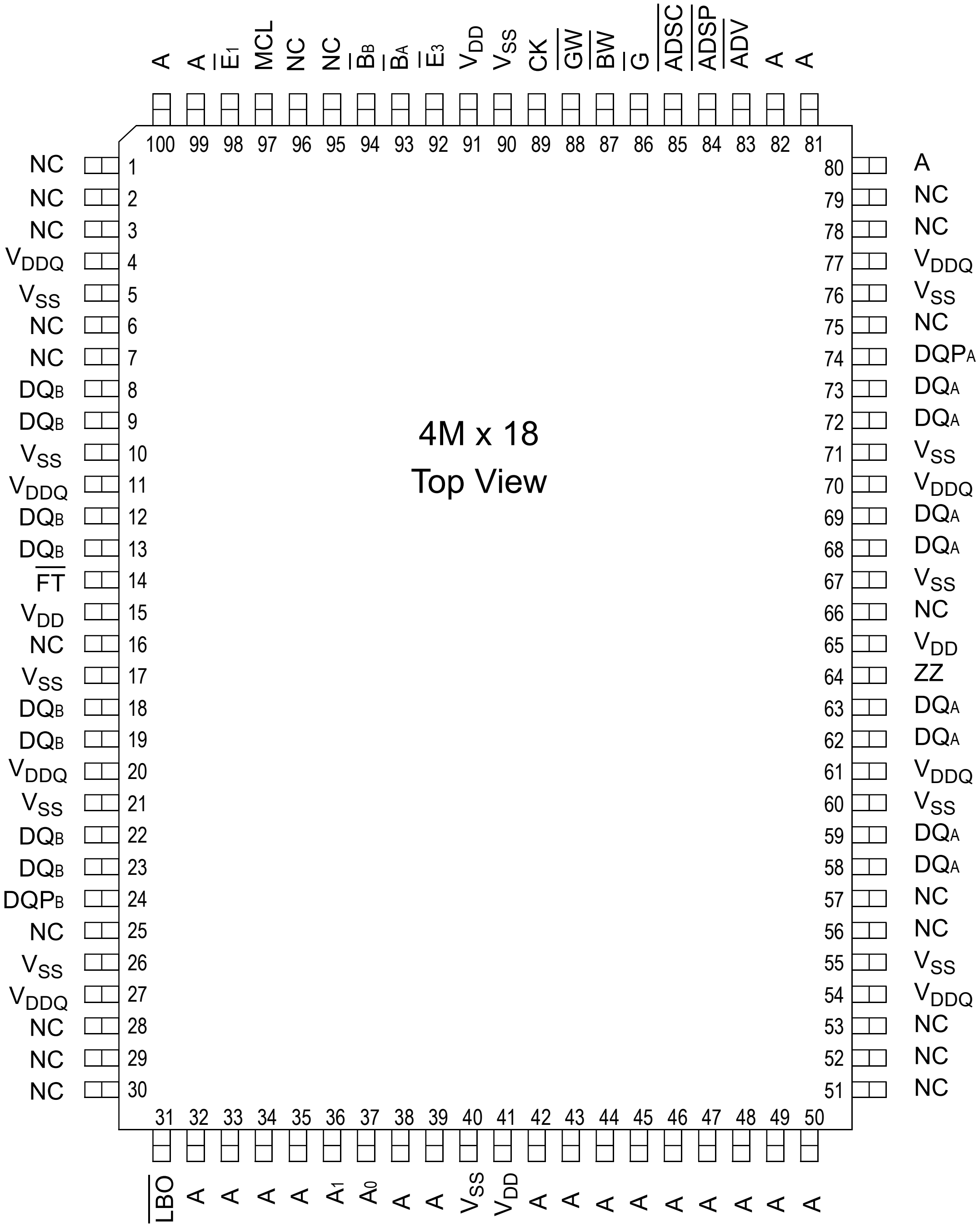
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS8132036 100-Pin Ceramic QFP Pinout (144Mb)



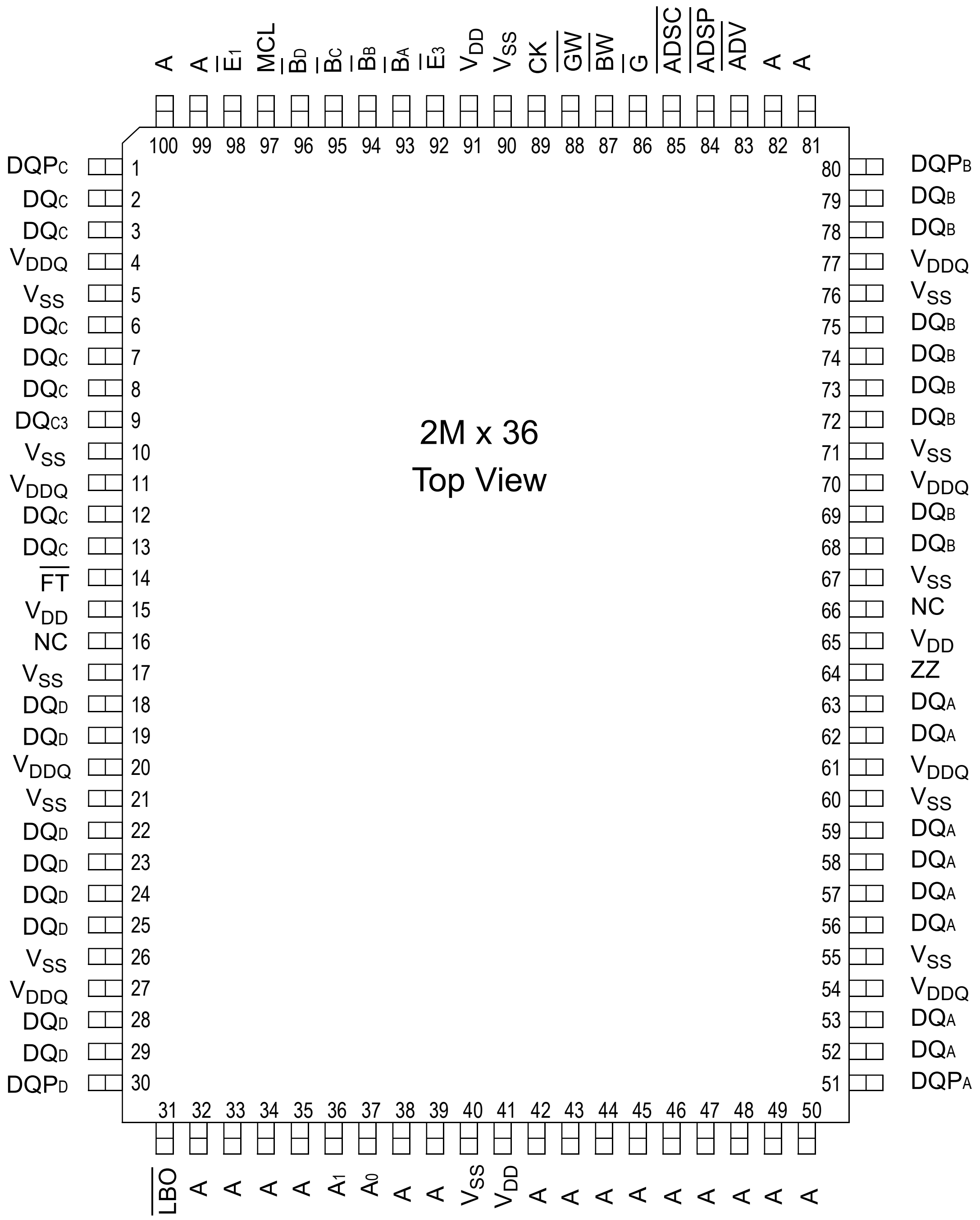
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS868018 100-Pin Ceramic QFP Pinout (72Mb)



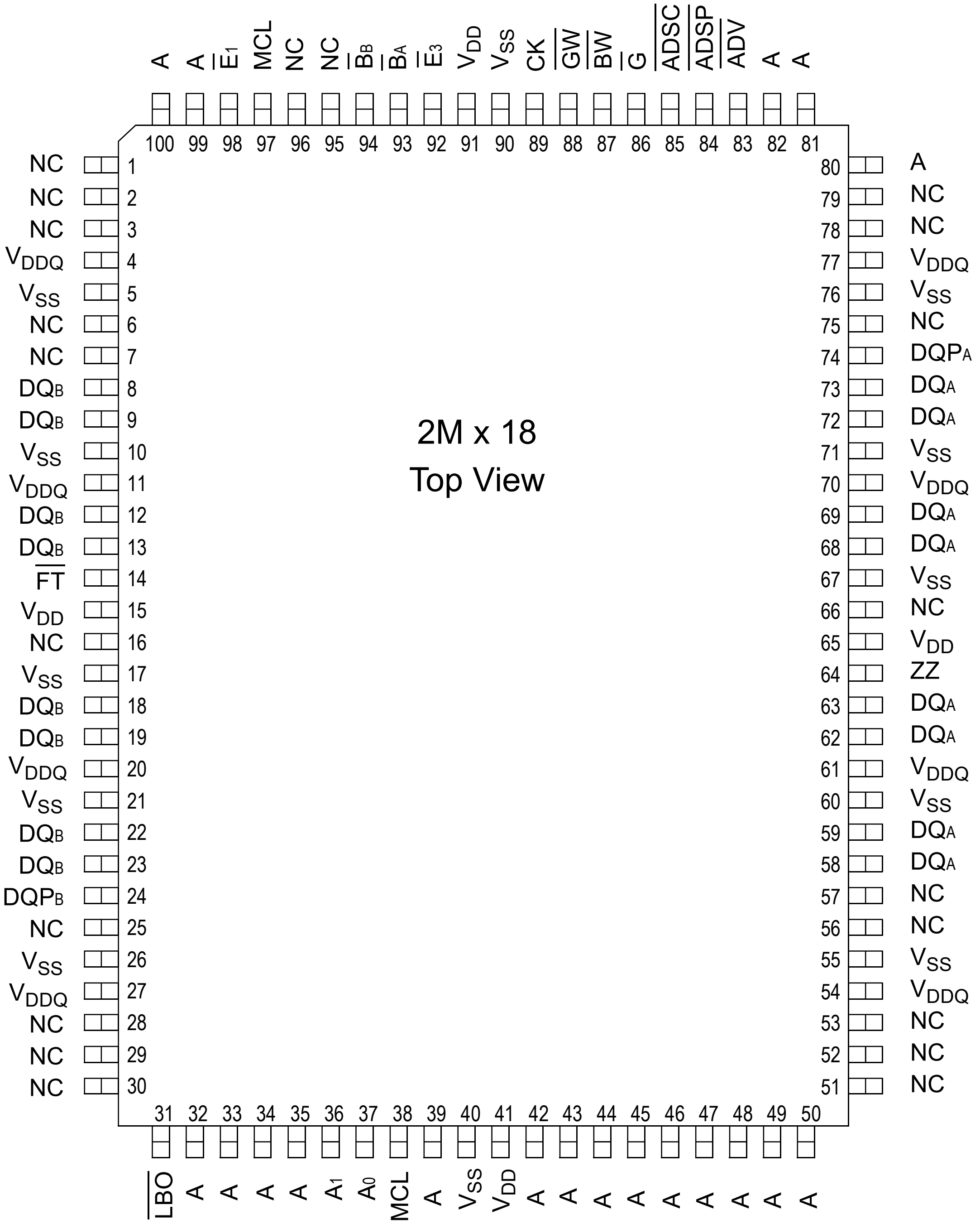
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS868036 100-Pin Ceramic QFP Pinout (72Mb)



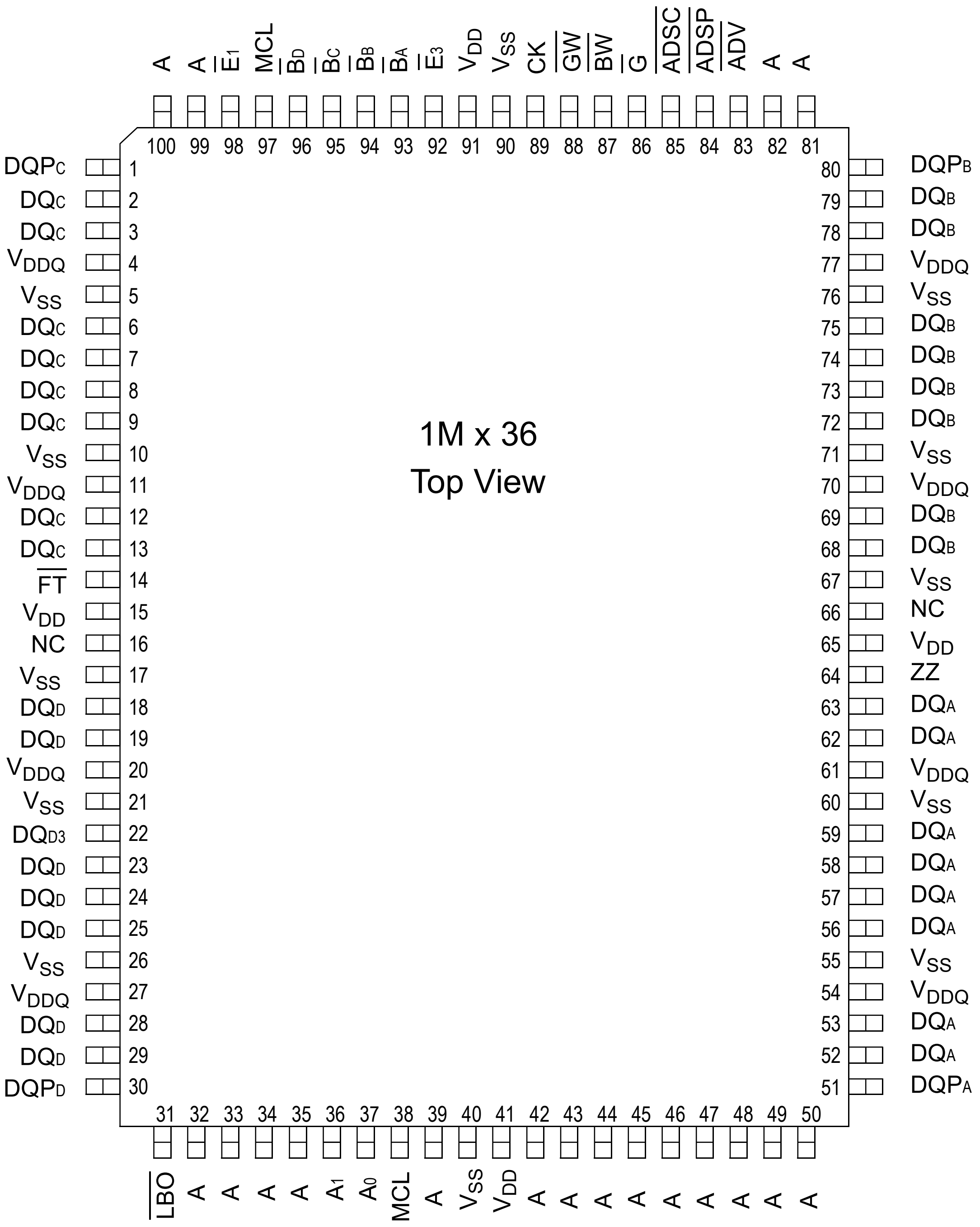
Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS836018 100-Pin Ceramic QFP Pinout (36Mb)



Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

GS836036 100-Pin Ceramic QFP Pinout (36Mb)

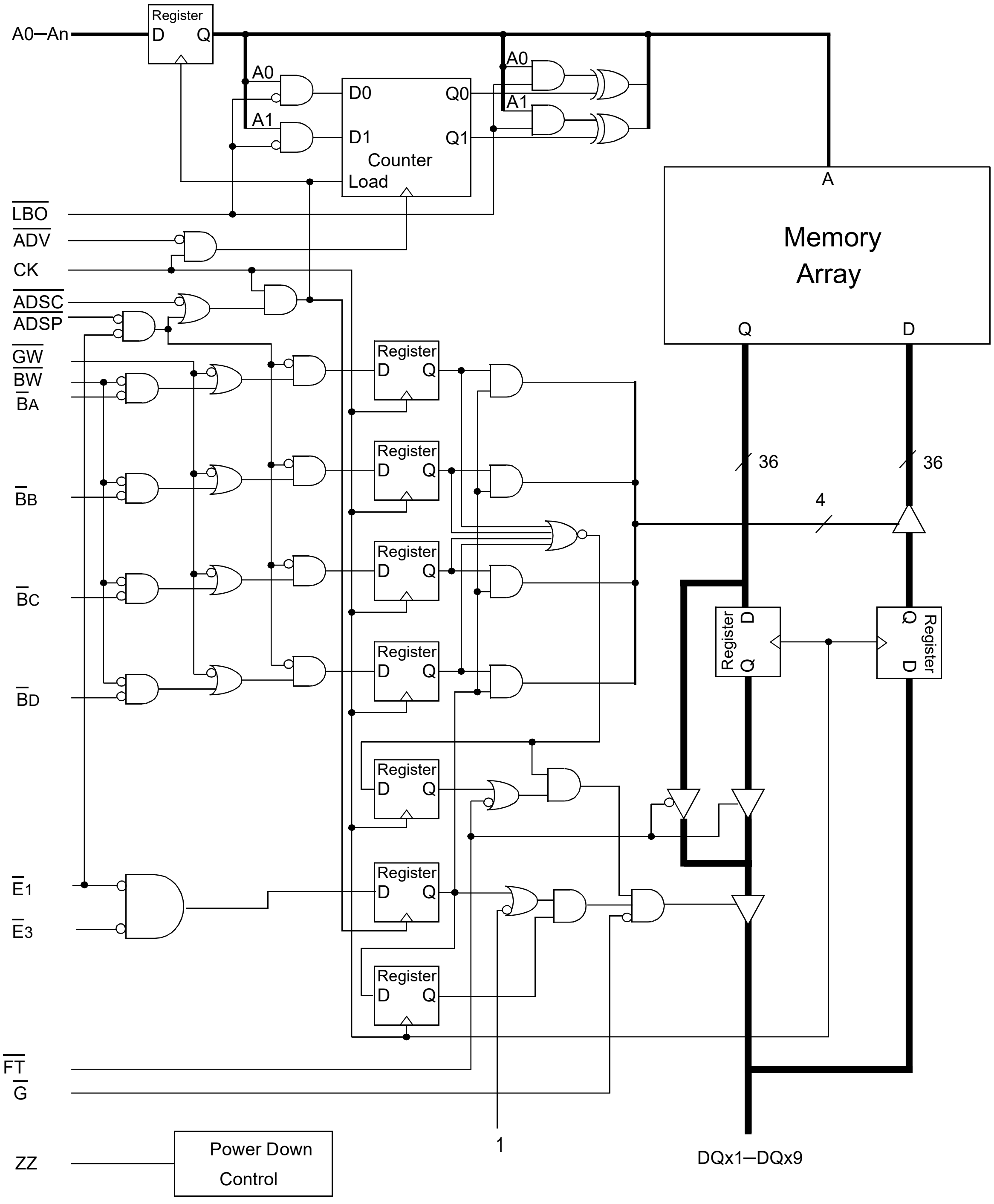


Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

Ceramic QFP Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Inputs
DQ_A DQ_B DQ_C DQ_D	I/O	Data Input and Output pins
NC		No Connect
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low
$\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_C, DQ_D Data I/Os; active low
CK	I	Clock Input Signal; active high
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep Mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC	—	No Connect
NU	—	Not Used—There is an internal chip connection to these pins, but they are unused by the device. They may be left unconnected, tied Low (to V_{SS}), or tied High (to V_{DDQ} or V_{DD}).
MCL	In	Must Connect Low—May be tied to V_{SS} directly or via a 1kΩ resistor.

Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin , so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

Byte Write Truth Table

Function	$\overline{\mathrm{GW}}$	$\overline{\mathrm{BW}}$	$\overline{\mathrm{B}}$A	$\overline{\mathrm{B}}$B	$\overline{\mathrm{B}}$C	$\overline{\mathrm{B}}$D	Notes
Read	H	H	X	X	X	X	1
Write No Bytes	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs, $\overline{\mathrm{B}}$A, $\overline{\mathrm{B}}$B, $\overline{\mathrm{B}}$C and/or $\overline{\mathrm{B}}$D.
2. Byte Write Enable inputs BA, BB, BC and/or BD may be used in any combination with BW to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x32 and x36 versions.

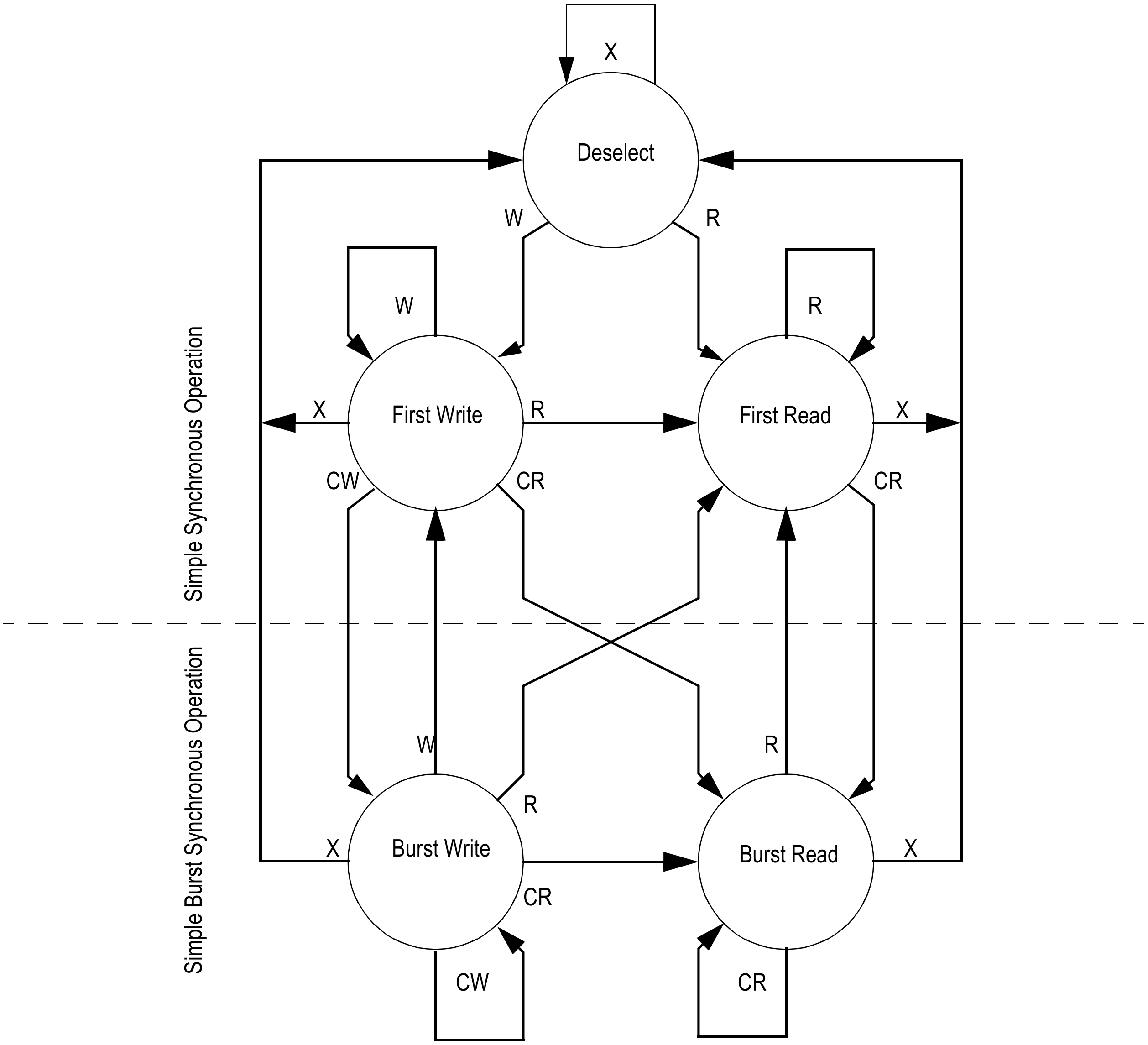
Synchronous Truth Table

Operation	Address Used	State Diagram Key	$\overline{E}1$	$\overline{E}3$	$\overline{\text{ADSP}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	$\overline{W}$	DQ[3]
Deselect Cycle, Power Down	None	X	L	H	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	H	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	H	X	X	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	L	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	L	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	L	H	L	X	T	D
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

Notes:

1. X = Don't Care, H = High, L = Low
2. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
3. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
4. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
5. Tying $\overline{\text{ADSP}}$ high and $\overline{\text{ADSC}}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
6. Tying ADSP high and ADV low while using ADSC to load new addresses allows simple burst operations. See *ITALIC* items above.

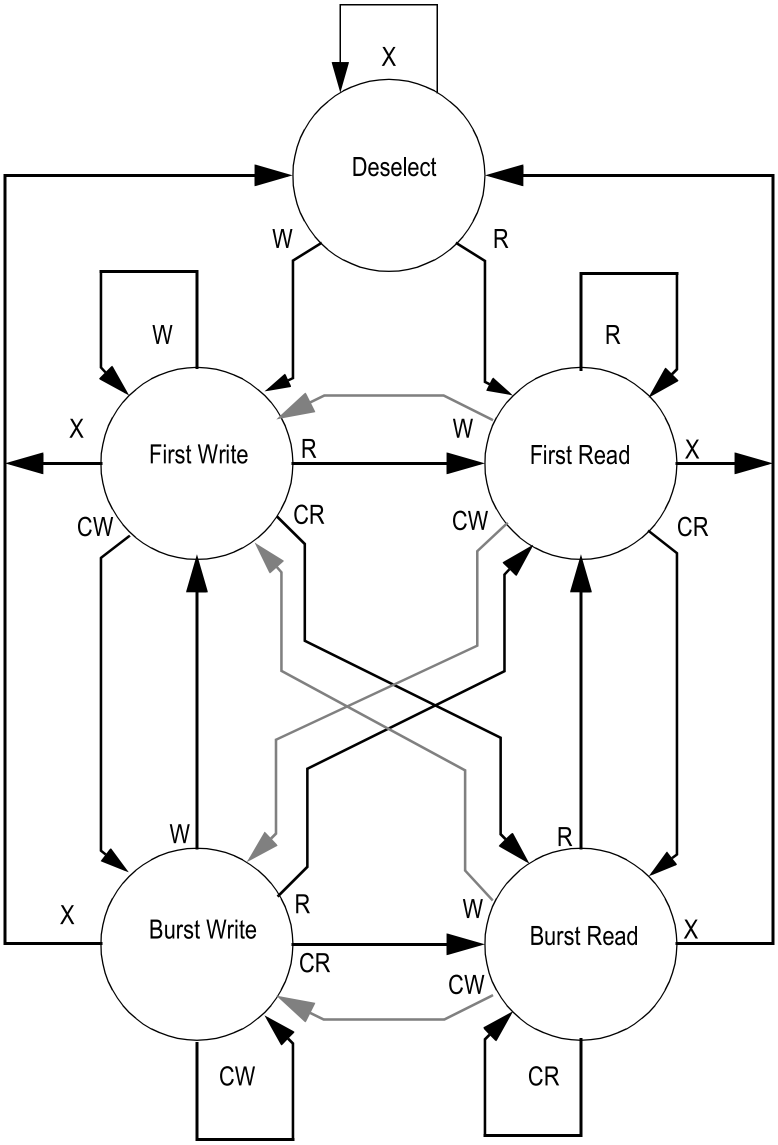
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable (E1) and Write (BA, BB, BC, BD, BW, and GW) control inputs, and that ADSP is tied high and ADSC is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{\text{ADSC}}$ control inputs, and assumes ADSP is tied high and ADV is tied low.

Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of “Dummy Reads” (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM’s drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DD} +0.5 ($\leq$ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 ($\leq$ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–65 to 150 (TBR)	^oC
T_{BIAS}	Temperature Under Bias	–55 to 125	^oC

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V

V_{DD3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Note:
V_{IH} (max) must be met for any instantaneous value of V_{DD}.

V_{DD2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	0.6^*V_{DD}	—	$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}	–0.3	—	0.3^*V_{DD}	V

Note:
V_{IH} (max) must be met for any instantaneous value of V_{DD}.

Operating Temperature

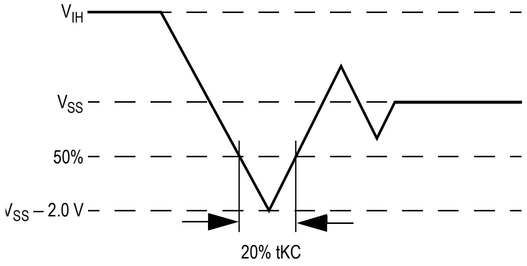
Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature	T_J	–55	25	125	°C

Thermal Impedance

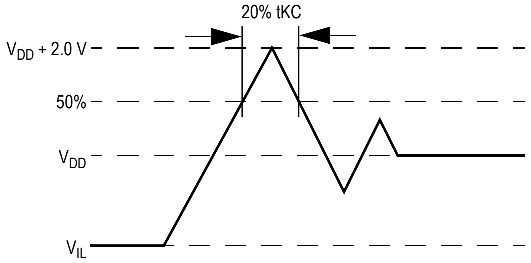
Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
100-pin Ceramic QFP	4-layer (TBR)	n/a	n/a	n/a	TBD	TBD

Notes:
1. Thermal Impedance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Note:
Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Capacitance

($T_A = 25^oC$, f = 1 MHz, $V_{DD} = 2.5$ V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$ V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0$ V	6	7	pF

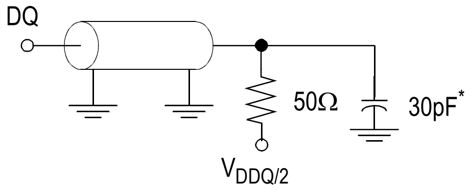
Note:
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} – 0.2$ V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	**Fig. 1**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\ V \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{FT}$ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\ V \leq V_{IN} \leq V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode		Symbol	-333M	-250M	Unit
					–55 to 125°C	–55 to 125°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	**(x32/x36)**	Pipeline	I_{DD}	720	590	mA
			Flow Through	I_{DD}	555	500	mA
		(x18)	Pipeline	I_{DD}	650	550	mA
			Flow Through	I_{DD}	520	480	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	I_{SB}	220	220	mA
			Flow Through	I_{SB}	220	220	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	240	240	mA
			Flow Through	I_{DD}	240	240	mA

Notes:

1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

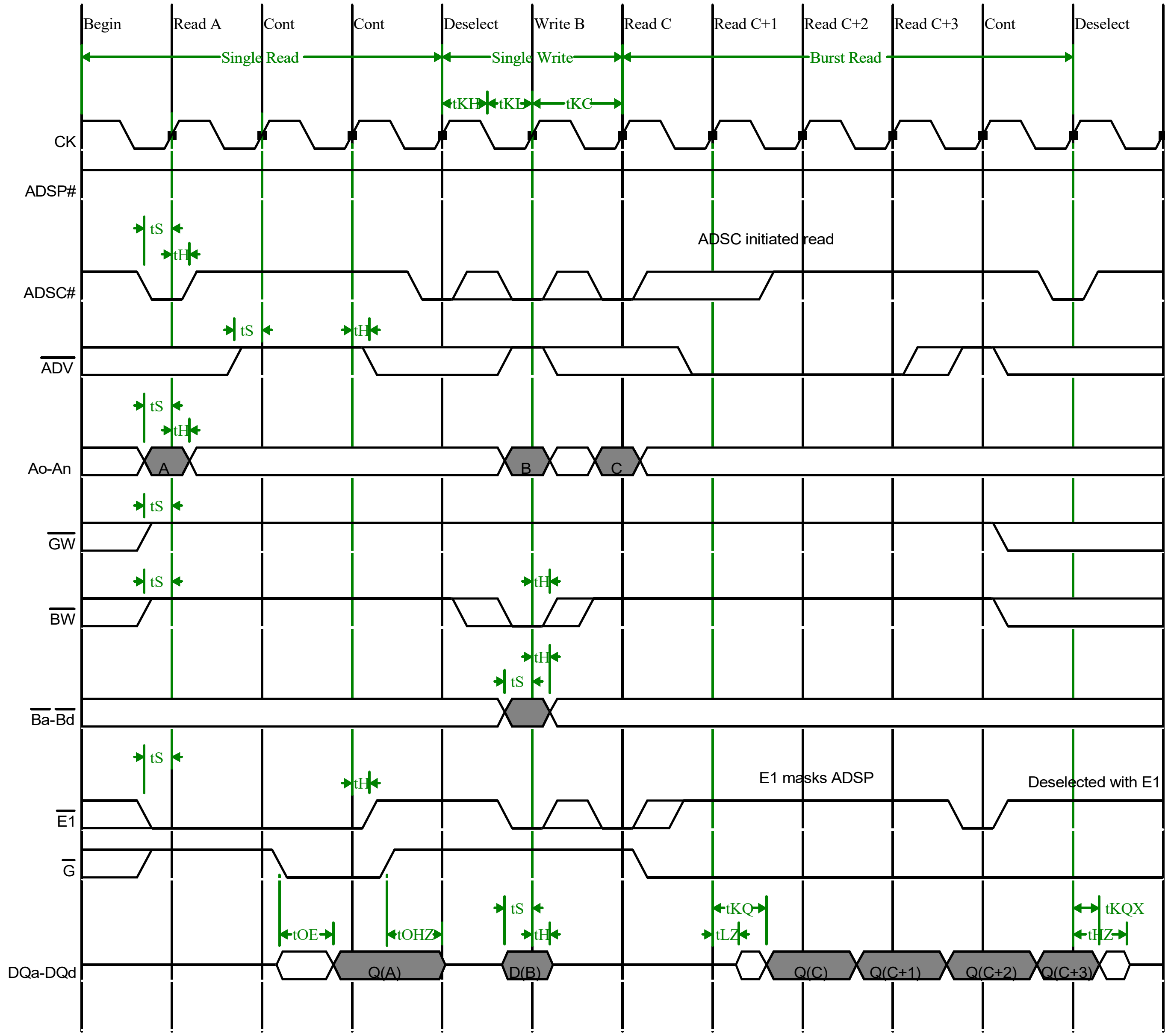
AC Electrical Characteristics

	Parameter	Symbol	-333M		-250M		Unit
			Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	3.0	—	4.0	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	2.5	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	ns
	Setup time	tS	1.0	—	1.2	—	ns
	Hold time	tH	0.1	—	0.2	—	ns
Flow Through	Clock Cycle Time	tKC	4.5	—	5.5	—	ns
	Clock to Output Valid	tKQ	—	4.5	—	5.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	ns
	Setup time	tS	1.3	—	1.5	—	ns
	Hold time	tH	0.3	—	0.5	—	ns
	Clock HIGH Time	tKH	1.0	—	1.3	—	ns
	Clock LOW Time	tKL	1.2	—	1.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	2.5	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	2.5	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	2.5	ns
	ZZ setup time	tZZS[2]	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	ns

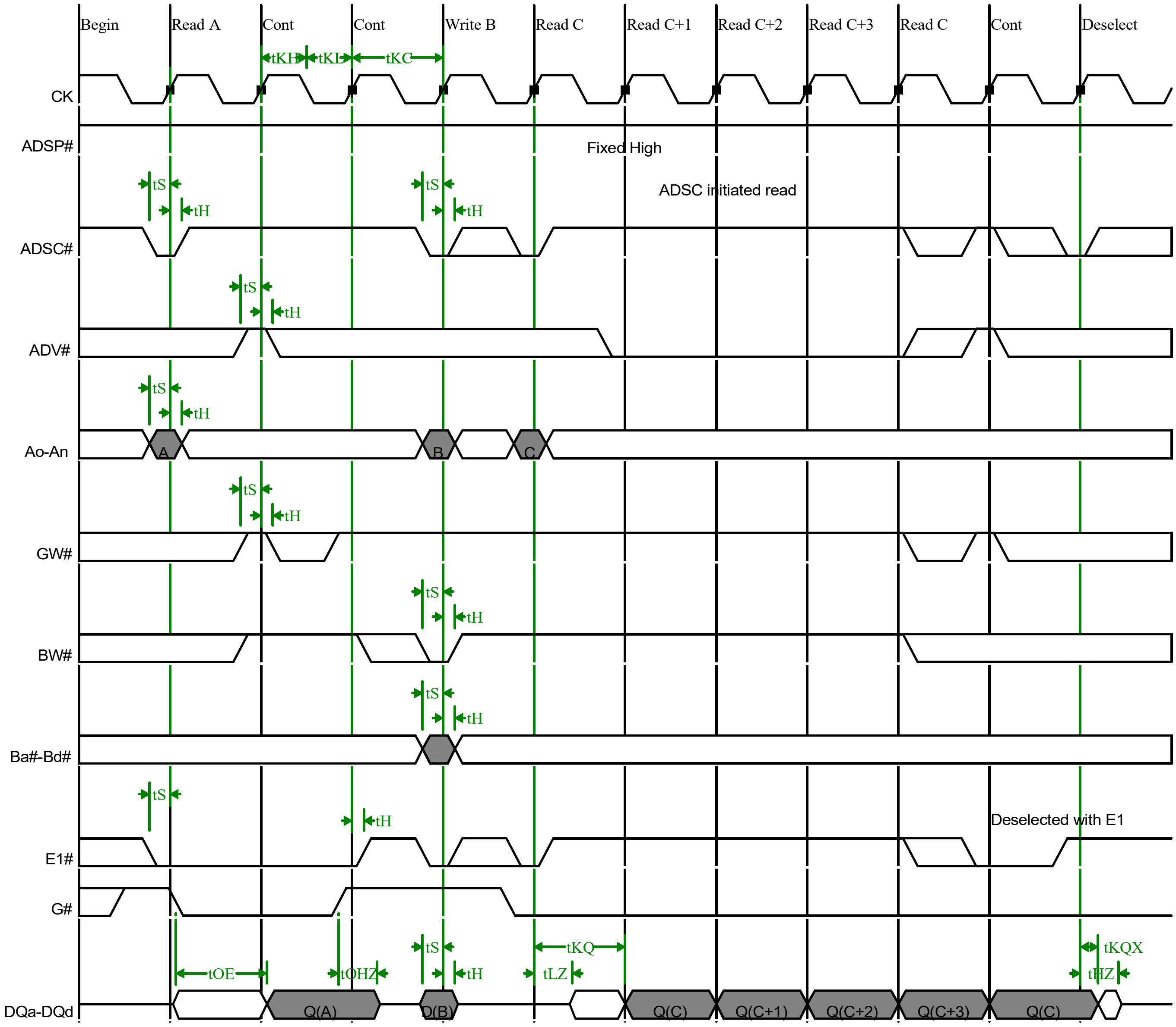
Notes:

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Timing (SCD)



Flow Through Mode Timing (SCD)

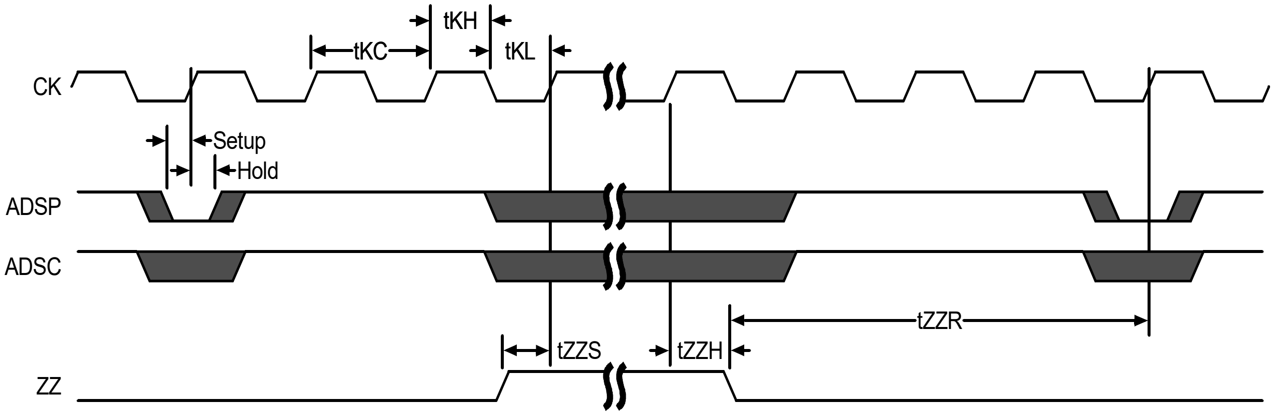


Sleep Mode

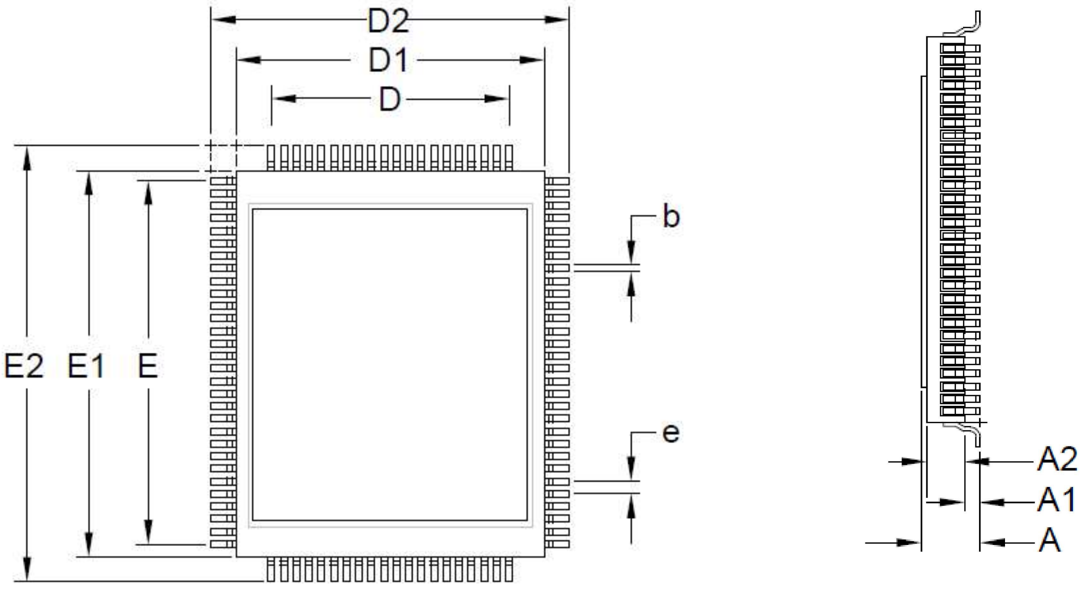
During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



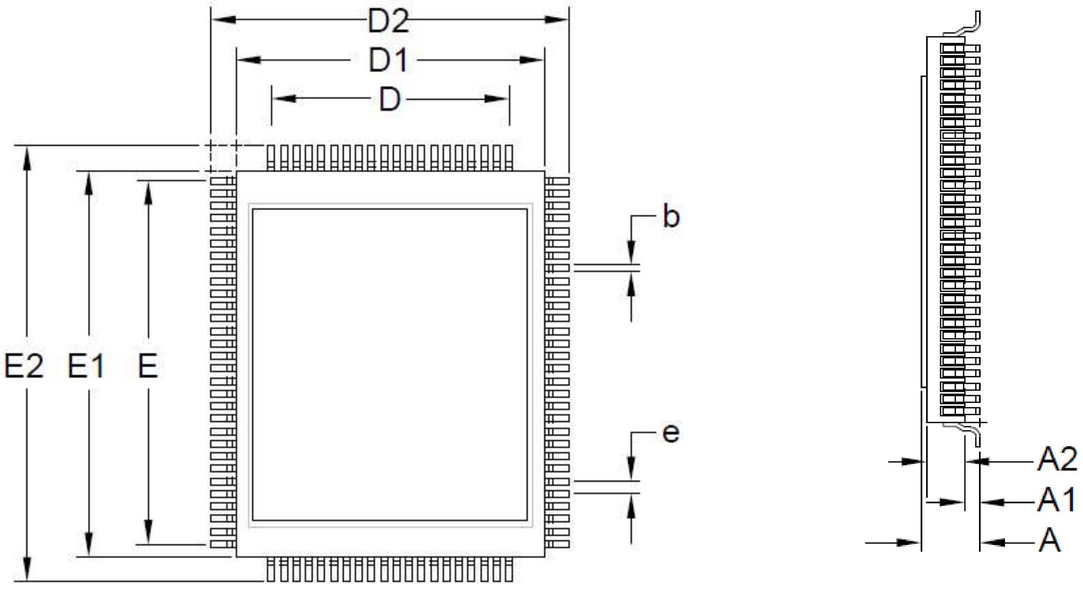
Ceramic QFP Package Drawing (Package CQ)



Symbol	Min.	Max
A	2.84	3.03
A1	0.70	0.80
A2	1.88	1.98
b	0.30	0.35
c	0.19	0.20
D	12.35 BSC	
D1	15.84	16.16
D2	18.14	19.06
E	18.85 BSC	
E1	19.80	20.20
E2	22.10	23.10
e	0.65 BSC	
L	1.15	1.45
L1	0.40	0.70
R	0.19	0.20

Note:
All dimensions are in millimeters (mm).

Ceramic QFP Package Drawing (Package CQ)



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Note:
All dimensions are in millimeters (mm).

Ordering Information—GSI SyncBurst Synchronous SRAM

Org	Part Number	Type	Package	Speed (MHz)	T_J*
144Mb					
4M x 36	GS8132036CQ-333MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
4M x 36	GS8132036CQ-250MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
8M x 18	GS8132018CQ-333MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
8M x 18	GS8132018CQ-250MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
4M x 36	GS8132036CQ-333MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
4M x 36	GS8132036CQ-250MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
8M x 18	GS8132018CQ-333MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
8M x 18	GS8132018CQ-250MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
4M x 36	GS8132036CQ-333MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
4M x 36	GS8132036CQ-250MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
8M x 18	GS8132018CQ-333MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
8M x 18	GS8132018CQ-250MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
72Mb					
2M x 36	GS868036CQ-333MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
2M x 36	GS868036CQ-250MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
4M x 18	GS868018CQ-333MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
4M x 18	GS868018CQ-250MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
2M x 36	GS868036CQ-333MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
2M x 36	GS868036CQ-250MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M

* M = Military Temperature Range

Ordering Information—GSI SyncBurst Synchronous SRAM

Org	Part Number	Type	Package	Speed (MHz)	T_J*
4M x 18	GS868018CQ-333MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
4M x 18	GS868018CQ-250MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
2M x 36	GS868036CQ-333MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
2M x 36	GS868036CQ-250MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
4M x 18	GS868018CQ-333MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
4M x 18	GS868018CQ-250MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
36Mb					
1M x 36	GS836036CQ-333MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
1M x 36	GS836036CQ-250MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
2M x 18	GS836018CQ-333MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	333	M
2M x 18	GS836018CQ-250MS	Pipeline/Flow Through	Ceramic QFP (Engineering Sample)	250	M
1M x 36	GS836036CQ-333MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
1M x 36	GS836036CQ-250MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
2M x 18	GS836018CQ-333MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	333	M
2M x 18	GS836018CQ-250MQ	Pipeline/Flow Through	Ceramic QFP (Class-Q)	250	M
1M x 36	GS836036CQ-333MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
1M x 36	GS836036CQ-250MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M
2M x 18	GS836018CQ-333MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	333	M
2M x 18	GS836018CQ-250MV	Pipeline/Flow Through	Ceramic QFP (Class-V)	250	M

* M = Military Temperature Range

Datasheet Revision History

File Name	Types of Changes Format or Content	Revisions
01836CQ-RAD_r1		Creation of new Rad-Hard datasheet
01836CQ-RAD_r1_01	Content	Added new part numbers to designate qualification nomenclature (S/Q/V) (Rev1.01a: Changed unused address pins to MCL)