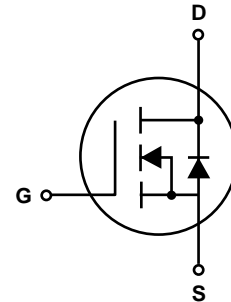
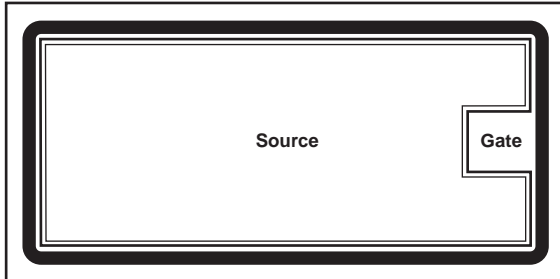


N-Channel Enhancement-Mode MOSFET Die

V_{DS} 20V R_{DS(ON)} 30mΩ I_D 6.0A

TRENCH GENFET™
New Product

Chip Geometry



Physical Characteristics

- Die size : 1800 x 1120µm (70.9 x 44.1 mils)
- Metalization:
Top: Al/Si/Cu
Back: Ti/Ni/Ag
- Metal Thickness:
Top: 3.0µm
Back: 1.4µm
- Die thickness: 9 - 13 mils
- Bonding Area:
Source: Full metalized surface of source region
Gate: 181 x 181µm
- Recommended Wire Bonding:
Source: 2 mil Ø Au wire (3 or more wires preferred)
Gate: 2 mil Ø Au wire

Note: More source wires can further improve performance

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Fast Switching
- High temperature soldering in accordance with CECC802/Reflow guaranteed
- Logic Level
- Ideal for Li ion battery pack applications

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±10	
Continuous Drain Current T _J = 150°C ⁽¹⁾	I _D	T _A = 25°C T _A = 70°C	A
Pulsed Drain Current		I _{DM}	
Continuous Source Current (Diode Conduction) ⁽¹⁾	I _S	1.7	
Maximum Power Dissipation ⁽¹⁾	P _D	T _A = 25°C T _A = 70°C	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	
Maximum Junction-to-Ambient ⁽¹⁾ Thermal Resistance	R _{θJA}	62.5	°C/W

Note: Maximum ratings are based on die packaged in a SO-8 Dual package. Actual rating can increase (or decrease), depending on actual assembly method used

N-Channel Enhancement-Mode MOSFET Die

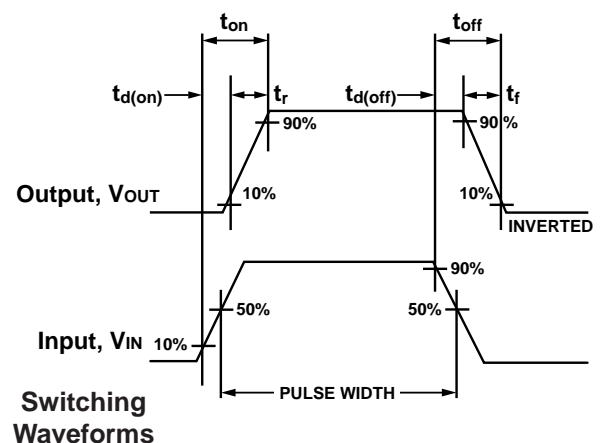
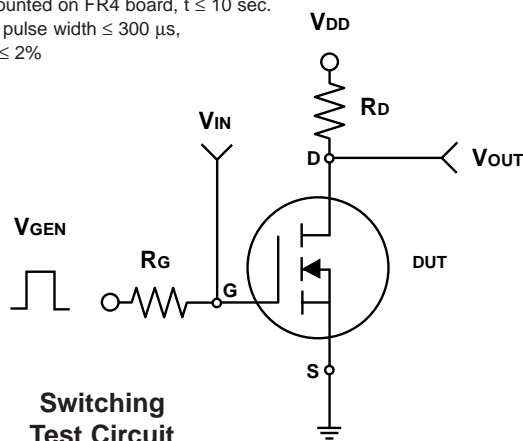
Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	20	–	–	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.5	–	–	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V	–	–	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20V, V _{GS} = 0V	–	–	1	μA
		V _{DS} =20V, V _{GS} =0V, T _J =55°C	–	–	5	
On-State Drain Current ⁽²⁾	I _{D(on)}	V _{DS} ≥ 5V, V _{GS} = 4.5V	20	–	–	A
Drain-Source On-State Resistance ⁽²⁾	R _{DS(on)}	V _{GS} = 4.5V, I _D = 6A	–	22	30	mΩ
		V _{GS} = 2.5V, I _D = 5.2A	–	28	40	
Forward Transconductance ⁽²⁾	g _{fs}	V _{DS} = 10V, I _D = 6A	–	24	–	S
Dynamic						
Total Gate Charge	Q _g	V _{DS} = 10V, V _{GS} = 4.5V I _D = 6A	–	13	40	nC
Gate-Source Charge	Q _{gs}		–	2.2	–	
Gate-Drain Charge	Q _{gd}		–	3	–	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10V, R _L = 10Ω I _D ≈ 1A, V _{GEN} = 4.5V R _G = 6Ω	–	11	60	ns
Rise Time	t _r		–	15	140	
Turn-Off Delay Time	t _{d(off)}		–	43	140	
Fall Time	t _f		–	22	60	
Input Capacitance	C _{iss}	V _{GS} = 0V	–	1240	–	pF
Output Capacitance	C _{oss}	V _{DS} = 10V	–	200	–	
Reverse Transfer Capacitance	C _{rss}	f = 1.0MHz	–	120	–	
Source-Drain Diode						
Diode Forward Voltage ⁽²⁾	V _{SD}	I _S = 1.7A, V _{GS} = 0V	–	0.7	1.3	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7A, di/dt = 100A/μs	–	–	100	ns

Notes:

(1) Surface mounted on FR4 board, t ≤ 10 sec.

(2) Pulse test; pulse width ≤ 300 μs,
duty cycle ≤ 2%



N-Channel Enhancement-Mode MOSFET Die

Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 1 – Output Characteristics

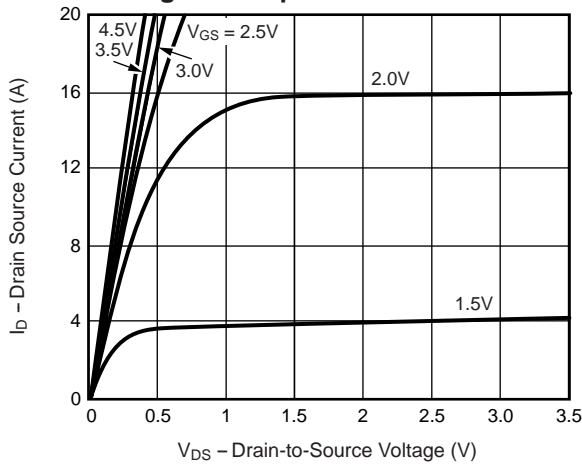


Fig. 2 – Transfer Characteristics

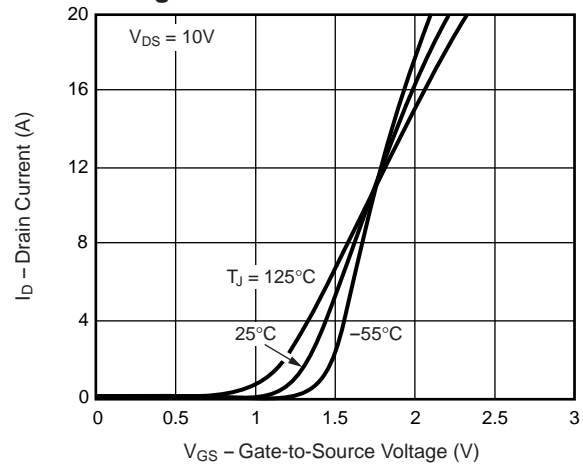


Fig. 3 – Threshold Voltage vs. Temperature

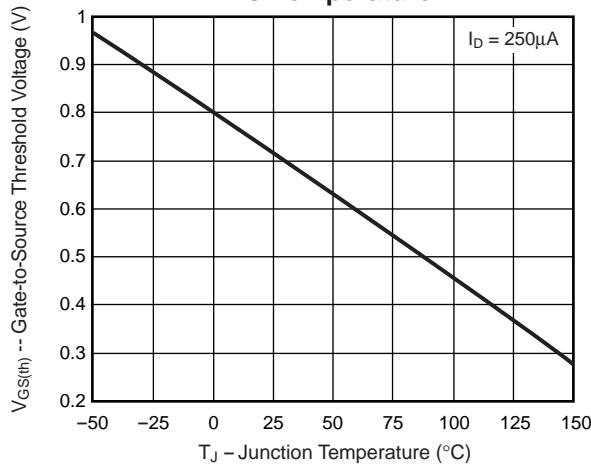


Fig. 4 – On-Resistance vs. Drain Current

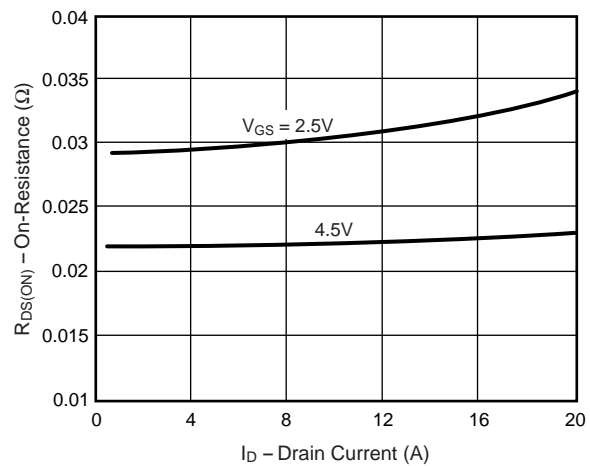
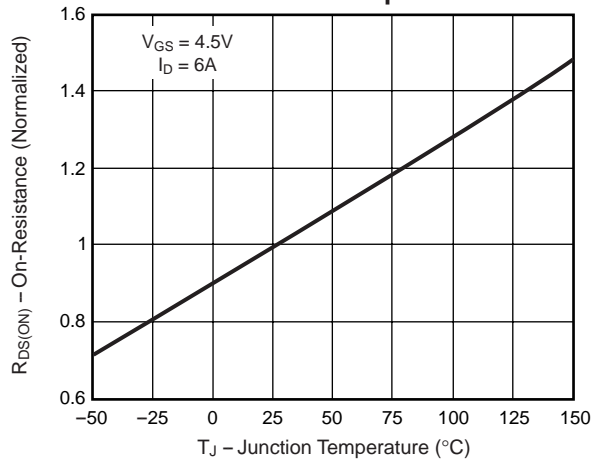


Fig. 5 – On-Resistance vs. Junction Temperature



N-Channel Enhancement-Mode MOSFET Die

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

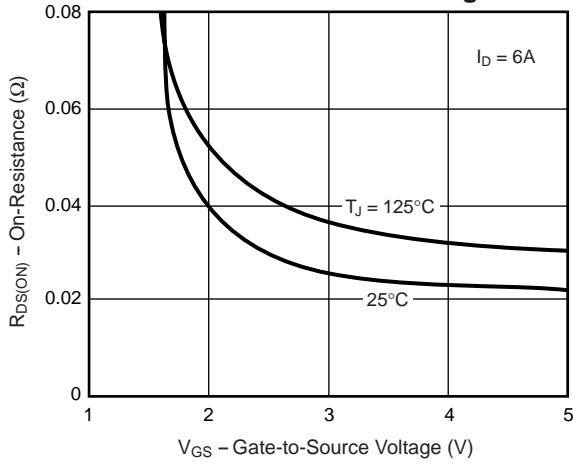


Fig. 7 – Gate Charge

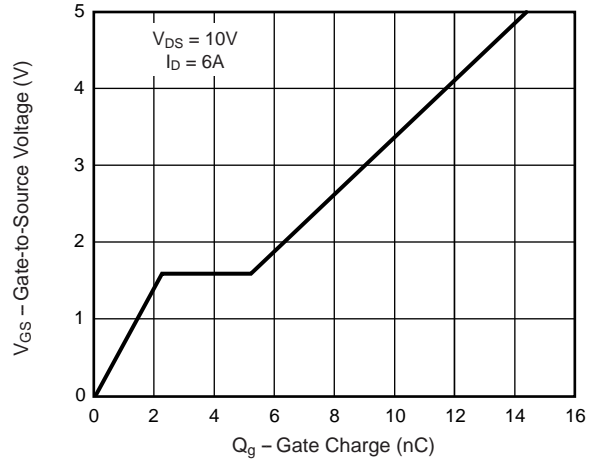


Fig. 8 – Capacitance

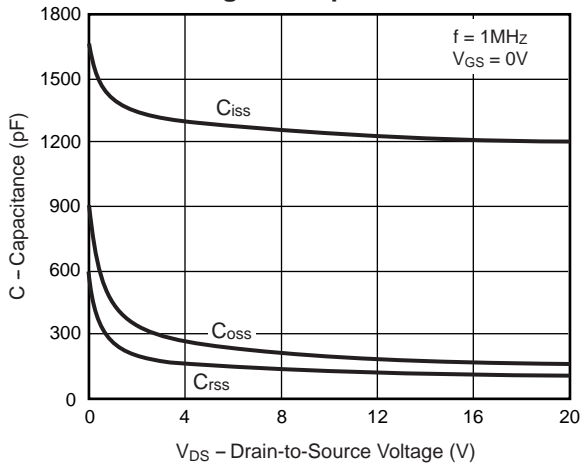
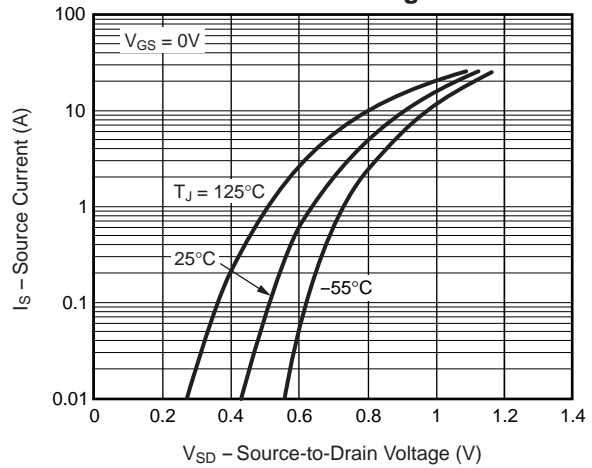


Fig. 9 – Source-Drain Diode Forward Voltage



N-Channel Enhancement-Mode MOSFET Die

Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 10 – Breakdown Voltage vs. Junction Temperature

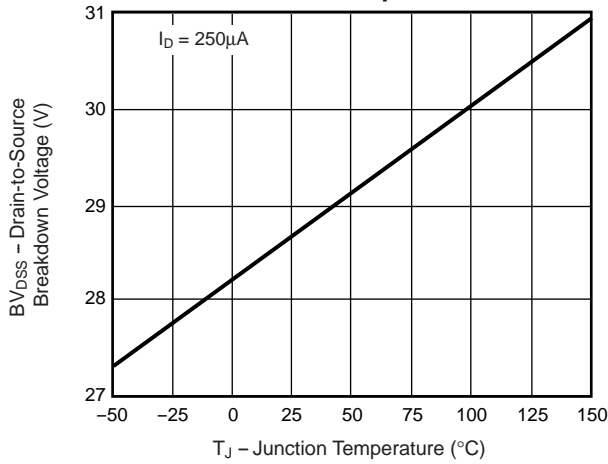


Fig. 11 – Thermal Impedance

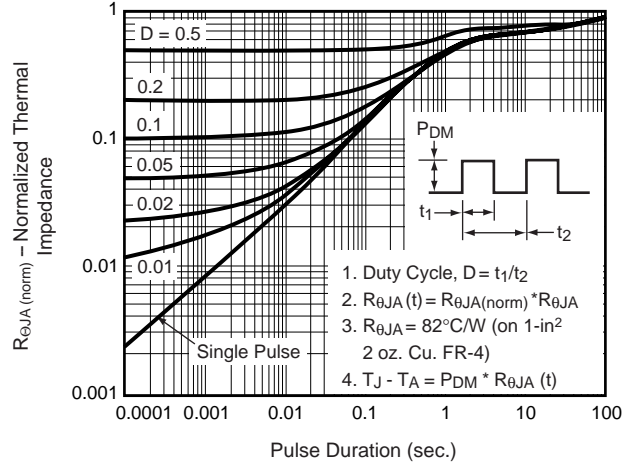


Fig. 12 – Power vs. Pulse Duration

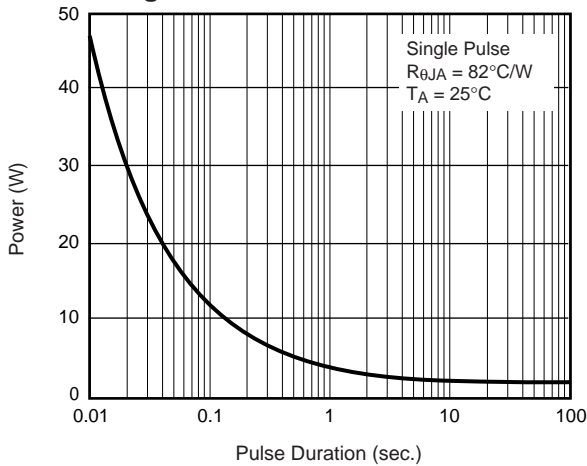


Fig. 13 – Maximum Safe Operating Area

