National Semiconductor

microCMOS

MM82PC12 8-Bit Input/Output Port

July 1987

General Description

The MM82PC12 is a microCMOS 8-bit input/output port contained in a standard 24-pin dual-in-line package. The MM82PC12 can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The MM82PC12 includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

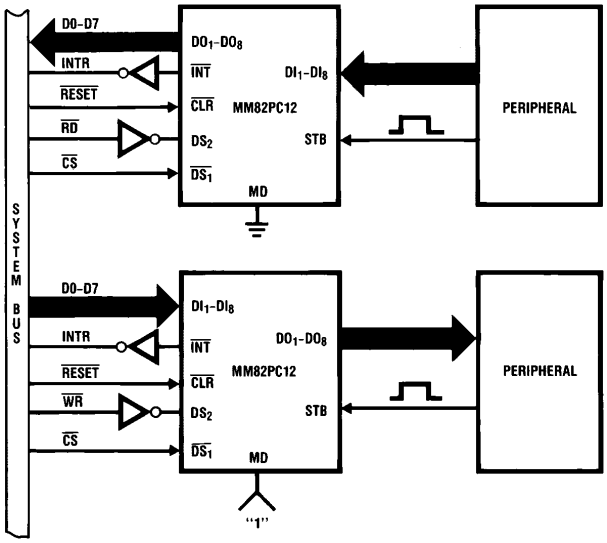
The MM82PC12 is pinout and function compatible with standard INS8212 and DP8212 devices.

For military applications, the MM82PC12 is available with class B screening in accordance with method 5004 of MIL-STD-883.

Features

- Drive capability—150 pF load
- High noise immunity
- Low power dissipation
- Full interface to CMOS logic levels
- microCMOS technology
- TTL drive capability when $V_{CC} = 5V$
- 8-bit data latch and buffer
- Service request flip-flop for generation and control of interrupts
- 1 μA input load current
- Reduces system package count by replacing buffers, latches, and multiplexers in microcomputer systems

System Configuration



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TRI-STATE® is a registered trademark of National Semiconductor Corp.

  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Voltage at Any Pin With Respect to Ground	−0.3V to V_{CC} + 0.3V
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	500 mW
Maximum V_{CC}	7V

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.*

Operating Range V_{CC} = 5V ±10%

Ambient Temperature	
Military	−55°C to +125°C
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

DC Electrical Characteristics

V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC}	V
V_{IL}	Input Low Voltage		0		0.2 V_{CC}	V
V_{OH}	Output High Voltage	V_{CC} = 4.5V, V_{IH} = 4.5V, I_{OH} = −2 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = 5.5V, V_{IL} = 0V, V_{IH} = 5.5V, I_{OL} = 2 mA			0.4	V
I_{IH}	Input High Current	V_{CC} = 5.5V, V_{IN} = 5.5V			10	μA
I_{IL}	Input Low Current	V_{CC} = 5.5V, V_{IN} = 0V			−10	μA
I_{OH}	Output High Current	V_{CC} = 4.5V, V_{OUT} = 2.4V, V_{IH} = 4.5V	−2.0			mA
I_{OL}	Output Low Current	V_{CC} = 5.5V, V_{OUT} = 0.4V, V_{IL} = 0V	2.0			mA
I_{CC}	Power Supply Current	V_{CC} = 5.5V, V_{IH} = 5.5V, V_{IL} = 0V			400	μA
I_{OZL}	TRI-STATE Low Leakage Current	V_{CC} = 5.5V, V_{OUT} = 0V			−10	μA
I_{OZH}	TRI-STATE High Leakage Current	V_{CC} = 4.5V, V_{OUT} = 4.5V			10	μA

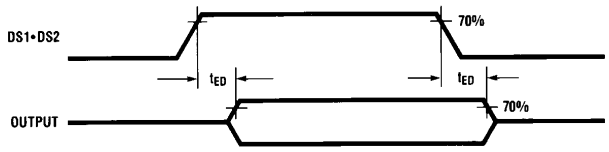
AC Electrical Characteristics

T_A = −55°C to +125°C, V_{CC} = 5V ±10%, GND = 0V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PW}	Pulse Width (STB, DS1 • DS2, CLR)			25	40	ns
t_{PD}	Data In to Data Out			45	60	ns
t_{WE}	Write Enable to Data Out			55	75	ns
t_{SET}	Data Setup Time		15			ns
t_H	Data Hold Time		20			ns
t_R	Reset to Data Out			50	65	ns
t_S	Select to Interrupt			50	65	ns
t_C	Clear to Data Out			45	60	ns
t_{ED}	Output Enable/Disable Time			50	65	ns

Timing Waveforms

Read Timing



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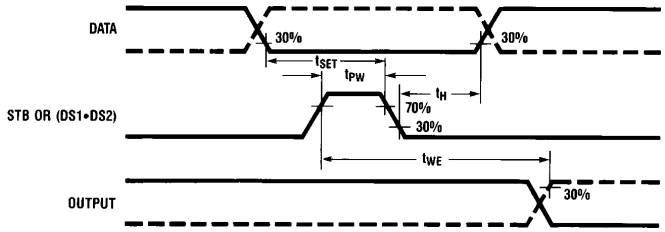
Write Timing



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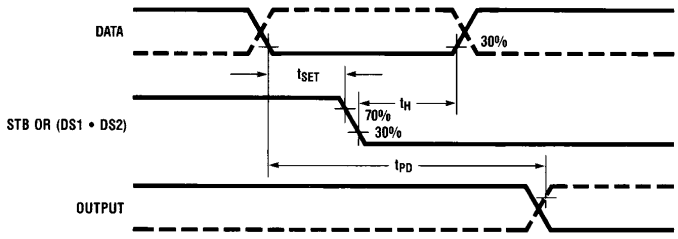
Data Setup, Hold Delay Timing



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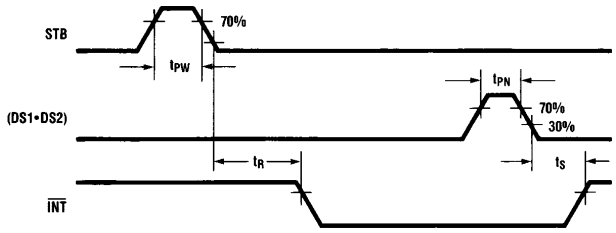
Interrupt Timing



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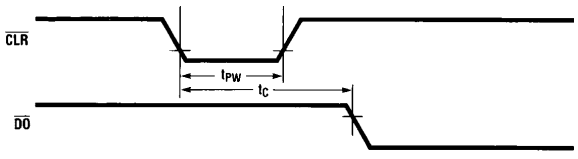
Clear Timing



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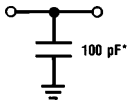
Propagation Delays

Figure 1 illustrates the calculations of a more useful propagation delay. The figure uses a 5V supply with a tolerance of ±10%, ambient temperature of +25°C, and a load capacitance of 100 pF. The AC Characteristics table depicts t_{PD}, at 5V, 25°C, equalling 25 ns. Use the graph in *Figure 1* to get the degradation multiple for 150 pF. The number shown is 1.09. The adjusted propagation delay is, therefore 25 × 1.09 or 27 ns.



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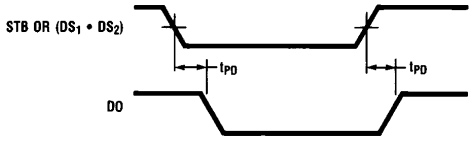
*Including jig and probe capacitance.

Output Test Circuit for Propagation Delays



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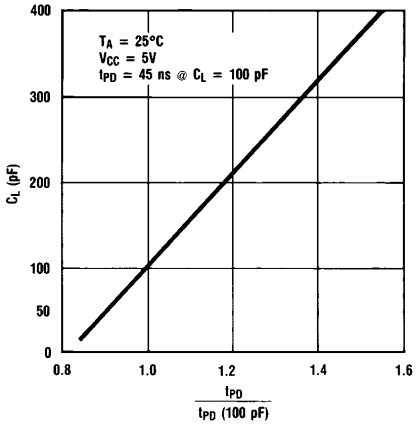

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FIGURE 1. Normalized Typical Propagation Delay vs. Load Capacitance

Pin Descriptions

The following describes the function of all the MM82PC12 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select ($\overline{DS}_1$, DS_2): When $\overline{DS}_1$ is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When MD is high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic ($DS_1 \bullet DS_2$). When MD is low (input mode), the state of the output buffers is determined by the device selection logic ($DS_1 \bullet DS_2$) and the source of the data latch clock input is the strobe (STB) input.

Strobe (STB): STB is used as the data latch clock input when the mode (MD) input is low (input mode). STB is also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI_1–DI_8): Data In is the 8-bit data input to the data latch, which consists of eight D-type flip-flops incorporating a level sensitive clock. While the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. Clear ($\overline{CLR}$) is only effective when the clock is low (latch in the latched state).

Clear ($\overline{CLR}$): When $\overline{CLR}$ is low, the data latch is reset (cleared) if the clock is also low. The clock input high overrides the clear ($\overline{CLR}$) input data latch reset. $\overline{CLR}$ being low also resets the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

Interrupt ($\overline{INT}$): The interrupt pin goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

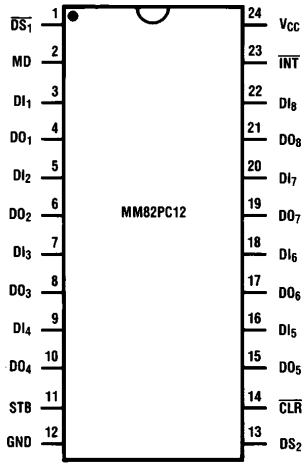
Data Out (DO_1–DO_8): Data Out is the 8-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

Reliability Information

Gate Count 108
Transistor Count 248

Connection Diagrams

Dual-In-Line Package



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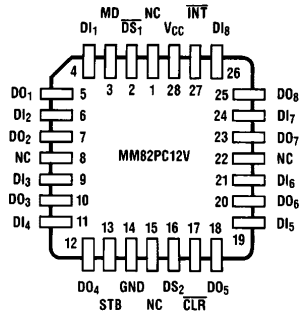
Top View

Order Number MM82PC12J or N
See NS Package Number J24A or N24A

Plastic Chip Carrier



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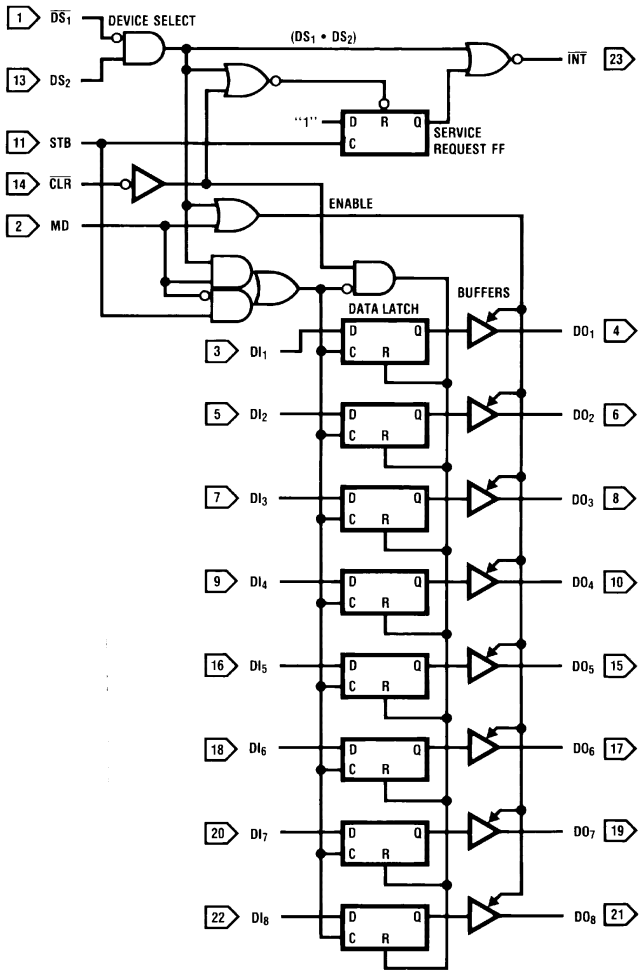
Top View

Order Number MM82PC12V
See NS Package Number V28A

Logic Diagram



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Logic Table A

STB	MD	$DS_1 \cdot DS_2$	Data Out Equals
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

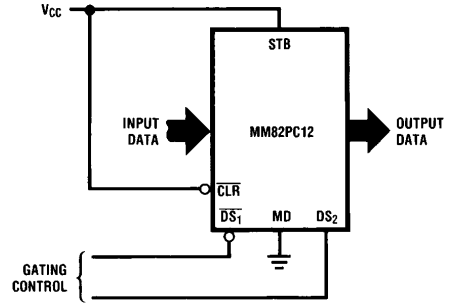
Note: $\overline{CLR}$ ⌐ resets data latch to the output low state. The data latch clock is level sensitive, a low level clock latches the data.

Logic Table B

$\overline{CLR}$	$DS_1 \cdot DS_2$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌐	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

Applications in Microcomputer Systems



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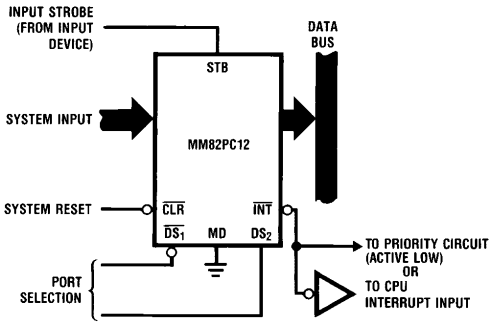
Gated Buffer (TRI-STATE)



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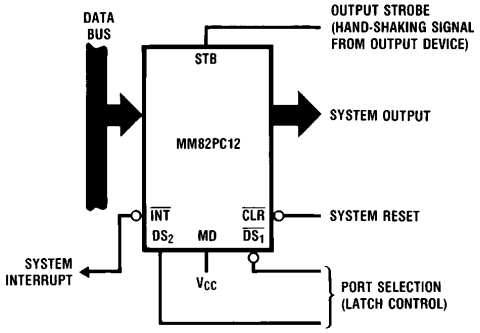
Interrupting Input Port



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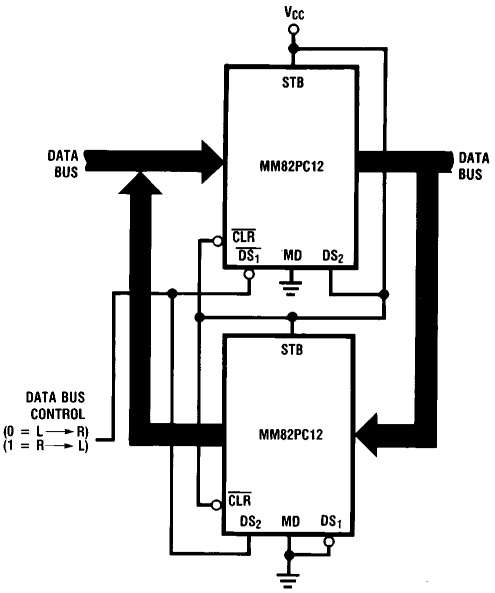
Output Port (with Handshaking)



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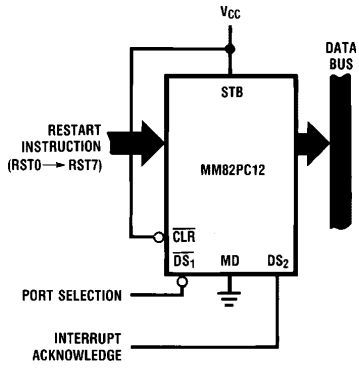
Bidirectional Bus Driver



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Interrupt Instruction Port

Ordering Information

MM82PC12XXX

- **/A+ = A+ Reliability Screening**
- **/883 = MIL-STD-883B Screening (Note 1)**
- **I = Industrial Temperature (−40°C to +85°C)**
- **M = Military Temperature (−55°C to +125°C)**
- **No Designation = Commercial Temperature (0°C to +70°C)**
- **N = Plastic Package**
- **J = Cerdip Package**
- **V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)**

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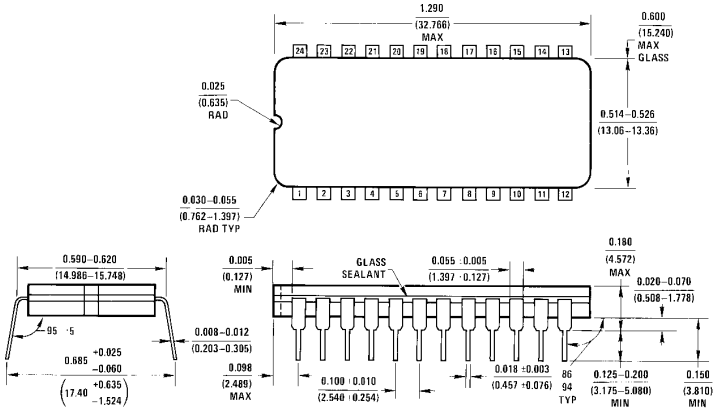
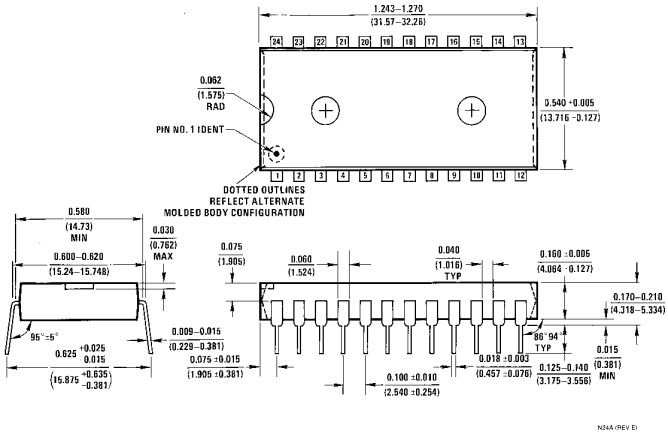
Note 1: Do not specify a temperature option; all parts are screened to military temperature.

Physical Dimensions inches (millimeters)

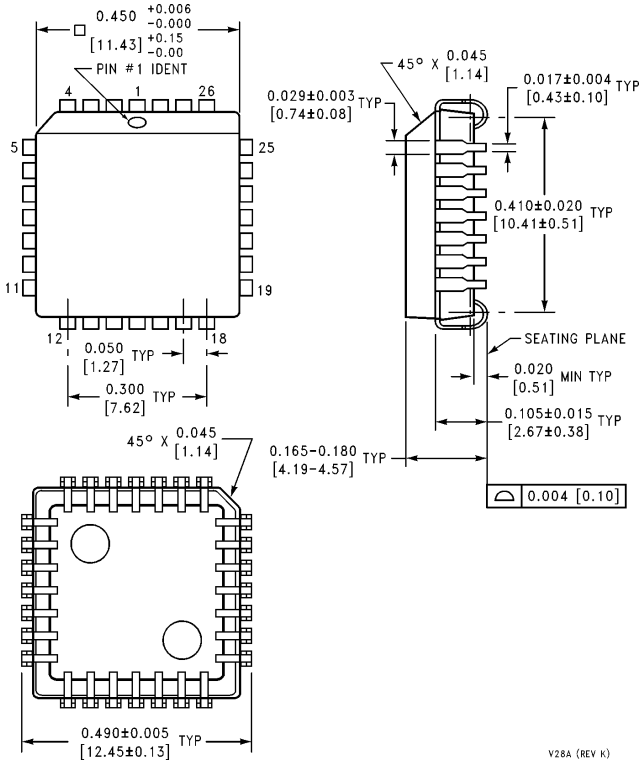


Ceramic Dual-In-Line Package (J)
Order Number MM82PC12J
NS Package J24A



Molded Dual-In-Line Package (N)
Order Number MM82PC12N
NS Package N24A

Physical Dimensions inches (millimeters) (Continued)



Plastic Chip Carrier Package (V)
Order Number MM82PC12V
NS Package V28A

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