

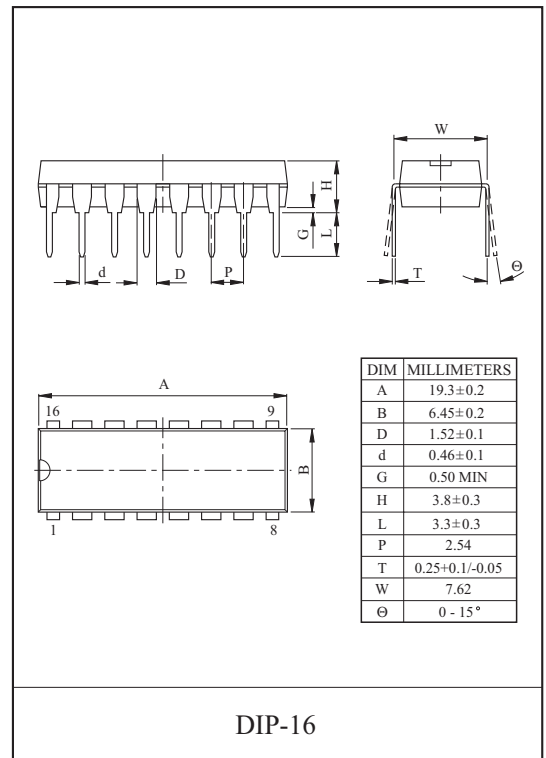
## 7 CIRCUIT DARLINGTON TRANSISTOR ARRAY

### FEATURES

- Output Current : 500mA Max.
- High Sustaining Voltage Outputs : 50V Min.
- Output Clamp Diodes.
- Inputs Compatible With Various Types of Logic.
- PKG Type AP : DIP-16Pin, DIP-16Pin(1) AF : FLP-16Pin
- Suffix U : Qualified to AEC-Q100(Grade 1)

ex) KID6500\*AF-EL/PU

TYPE	INPUT RESISTOR	DESIGNATION
KID65001AP/AF	No (External)	General Purpose
KID65002AP/AF	Zener Diode 7V+10.5k	14 25V P-MOS
KID65003AP/AF	2.7k	TTL, 5V C-MOS
KID65004AP/AF	10.5k	6 15V P-MOS, C-MOS



### DESCRIPTION:

The KID65001AP/AF Series are high-voltage, high-current darlington transistor array comprised of seven NPN darlington pairs. All units feature internal clamp diodes for switching inductive loads.

### MAXIMUM RATINGS (Ta=25 , unless otherwise noted)

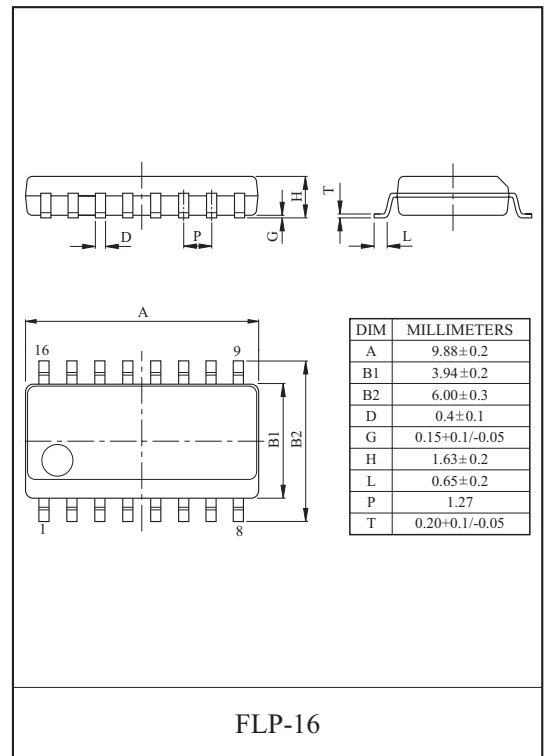
CHARACTERISTIC		SYMBOL	RATING	UNIT
Output Sustaining Voltage		$V_{CE(SUS)}$	50	V
Output Current		$I_{OUT}$	500	mA/ch
Input Voltage		$V_{IN}^{1)}$	-0.5 +30	V
Input Current		$I_{IN}^{2)}$	25	mA
Clamp Diode	Reverse Voltage	$V_R$	50	V
	Forward Current	$I_F$	500	mA
GND Terminal Current		$I_{GND}$	2.8	A
Power Dissipation	AP	$P_D$	1.47	W
	AF		0.54 /0.63 <sup>3)</sup> /1.25 <sup>4)</sup>	W
Operating Temperature		$T_{opr}$	-40 125	
Storage Temperature		$T_{stg}$	-55 150	

1) Except KID65001AP/AF

2) Only KID65001AP/AF

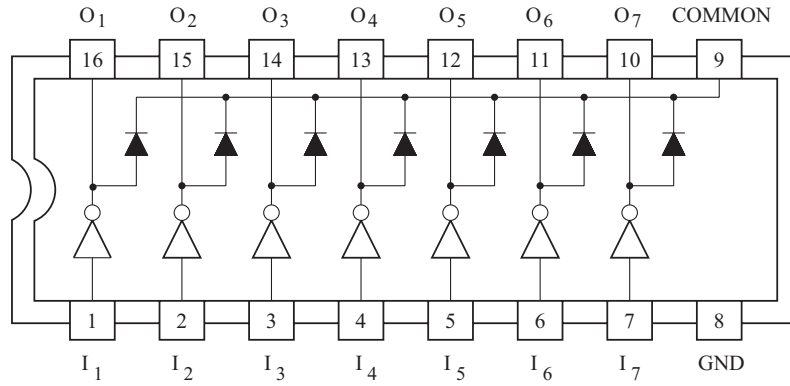
3) On PCB(30 × 30 × 1.6mm, Cu 50%)

4) On PCB (Test Board : JEDEC 2s2p)

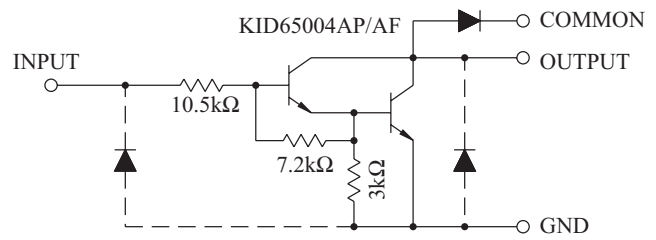
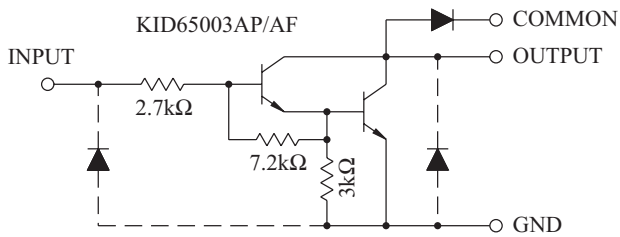
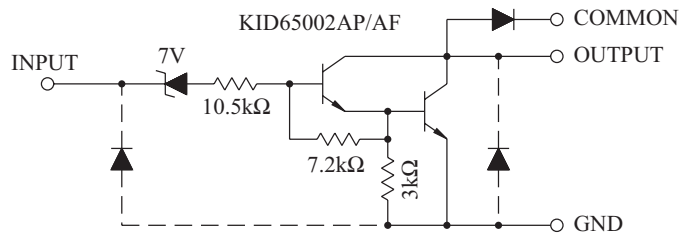
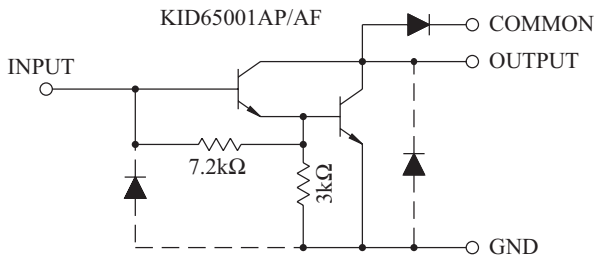


# KID65001AP/AF~KID65004AP/AF

## PIN CONNECTION (TOP VIEW)



## SCHEMATICS (EACH DRIVER)



# KID65001AP/AF~KID65004AP/AF

## RECOMMENDED OPERATING CONDITIONS (Ta=-40 85 )

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage		$V_{CE(SUS)}$	-	0	-	50	V
Output Current	$I_{OUT}$ (AP, Ta=85 )	$I_{OUT}$	T <sub>PW</sub> =25ms, Duty=10%, 7 Circuits	0	-	370	mA
			T <sub>PW</sub> =25ms, Duty=30%, 7 Circuits	0	-	200	
	$I_{OUT}$ (AF, Ta=85 )	$I_{OUT}$	T <sub>PW</sub> =25ms, Duty=10%, 7 Circuits	-	-	290	mA
			T <sub>PW</sub> =25ms, Duty=30%, 7 Circuits	-	-	150	
Input Voltage		$V_{IN}$	Except KID65001AP/AF	0	-	30	V
Input Current		$I_{IN}$	Only KID65001AP/AF	0	-	5	mA
Clamp Diode Reverse Voltage		$V_R$	-	-	-	50	V
Clamp Diode Forward Current		$I_F$	-	-	-	400	mA
Power Dissipation	AP	$P_D$	Ta=85	-	-	0.76	W
	AF		Ta=85	0.28 / 0.32* / 0.65**			

\* On PCB (30 × 30 × 1.6mm, Cu 50%)

\*\* On PCB (Test Board : JEDEC 2s2p)

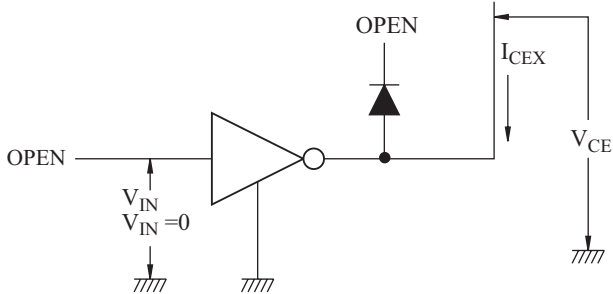
## ELECTRICAL CHARACTERISTICS (Ta=25 , unless otherwise noted)

CHARACTERISTICS		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		$I_{CEX}$	1	$V_{CE}=50V, Ta=25$	-	-	50	μA
				$V_{CE}=50V, Ta=85$	-	-	100	
				$V_{CE}=50V, V_{IN}=6V$	-	-	500	
				$V_{CE}=50V, V_{IN}=1V$	-	-	500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	2	$I_{OUT}=350mA, I_{IN}=500\mu A$	-	1.3	1.6	V
				$I_{OUT}=200mA, I_{IN}=350\mu A$	-	1.1	1.3	
				$I_{OUT}=100mA, I_{IN}=250\mu A$	-	0.9	1.1	
Input Current (Output On)	KID65002AP/AF	$I_{IN(ON)}$	3	$V_{IN}=17V$	-	0.82	1.25	mA
	KID65003AP/AF			$V_{IN}=3.85V$	-	0.93	1.35	
	KID65004AP/AF			$V_{IN}=5V$	-	0.35	0.5	
				$V_{IN}=12V$	-	1.0	1.45	
Input Current (Output OFF)		$I_{IN(OFF)}$	4	$I_{OUT}=500\mu A, Ta=85$	50	65	-	μA
Input Voltage	KID65002AP/AF	$V_{IN(ON)}$	5	$V_{CE}=2V, I_{OUT}=300mA$	-	-	13	V
	KID65003AP/AF			$V_{CE}=2V, I_{OUT}=200mA$	-	-	2.4	
				$V_{CE}=2V, I_{OUT}=250mA$	-	-	2.7	
	KID65004AP/AF			$V_{CE}=2V, I_{OUT}=300mA$	-	-	3.0	
				$V_{CE}=2V, I_{OUT}=125mA$	-	-	5.0	
				$V_{CE}=2V, I_{OUT}=200mA$	-	-	6.0	
	KID65002AP/AF			$V_{IN(OFF)}$	5	$V_{CE}=2V, I_{OUT}=275mA$	-	
		$V_{CE}=2V, I_{OUT}=350mA$	-			-	8.0	
		-	0			-	7.4	
	KID65003AP/AF	-	0	-	0.7			
KID65004AP/AF	-	0	-	1.0				
DC Current Transfer Ratio		$h_{FE}$	2	$V_{CE}=2V, I_{OUT}=350mA$	1000	-	-	
Clamp Diode Reverse Current		$I_R$	6	$V_R=50V, Ta=25$	-	-	50	μA
				$V_R=50V, Ta=85$	-	-	100	
Clamp Diode Forward Voltage		$V_F$	7	$I_F=350mA$	-	-	2.0	V
Input Capacitance		$C_{IN}$	-	-	-	15	-	pF
Turn-ON Delay		$t_{ON}$	8	$V_{OUT}=50V, R_L=163\Omega, C_L=15pF$	-	0.1	-	μs
Turn-OFF Delay		$t_{OFF}$			-	0.2	-	

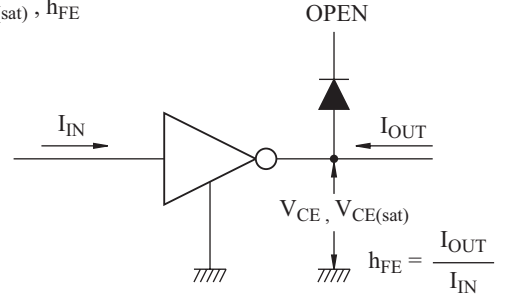
# KID65001AP/AF~KID65004AP/AF

## TEST CIRCUIT

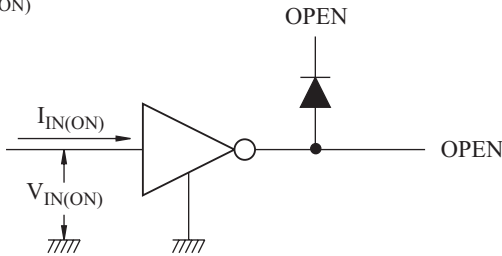
1.  $I_{CEX}$



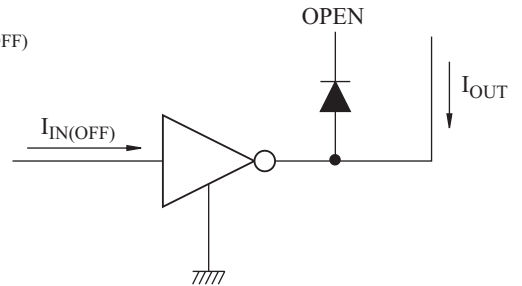
2.  $V_{CE(sat)}, h_{FE}$



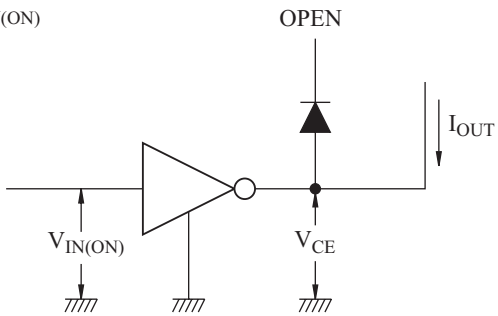
3.  $I_{IN(ON)}$



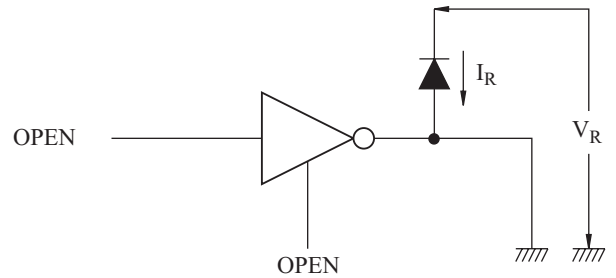
4.  $I_{IN(OFF)}$



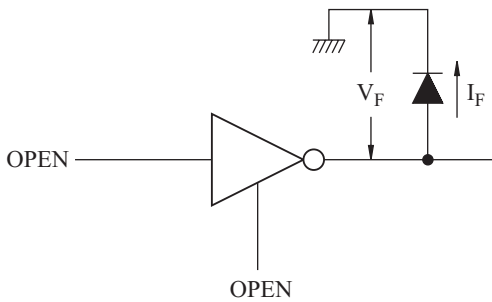
5.  $V_{IN(ON)}$



6.  $I_R$

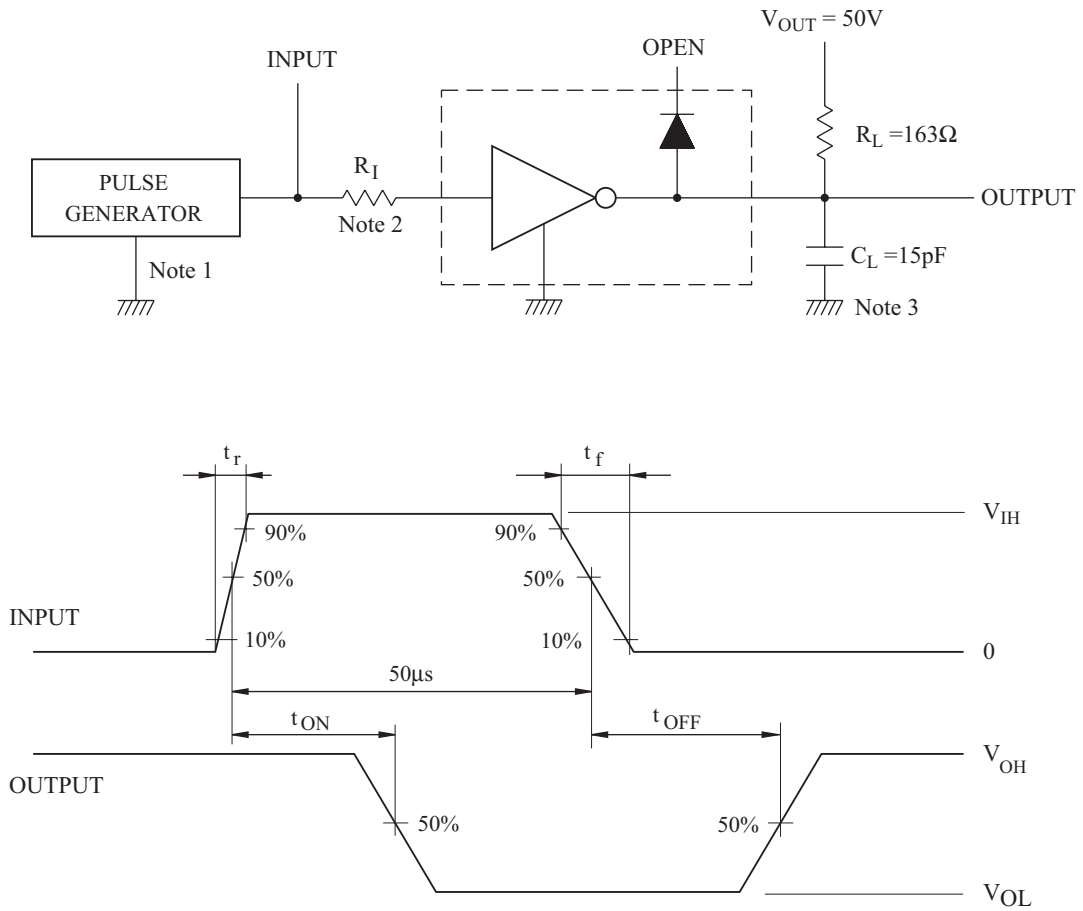


7.  $V_F$



# KID65001AP/AF~KID65004AP/AF

## 8. $t_{ON}$ , $t_{OFF}$



Notes : 1. Pulse Width  $50\mu s$ , Duty Cycle 10%  
Output Impedance  $50\Omega$ ,  $t_r$  5ns,  $t_f$  10ns

2. See below

### Input Conditions

Type Number	$R_I$	$V_{IH}$
KID65001AP/AF	2.7k	3V
KID65002AP/AF	0	13V
KID65003AP/AF	0	3V
KID65004AP/AF	0	8V

3.  $C_L$  includes probe and Jig capacitance.

# KID65001AP/AF~KID65004AP/AF

Fig. 1  $I_{OUT}$  - DUTY CYCLE

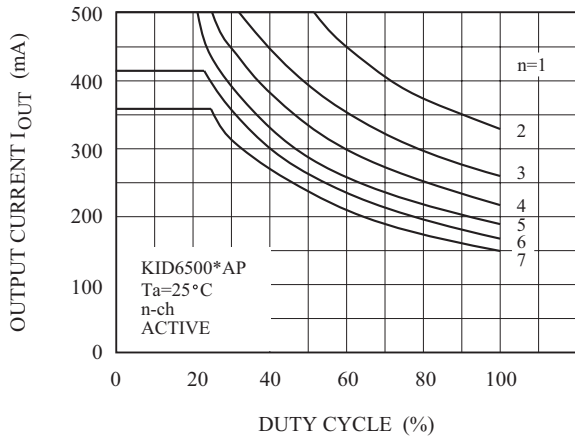


Fig. 2  $I_{OUT}$  - DUTY CYCLE

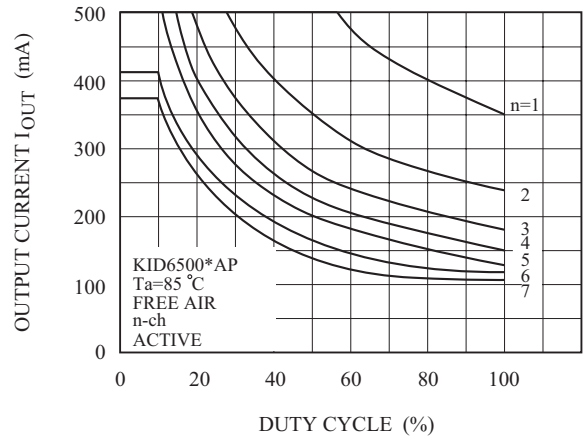


Fig. 3  $I_{OUT}$  - DUTY CYCLE

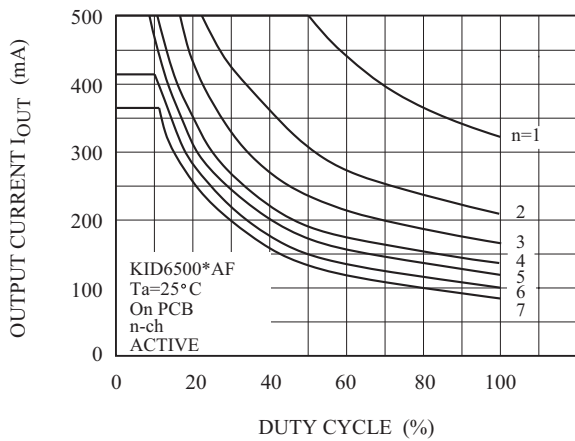


Fig. 4  $I_{OUT}$  - DUTY CYCLE

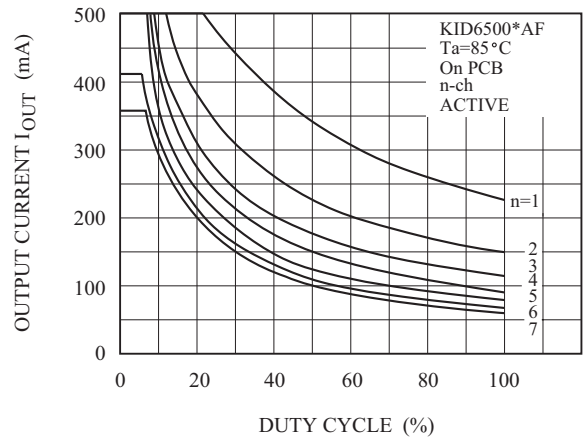


Fig. 5  $I_{IN}$  -  $V_{IN}$

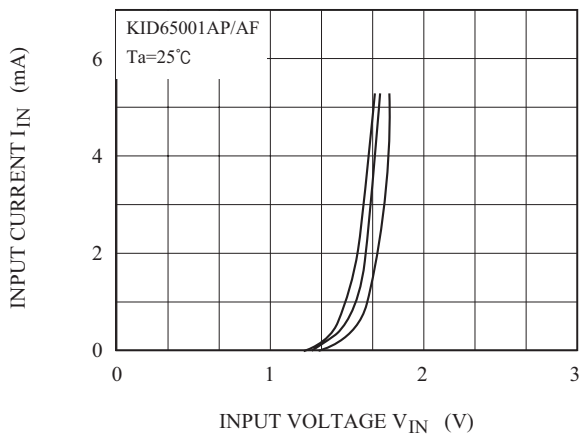
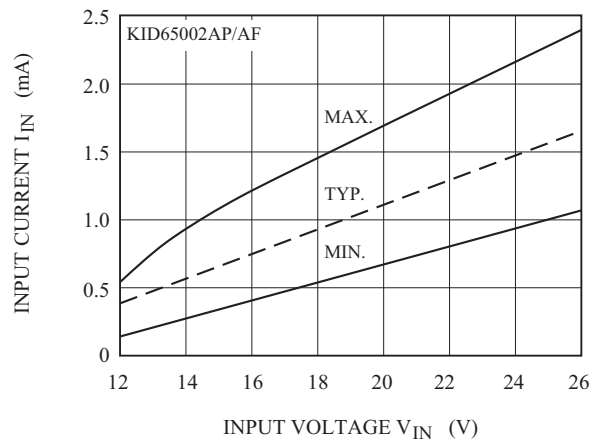


Fig. 6  $I_{IN}$  -  $V_{IN}$



# KID65001AP/AF~KID65004AP/AF

Fig. 7  $I_{IN} - V_{IN}$

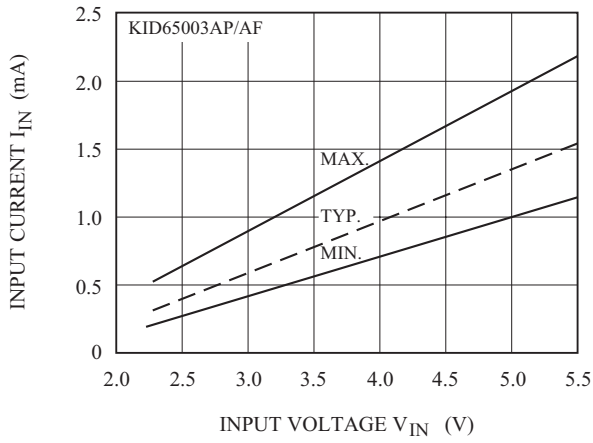


Fig. 8  $I_{IN} - V_{IN}$

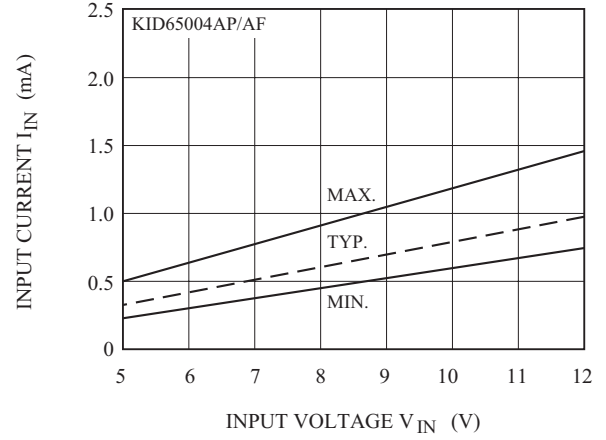


Fig. 9  $I_{OUT} - V_{CE(sat)}$

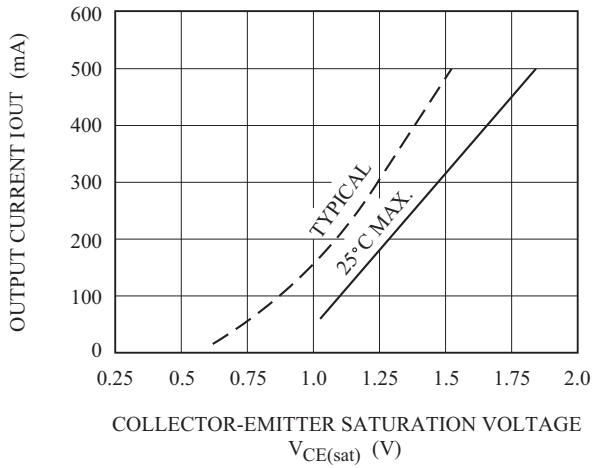


Fig. 10  $h_{FE} - I_{OUT}$

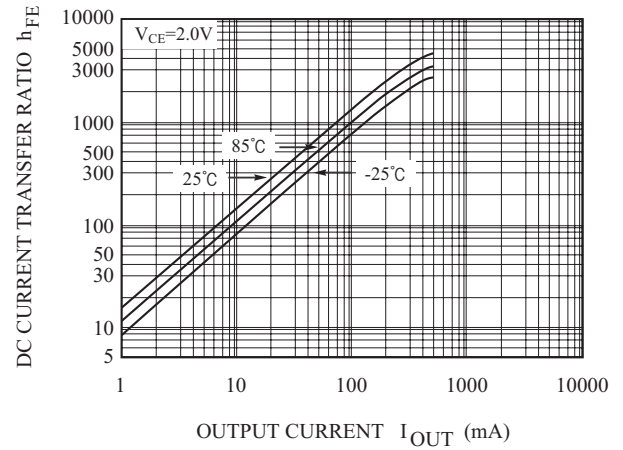


Fig. 11  $I_F - V_F$

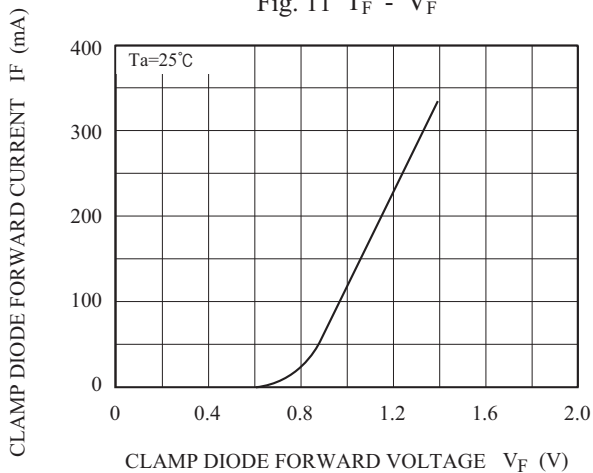


Fig. 12  $P_D - T_a$

