FINAL

Am29F040

4 Megabit (524,288 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% for read and write operations**
  - — Minimizes system level power requirements
- **Compatible with JEDEC-standards**
  - — Pinout and software compatible with single-power-supply Flash
  - — Superior inadvertent write protection
- **Package options**
  - — 32-pin PLCC
  - — 32-pin TSOP
  - — 32-pin PDIP
- **Minimum 100,000 write/erase cycles guaranteed**
- **High performance**
  - — 55 ns maximum access time
- **Sector erase architecture**
  - — Uniform sectors of 64 Kbytes each
  - — Any combination of sectors can be erased. Also supports full chip erase.
- **Sector protection**
  - — Hardware method that disables any combination of sectors from write or erase operations
- **Embedded Erase Algorithms**
  - — Automatically preprograms and erases the chip or any combination of sectors
- **Embedded Program Algorithms**
  - — Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Erase suspend/resume**
  - — Supports reading data from a sector not being erased
- **Low power consumption**
  - — 20 mA typical active read current
  - — 30 mA typical program/erase current
- **Enhanced power management for standby mode**
  - — <1 µA typical standby current
  - — Standard access time from standby mode

GENERAL DESCRIPTION

The Am29F040 is a 4 Mbit, 5.0 Volt-only Flash memory organized as 512 Kbytes of 8 bits each. The Am29F040 is offered in a 32-pin package. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F040 offers access times between 55 ns and 150 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F040 is entirely command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 Volt Flash or EPROM devices.

The Am29F040 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

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Any individual sector is typically erased and verified in 1.0 seconds (if already completely preprogrammed).

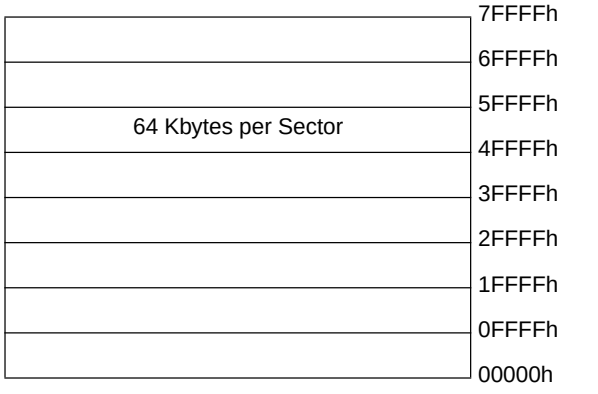
This device also features a sector erase architecture. The sector mode allows for 64K byte blocks of memory to be erased and reprogrammed without affecting other blocks. The Am29F040 is erased when shipped from the factory.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F040 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Flexible Sector-Erase Architecture

- Eight 64 Kbyte sectors
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable



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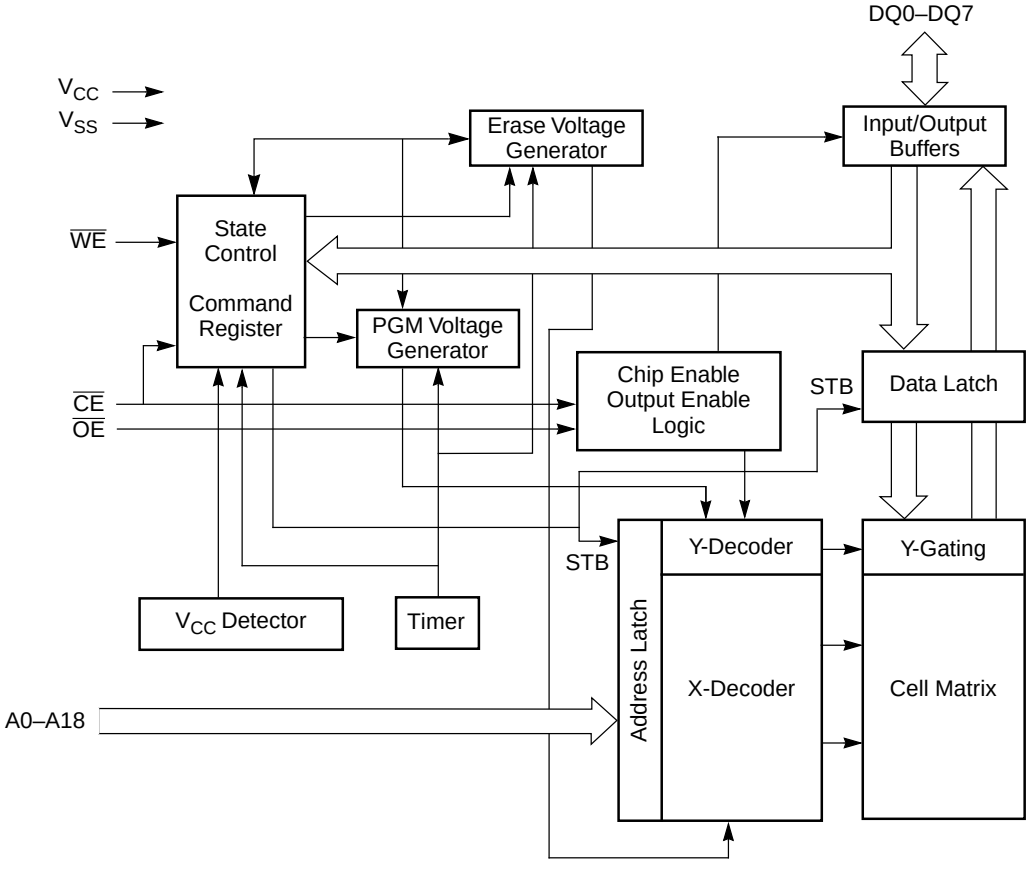
PRODUCT SELECTOR GUIDE

Family Part No:	**Am29F040**				
Ordering Part No: V_{CC} = 5.0 V ± 5%	**-55**				
V_{CC} = 5.0 V ± 10%		**-70**	**-90**	**-120**	**-150**
Max Access Time (ns)	55	70	90	120	150
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150
$\overline{OE}$ ($\overline{G}$) Access (ns)	25	30	35	50	55

BLOCK DIAGRAM



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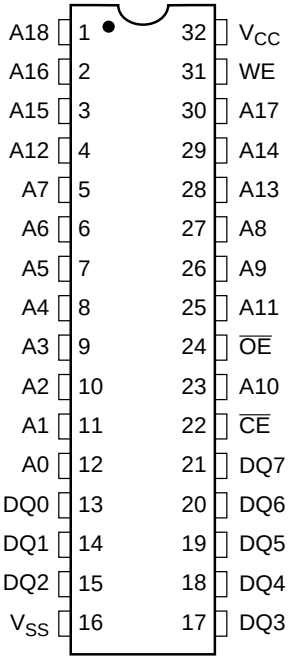
CONNECTION DIAGRAMS

PDIP



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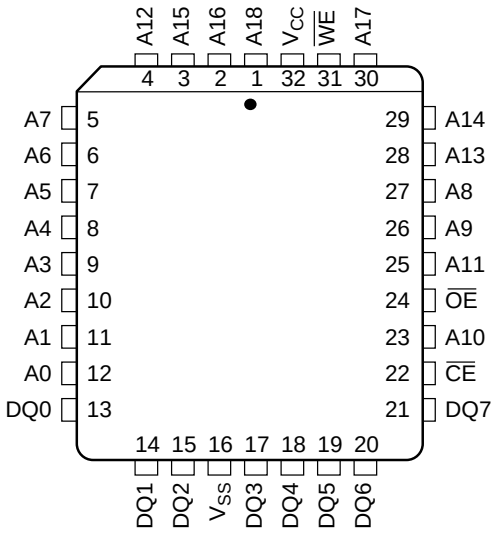
PLCC



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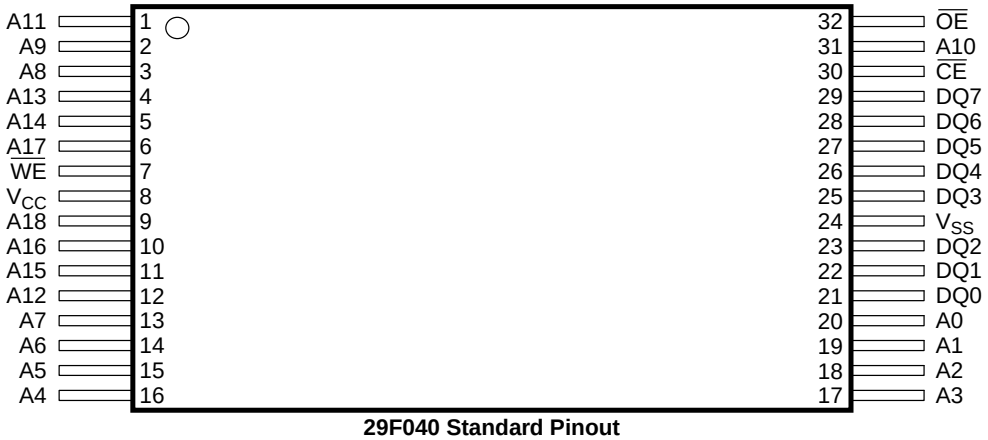
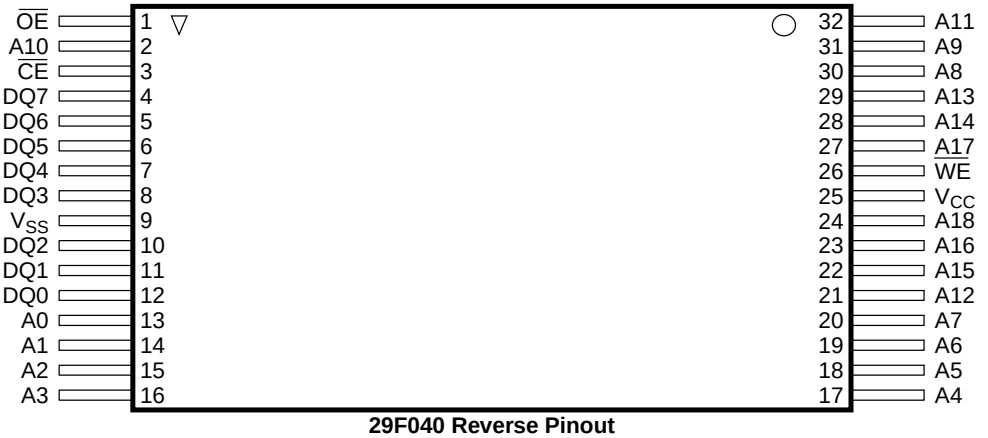
TSOP



29F040 Standard Pinout



29F040 Reverse Pinout

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PIN CONFIGURATION

A0–A18 = Address Inputs

DQ0–DQ7 = Data Input/Output

$\overline{CE}$ = Chip Enable

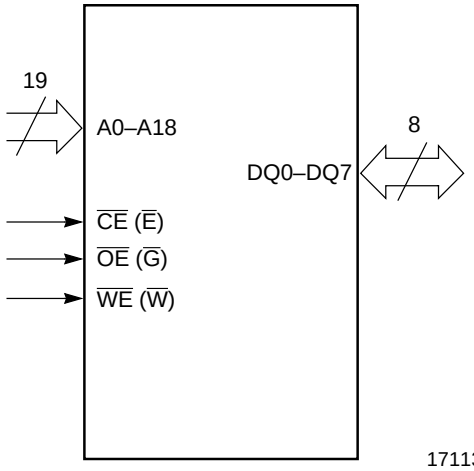
$\overline{OE}$ = Output Enable

$\overline{WE}$ = Write Enable

V_{SS} = Device Ground

V_{CC} = Device Power Supply (5.0 V ±10% or ±5%)

LOGIC SYMBOL



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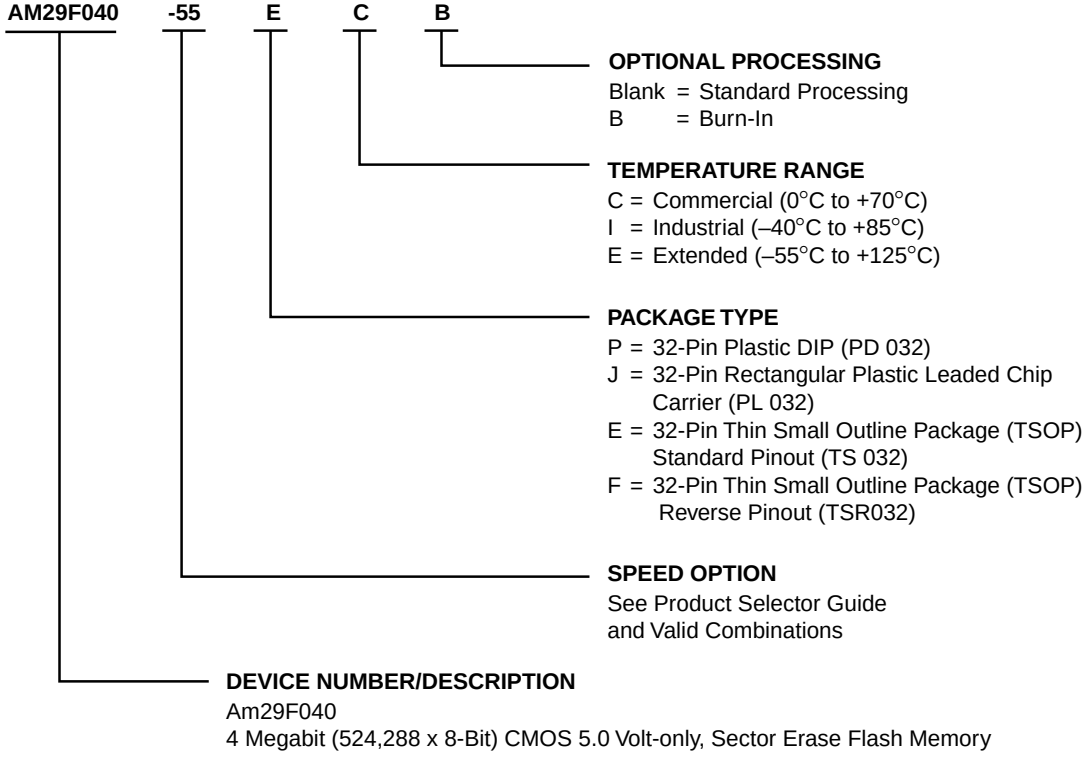
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM29F040-55	JC, JI, JE, EC, EI, EE, FC, FI, FE
AM29F040-70	
AM29F040-90	PC, PCB, PI, PIB, PE, PEB, JC, JCB, JI, JIB, JE, JEB, EC, ECB, EI, EIB, EE, EEB, FC, FCB, FI, FIB, P11 FE, FEB
AM29F040-120	
AM29F040-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1. Am29F040 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	I/O
Autoselect Manufacturer Code (Note 1)	L	L	H	L	L	L	V_{ID}	Code
Autoselect Device Code (Note 1)	L	L	H	H	L	L	V_{ID}	Code
Read (Note 4)	L	L	H	A0	A1	A6	A9	RD
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	PD (Note 2)
Verify Sector Protect (Note 3)	L	L	H	L	H	L	V_{ID}	Code
Autoselect Device Unprotect Code	L	L	H	H	H	L	V_{ID}	Code

Legend:

L = Logic 0, H = Logic 1, X = Don't Care. See DC Characteristics for voltage levels.

Notes:

1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 2 and 4.*
2. *Refer to Table 3 for valid PD (Program Data) during a write operation.*
3. *Refer to the section on Sector Protection.*
4. *$\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.*

Read Mode

The Am29F040 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

The Am29F040 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), when the current consumed is less than 5 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, for instances when the Am29F040 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 4 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (AMD = 01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F040 = A4H). All identifiers for manufacturer and device exhibit odd parity with the MSB (DQ7) defined as the parity bit. See Table 2.

Table 2. Am29F040 Autoselect Codes

Type	A18	A17	A16	A6	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer ID	X	X	X	V_{IL}	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Am29F040 Device ID	X	X	X	V_{IL}	V_{IL}	V_{IH}	A4H	1	0	1	0	0	1	0	0
Sector Protection	Sector Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

**Outputs 01H at protected sector addresses*

Table 3. Sector Addresses

	A18	A17	A16	Address Range
SA0	0	0	0	00000h–0FFFFh
SA1	0	0	1	10000h–1FFFFh
SA2	0	1	0	20000h–2FFFFh
SA3	0	1	1	30000h–3FFFFh
SA4	1	0	0	40000h–4FFFFh
SA5	1	0	1	50000h–5FFFFh
SA6	1	1	0	60000h–6FFFFh
SA7	1	1	1	70000h–7FFFFh

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/ Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F040 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 8). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (AMD's ExpressFlash™ Service).

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A17, and A18) are used to select the desired sector. The device produces a logical "1" at DQ0 for a protected sector and a logical "0" for an unprotected sector. See Table 2 for Autoselect codes.

Sector Unprotect

The Am29F040 also features a sector unprotect mode so that a protected sector may be unprotected to incorporate any changes in the code. The sector unprotect is enabled using programming equipment at the user's site.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to read mode. Table 4 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable).

Table 4. Am29F040 Command Definitions

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXXH	F0H										
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H	00H	01H				
								01H	A4H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care), Data (30H)											

Notes:

1. *Address bits A15, A16, A17, and A18 = X = Don't Care for all address commands except for Program Address (PA), Sector Address (SA), Read Address (RA), and autoselect sector protect verify.*
2. *Bus operations are defined in Table 1.*
3. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A18, A17, A16 will uniquely select any sector (see Table 3).
4. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
5. *Read from non-erasing sectors is allowed in the Erase Suspend mode.*

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains a command autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code A4H (see Table 2). All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

Scanning the sector addresses (A16, A17, A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program setup command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The

rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may cause the device to exceed programming time limits (DQ5 = 1) or result in an apparent success, according to the data polling algorithm, but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "setup" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The chip erase is performed sequentially one sector at a time. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "setup" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period resets the device to read mode, ignoring the previous command string. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode. *During the execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will be ignored.* $\overline{Data}$ polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writing the Erase Suspend command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Any other command written during the Erase Suspend mode will be ignored except the Erase Resume command. Writing the Erase Resume command resumes the erase operation. The addresses are "don't-cares" when writing the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 15 μs to suspend the erase operation. When the device has entered the erase-suspended mode, DQ7 bit will be at logic "1", and DQ6 will stop toggling. The user must use the address of the erasing sector for reading DQ6 and DQ7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Write Operation Status

Table 5. Write Operation Status

Status			DQ7	DQ6	DQ5	DQ3
In Progress	Byte Programming in Embedded Algorithm		$\overline{DQ7}$	Toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1
	Erase Suspended Mode	Erase Suspended Sector	1	No Toggle	0	1
		Non-Erase Suspended Sector	Data	Data	Data	Data
Exceeded Time Limits	Byte-Programming in Embedded Algorithm		$\overline{DQ7}$	Toggle	1	0
	Embedded Erase Algorithm		0	Toggle	1	1

DQ7

$\overline{\text{Data}}$ Polling

The Am29F040 device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device produces the compliment of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, reading the device produces the true data last written to DQ7. During the Embedded Erase Algorithm, reading the device produces a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm, reading the device produces a "1" at the DQ7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ7) is shown in Figure 3.

For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. Data Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the Am29F040 data pins (DQ7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, or sector erase time-out (see Table 5).

See Figure 12 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ6

Toggle Bit

The Am29F040 also features the “Toggle Bit” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ6 to toggle.

See Figure 13 for the Toggle Bit timing specifications and diagrams.

DQ5

Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a “1”. This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 1.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a “1” to a location previously programmed to “0”. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a “1”. Please note that this is not a device failure condition since the device was incorrectly used.

DQ3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high (“1”) the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low (“0”), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the command may not have been accepted.

Refer to Table 5, Write Operation Status.

Data Protection

The Am29F040 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, the Am29F040 locks out write cycles for $V_{CC} < V_{LKO}$ (see DC Characteristics section for voltages). When $V_{CC} < V_{LKO}$, the command register is disabled, all internal program/erase circuits are disabled, and the device resets to the read mode. The Am29F040 ignores all writes until $V_{CC} > V_{LKO}$. The user must ensure that the control pins are in the correct logic state when $V_{CC} > V_{LKO}$ to prevent unintentional writes.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

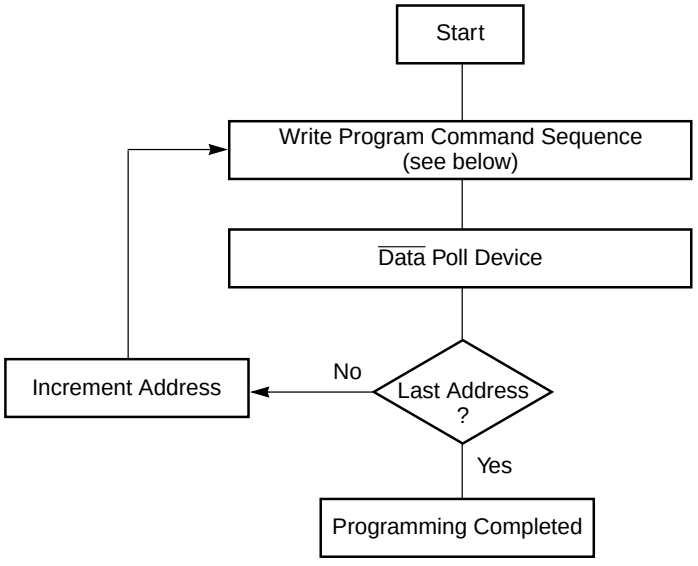
Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

Sectors of the Am29F040 may be hardware protected using programming equipment at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

EMBEDDED ALGORITHMS



Program Command Sequence (Address/Command):

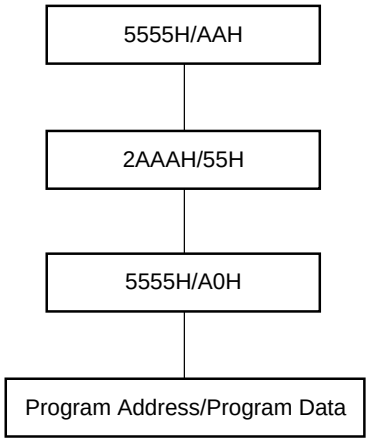


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Figure 1. Embedded Programming Algorithm

EMBEDDED ALGORITHMS

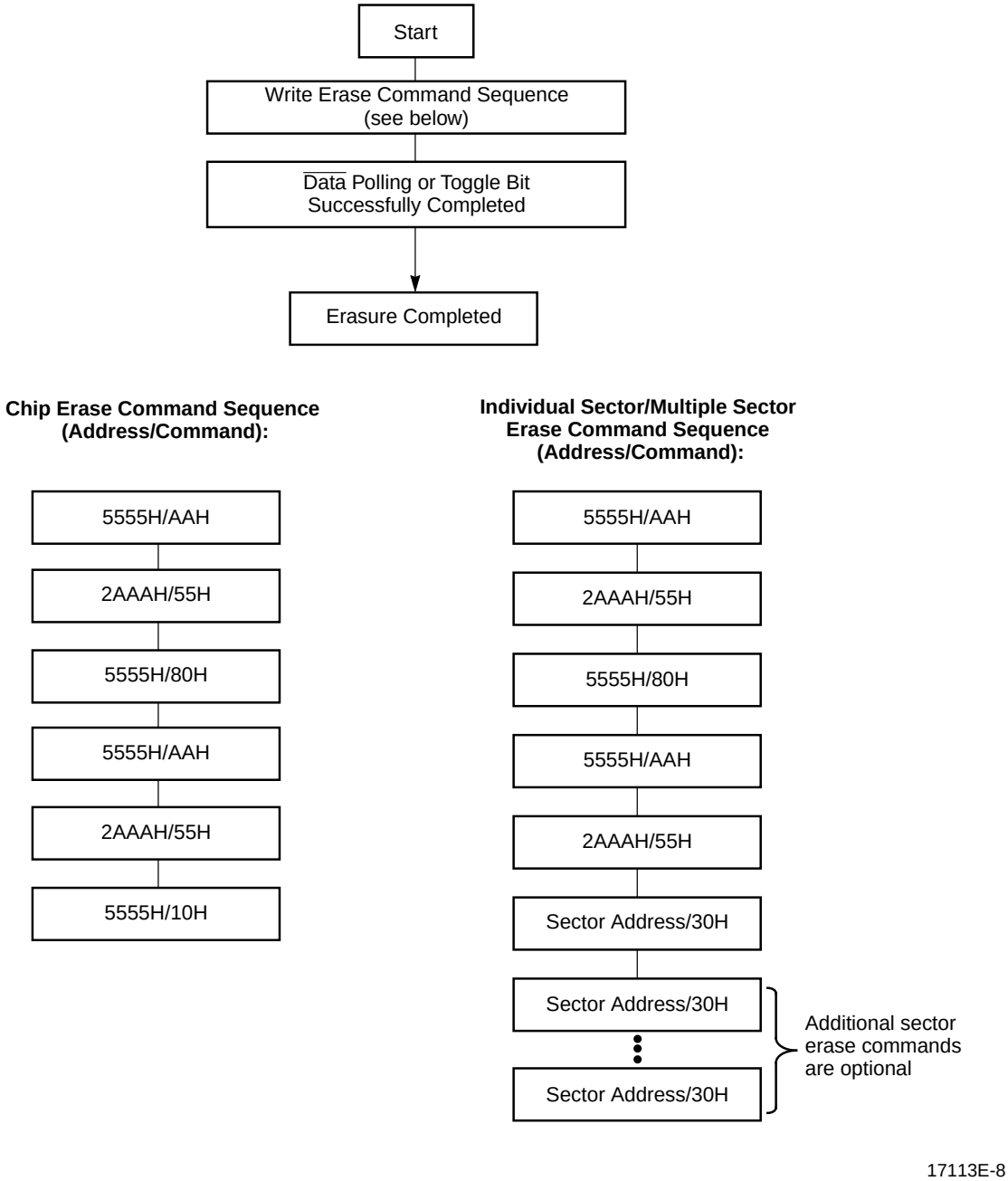
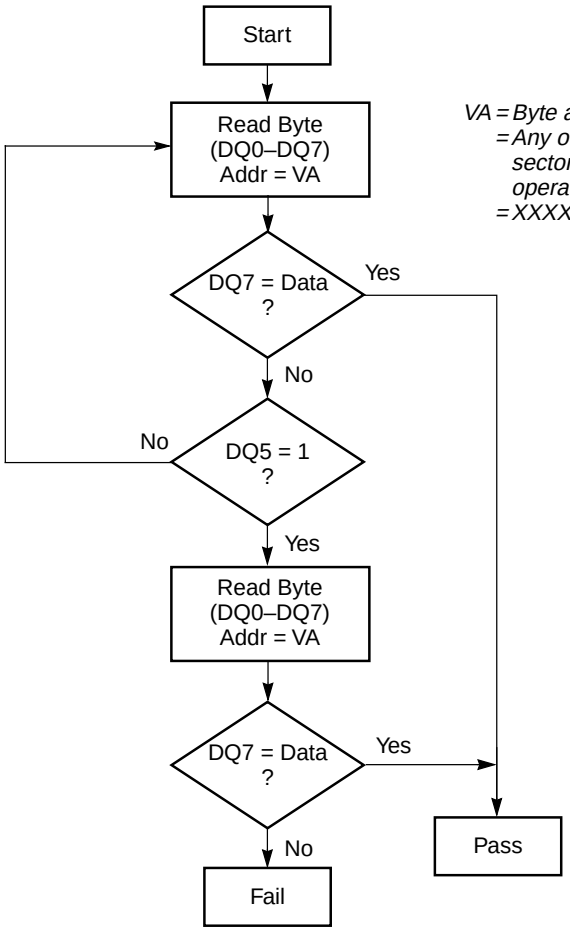
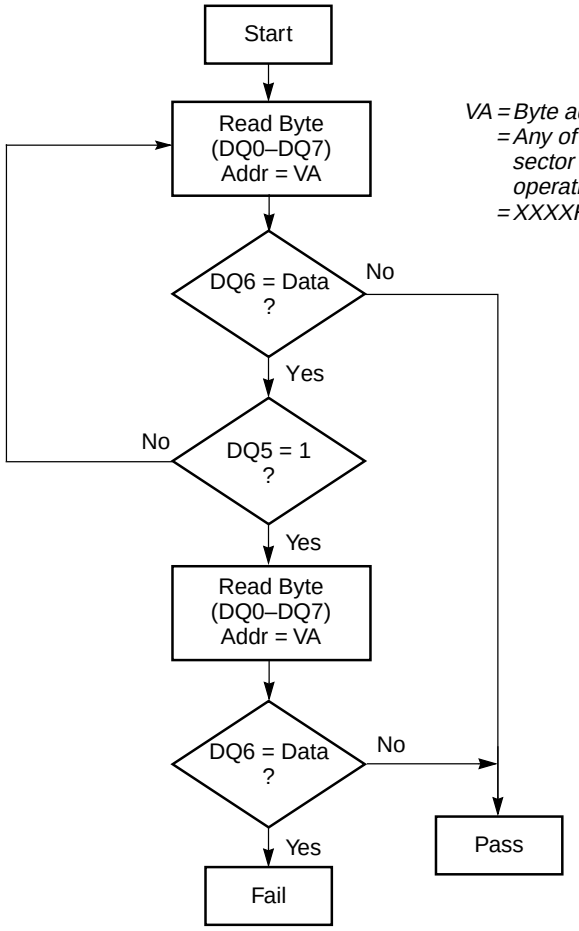


Figure 2. Embedded Erase Algorithm



Note:
DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 3. $\overline{\text{Data}}$ Polling Algorithm



Note:
DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 5. Toggle Bit Algorithm

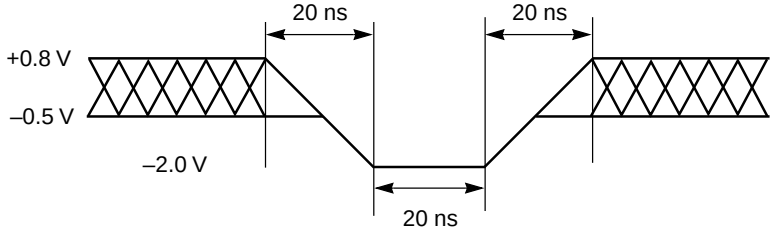


Figure 6. Maximum Negative Overshoot Waveform

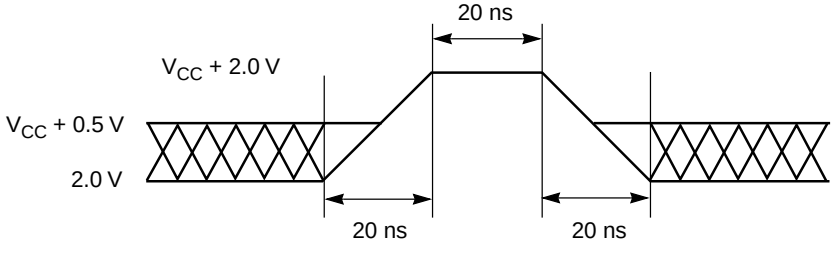


Figure 7. Maximum Positive Overshoot Waveform

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . . –65°C to +150°C
Plastic Packages . . . . . –65°C to +125°C

Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Voltage with Respect to Ground
All pins except A9 (Note 1). . . . . –2.0 V to +7.0 V

V_{CC} (Note 1). . . . . –2.0 V to +7.0 V

A9 (Note 2). . . . . –2.0 V to +13.0 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20ns.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for Am29F040-55. . . . . +4.75 V to +5.25 V

V_{CC} for Am29F040
-70, -90, -120, -150 . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC2}	V_{CC} Active Program/Erase Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		40	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$		1.0	mA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.25 V	10.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Level	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	2.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS (continued)

CMOS Compatible

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		20	30	mA
I_{CC2}	V_{CC} Active Program/Erase Current (Notes 2, 3)	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH		30	40	mA
I_{CC3}	V_{CC} Standby Current (Note 4)	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.5$ V		1	5	µA
V_{IL}	Input Low Level		–0.5		0.8	V
V_{IH}	Input High Level		0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.25 V	10.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12.0 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*
4. *I_{CC3} = 20 µA max at extended temperatures (> +85°C).*

AC CHARACTERISTICS

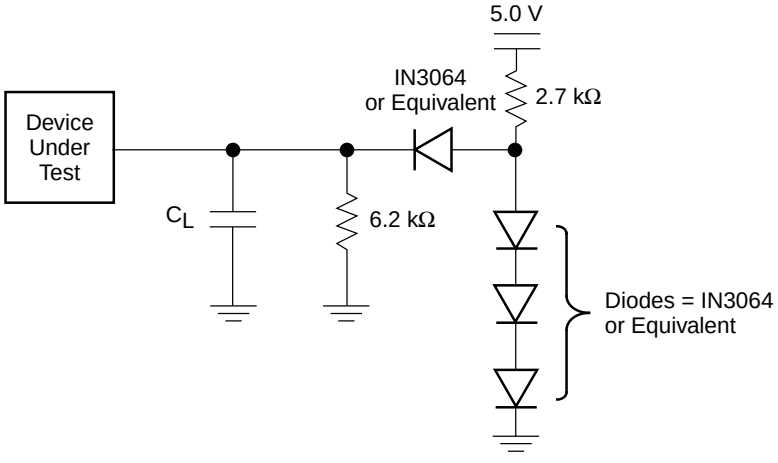
Read Only Operations Characteristics

Parameter Symbols		Description	Test Setup		Speed Options (Note 1)					Unit
JEDEC	Standard				-55	-70	-90	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 3)		Min	55	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	55	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	55	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	30	35	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 2, 3)		Max	18	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 2, 3)			18	20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0	0	0	0	0	ns

Notes:

1. *Test Conditions (for -55): Output Load: 1 TTL gate and 30 pF*
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level, input and output: 1.5 V and 1.5 V

   (for all others): Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level, input and output: 0.8 V and 2.0 V
2. *Output driver disable time.*
3. *Not 100% tested.*



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Notes:

For –55: C_L = 30 pF including jig capacitance

For all others: C_L = 100 pF including jig capacitance

Figure 8. Test Conditions

AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols		Description			Speed Options					Unit
JEDEC	Standard				-55	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	55	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	40	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	25	30	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min	0	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30	35	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	7	7	7	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ	1	1	1	1	1	sec
				Max	8	8	8	8	8	sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation (Note 1)		Typ	8	8	8	8	8	sec
				Max	64	64	64	64	64	sec
	t_{VCS}	V_{CC} Setup Time (Note 2)		Min	50	50	50	50	50	µs

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING WAVEFORMS

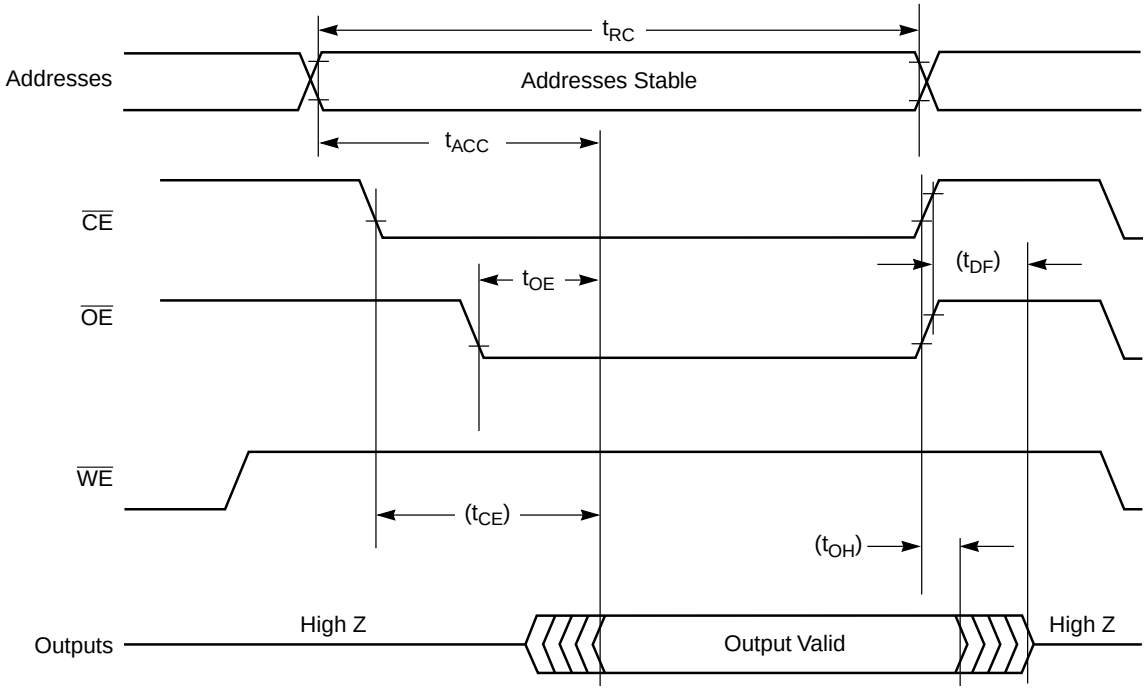

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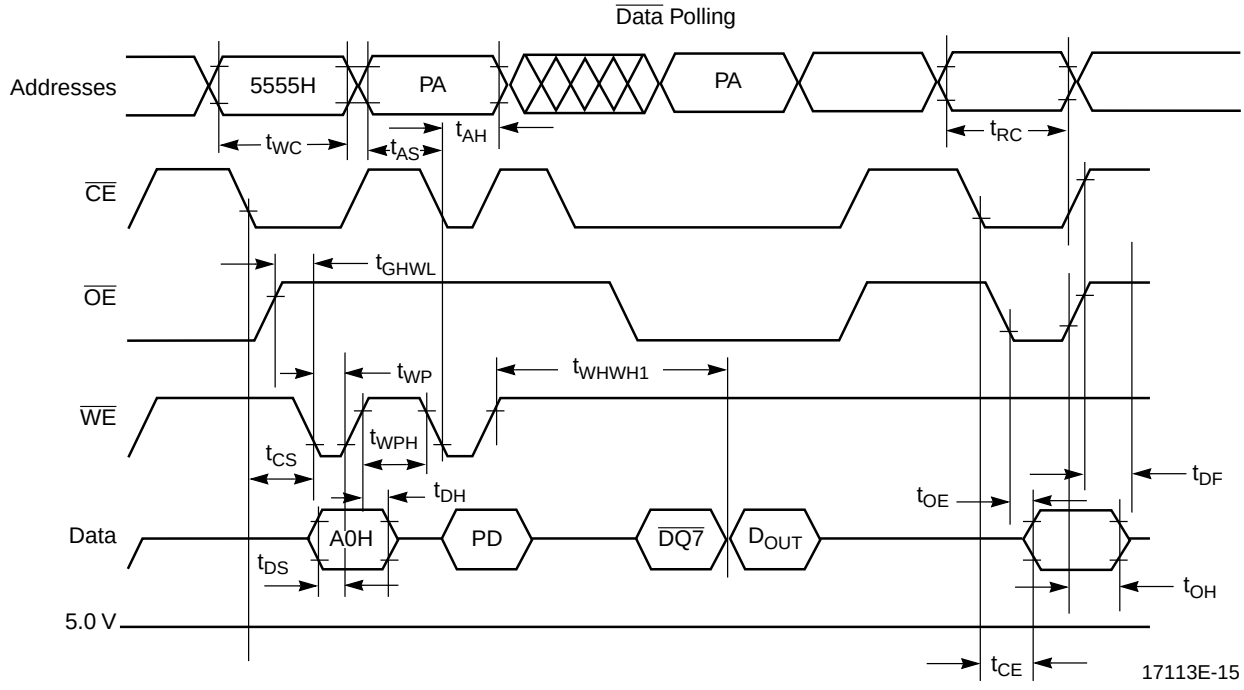
Figure 9. AC Waveforms for Read Operations

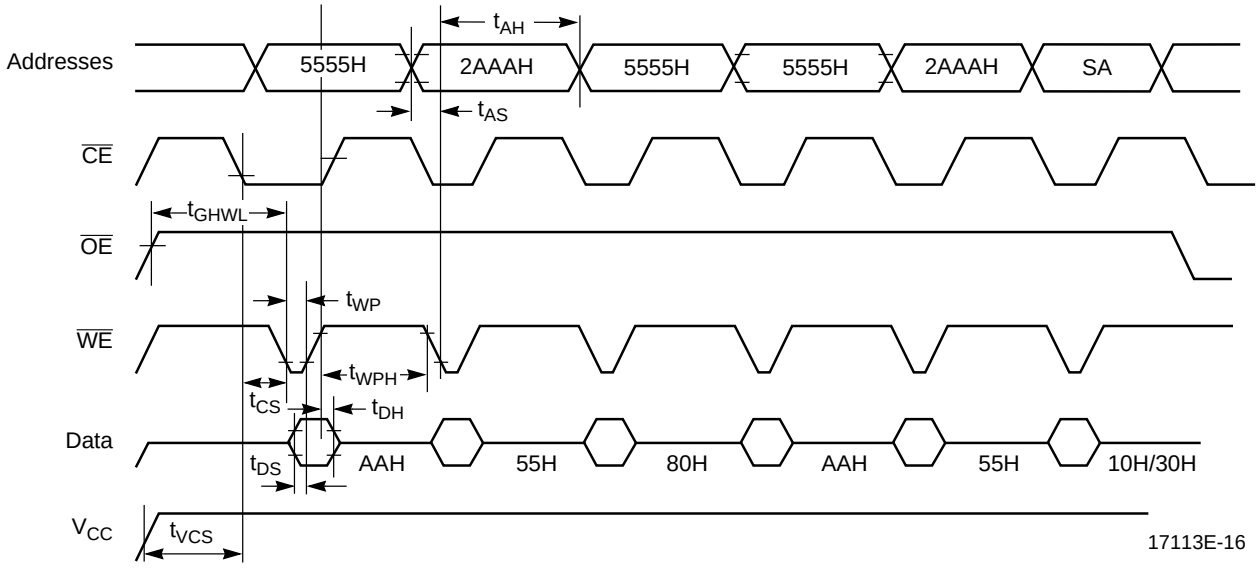
SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *D_{OUT} is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 10. Program Operation Timings

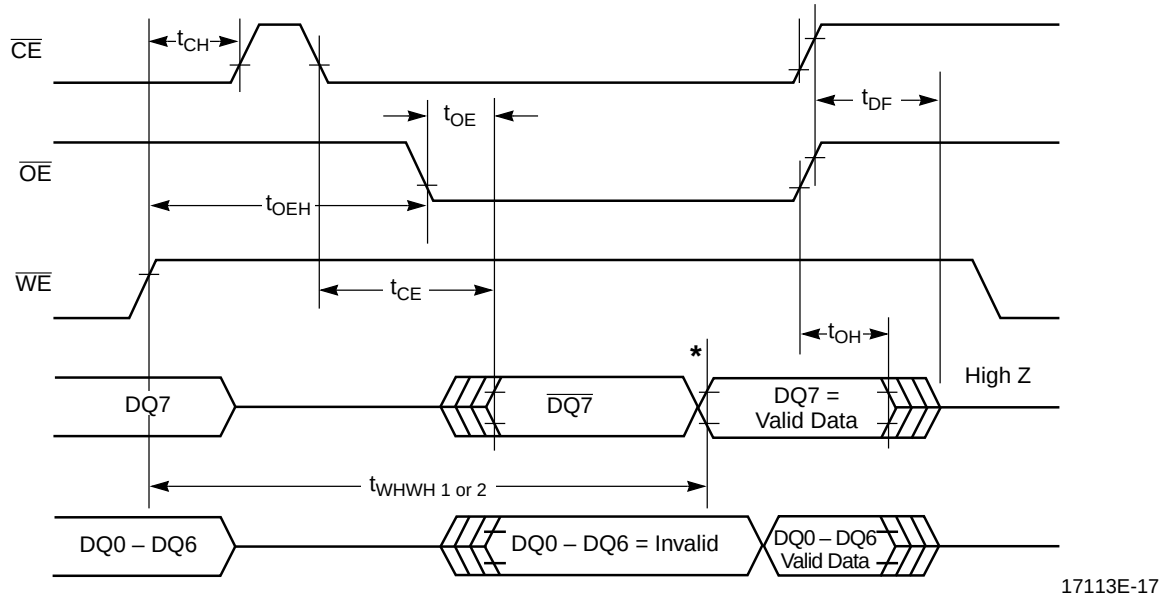


Note:

SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.

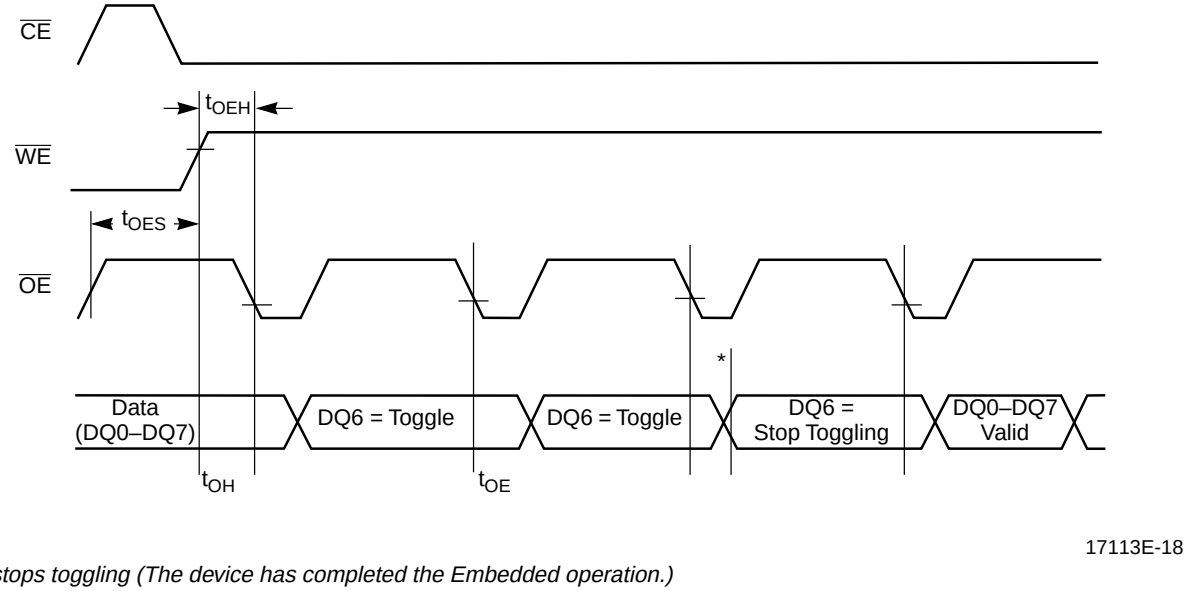
Figure 11. AC Waveforms Chip/Sector Erase Operations

SWITCHING WAVEFORMS



**DQ7 = Valid Data (The device has completed the Embedded operation.)*

Figure 12. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations



**DQ6 stops toggling (The device has completed the Embedded operation.)*

Figure 13. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

AC CHARACTERISTICS

Write/Erase/Program Operations

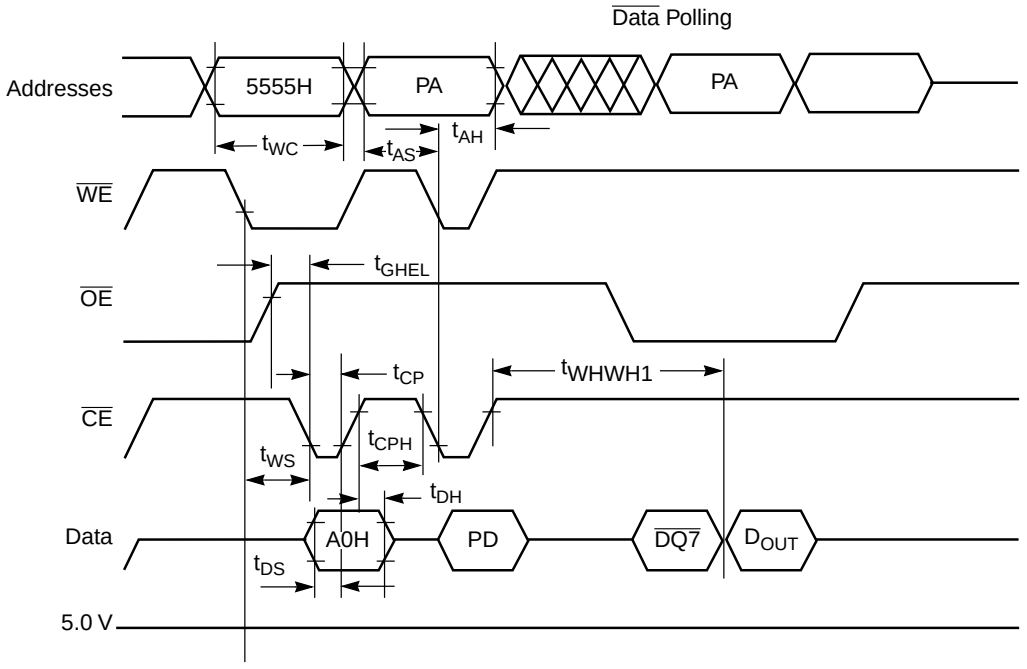
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols		Description			Speed Options					Unit
JEDEC	Standard				-55	-70	-90	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	55	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	40	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	25	30	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min	30	35	45	50	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	7	7	7	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ	1	1	1	1	1	sec
				Max	8	8	8	8	8	sec
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation (Note 1)		Typ	8	8	8	8	8	sec
				Max	64	64	64	64	64	sec
	t_{VCS}	V_{CC} Setup Time (Note 2)		Min	30	50	50	50	50	µs

Notes:

1. *This does not include the preprogramming time.*
2. *Not 100% tested.*

SWITCHING WAVEFORMS



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Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *D_{OUT} is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 14. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ	Max	Unit	Comments
Sector Erase Time	1.0 (Note 1)	8	sec	Excludes 00H programming prior to erasure
Chip Erase Time	8 (Note 1)	64	sec	Excludes 00H programming prior to erasure
Byte Programming Time	7 (Note 1)	300 (Note 2)	µs	Excludes system-level overhead (Note 3)
Chip Programming Time	3.6 (Note 1)	10.8 (Notes 2, 4)	sec	Excludes system-level overhead (Note 3)

Notes:

1. *25°C, 5 V V_{CC}, 100,000 cycles.*
2. *Under worst case condition of 90°C, 4.5 V V_{CC}, 100,000 cycles.*
3. *System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each byte. In the preprogramming step of the Embedded Erase algorithm, all bytes are programmed to 00H before erasure.*
4. *The Embedded Algorithms allow for 1.8 ms byte program time. DQ5 = "1" only after a byte takes the theoretical maximum time to program. A minimal number of bytes may require significantly more programming pulses than the typical byte. The majority of the bytes will program within one or two pulses (7 to 14µs). This is demonstrated by the Typical and Maximum Programming Times listed above.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.

LCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

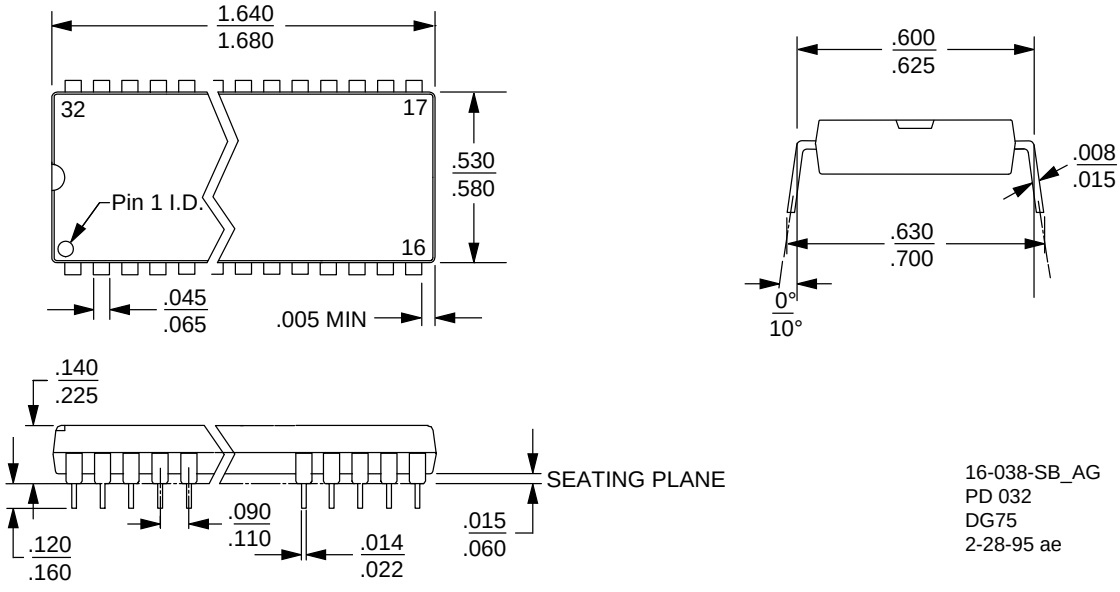
Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PHYSICAL DIMENSIONS

PD 032

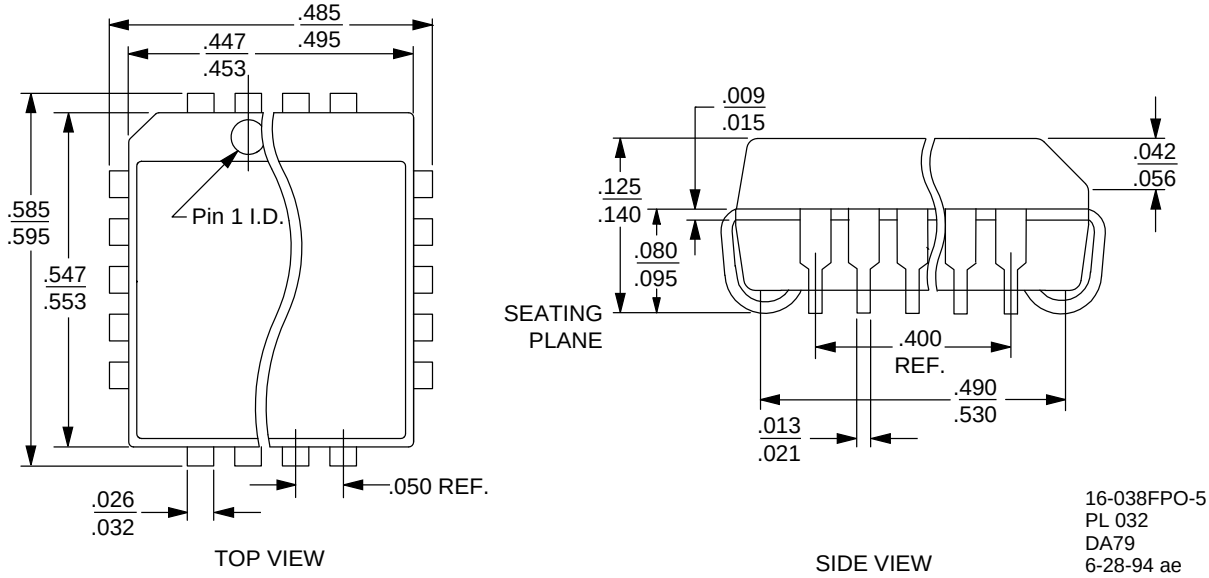
32-Pin Plastic DIP (measured in inches)



16-038-SB_AG
PD 032
DG75
2-28-95 ae

PL 032

32-Pin Plastic Leaded Chip Carrier (measured in inches)

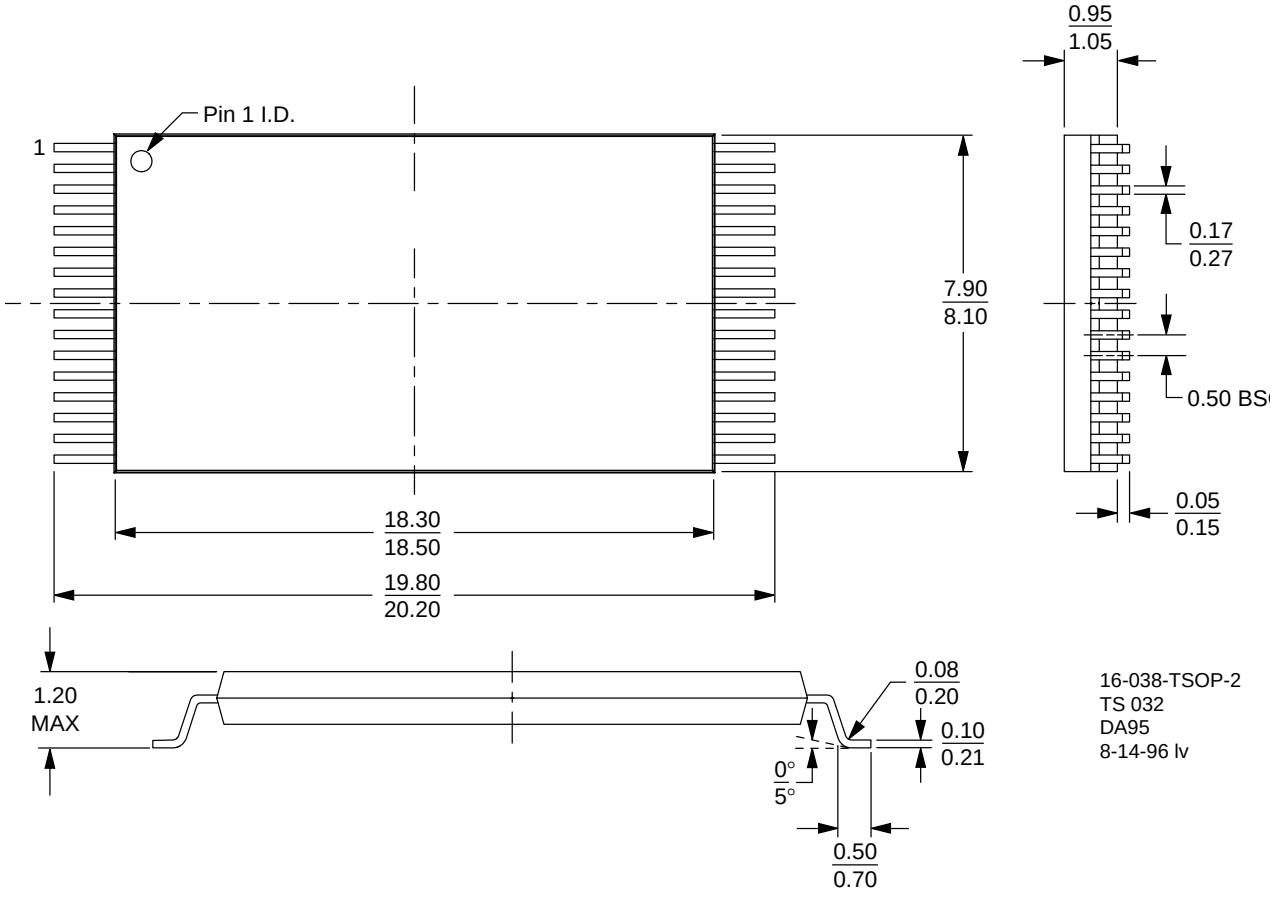


16-038FPO-5
PL 032
DA79
6-28-94 ae

PHYSICAL DIMENSIONS (continued)

TS 032

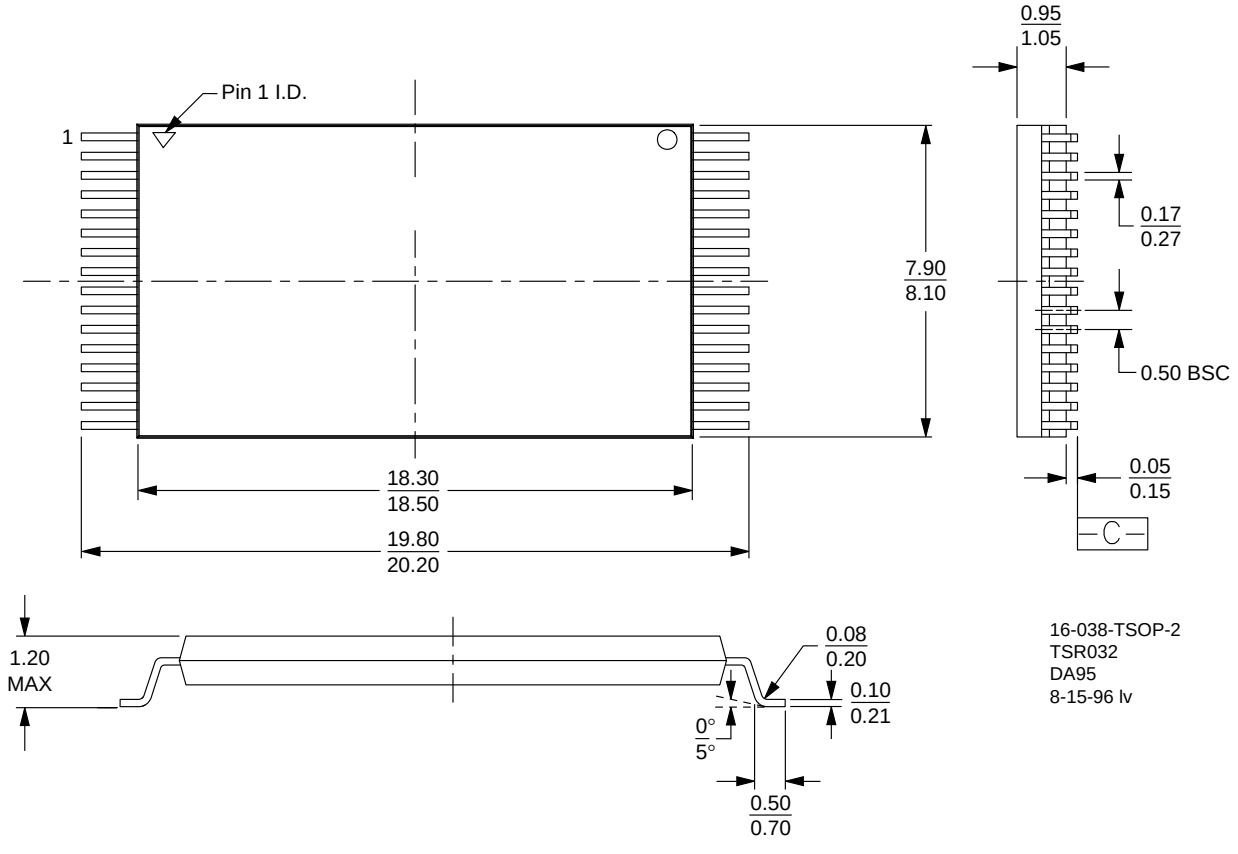
32-Pin Standard Thin Small Outline Package (measured in millimeters)



PHYSICAL DIMENSIONS (continued)

TSR032

32-Pin Reversed Thin Small Outline Package (measured in millimeters)



DATA SHEET REVISION SUMMARY FOR AM29F040

Distinctive Characteristics

Changed low power consumption specifications to typical values.

Added “enhanced power management” bullet.

General Description

Fifth paragraph, changed sector erase time to 1.0 sec.

Product Selector Guide

Removed the -75 (70 ns, ±5%) speed option.

Ordering Information

Added -55 speed option to the example part number. Removed the -75 speed option from the valid combinations. Added industrial and extended temperature ranges to -55 valid combinations. Added extended temperature to -70 valid combinations.

Table 1—User Bus Operations

Changed I/O write entry to “PD” and I/O read entry to “RD”; now matches Table 4. Corrected reference to tables in Note 2.

Standby Mode

Changed maximum CMOS standby mode current to 5 µA.

Autoselect

Deleted fourth paragraph.

Table 2—Autoselect Codes

Changed table title.

Table 3—Sector Addresses

Changed table title.

Sector Protection

Reworded second paragraph, second sentence.

Sector Unprotection

Deleted after second sentence.

Table 4—Command Definitions

Added “X” to first cycle of first Read/Reset command. Changed fourth cycle in Byte Program row from “data” to “PD”. Deleted Note 1. Rewrote Notes 2 and 6.

Sector Erase

Changed time-out to 80 µs. Deleted note. In second paragraph, deleted third sentence from end. In fourth paragraph, changed third sentence from end.

User Note for Chip Erase and Sector Erase Commands

Deleted section.

Erase Suspend

Deleted last sentence of fourth paragraph. Deleted fifth paragraph.

Table 5—Write Operation Status

Added overbars to DQ7.

DQ7—Data Polling

Fourth paragraph, added “Erase Suspend.”

DQ5—Exceeded Timing Limits

Clarified first sentence in fifth paragraph.

Absolute Maximum Ratings

Corrected V_{SS} in second sentence to V.

Operating Ranges—V_{CC} Supply Voltages

Added -55 and -70 speed options. Deleted -75 speed option.

DC Characteristics

TTL/NMOS Compatible: Changed I_{CC1}, I_{CC2}, and V_{ID} specifications.

CMOS Compatible: Changed I_{CC1}, I_{CC2}, I_{CC3} and V_{ID} specifications, added typical values. Added Note 4.

AC Characteristics

Read Only Operations Characteristics: Removed -75 speed option. Changed t_{GLQV} in -55 column to 30 ns. Combined Notes 1 and 2.

Figure 7—Test Conditions

Changed first C_L in note to -55.

AC Characteristics

Write/Erase/Program Operations (also same table for Alternate $\overline{CE}$ Controlled Writes): Removed -75 speed option. Changed specifications on t_{WHWH1}, t_{WHWH2}, and t_{WHWH3}.

Erase and Programming Performance

Changed maximum specifications. Clarified note 5. Deleted Note 2.