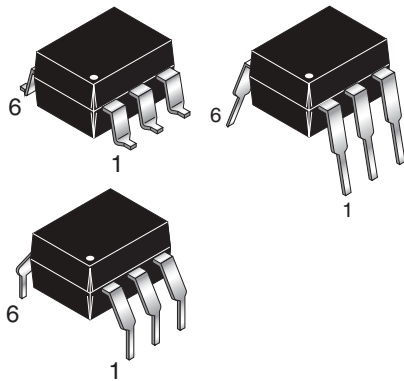


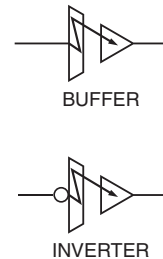
LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

PACKAGE



SYMBOL



DESCRIPTION

OPTOLOGIC™ is the first family of truly logic compatible optically coupled logic interface gates.

The family consists of four device types offering LSTTL to TTL and LSTTL to CMOS interfacing. Each of these interfacing functions is available as a buffer ($A=B$), or as an inverter ($A=\bar{B}$).

The LSTTL input compatibility is provided by an input integrated circuit, with industry standard logic levels. This input amplifier IC switches a temperature compensated current source driving a high speed 850 nm AlGaAs LED emitter. This novel integration scheme eliminates CTR degradation over time and temperature.

The emitter is optically coupled to an integrated photodetector/high-gain, high-speed output amplifier IC. The superior 15kV/μS common-mode noise rejection is ensured through the use of an optically transparent noise shield.

The TTL compatible output has a totem-pole with a fan-out of 10. The CMOS compatible output has an open collector Schottky-clamped transistor that interfaces to any CMOS logic between 4.5 and 15 volts. The 74OL6010/11 may also be used to drive power MOSFETS or transistors up to 15 volts.

The Optologic coupler family typically offers propagation of delays of 60 ns and can support 15 MBaud data communication.

The two input chips and the output chip are assembled in a 6-pin DIP high insulation voltage plastic package. Fairchild's proprietary OPTOPLANAR® construction provides a withstand test voltage of 5300 VRMS (1 minute).

FEATURES

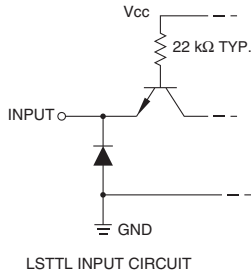
- Industry first LSTTL to TTL and LSTTL to CMOS complete logic-to-logic optocoupler
- Incorporates LED drive circuitry — use as logic gate
- Very high speed
- Choice of buffer or inverter
- Choice of TTL or CMOS compatible output up to 15 volts
- Fan-out of 10 TTL loads, fan-in 1 LSTTL load
- Internal noise shield — very high CMR of ±15 kV/μS
- UL recognized (File #E90700)
- Same noise immunity as LSTTL/TTL.

APPLICATIONS

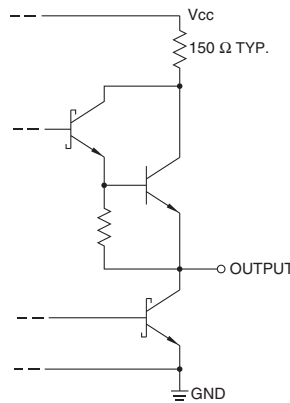
- Transmission line interface — receiver and driver
- Excellent as bridged receiver in fast LAN highways
- Bus interface
- Logic family interface with ground loop noise elimination
- High speed AC/DC voltage sensing
- Driver for power semiconductor devices
- Level shifting
- Replaces fast pulse transformers

LSTTL TO

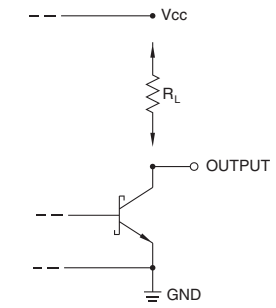
| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |



All Inputs



TTL OUTPUT CIRCUIT
74OL6000/01 Output



CMOS OUTPUT CIRCUIT

74OL6010/11 Output

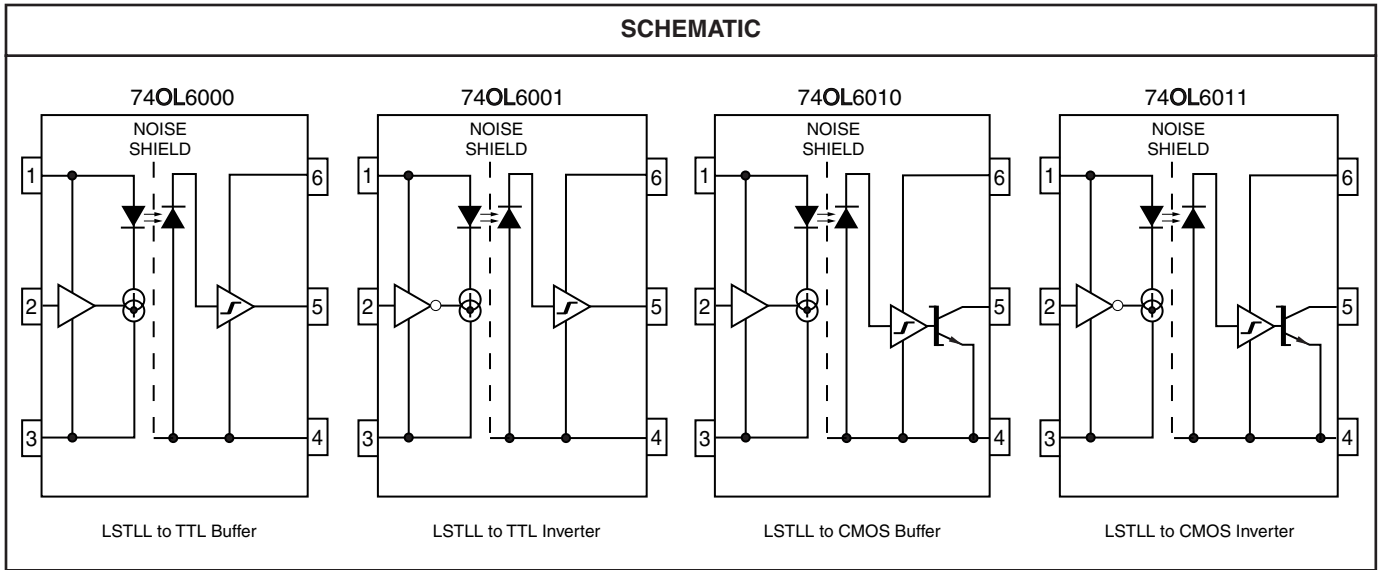
| PIN CONFIGURATION | |
|--------------------------------|---------------------------------|
| 1- V_{CCI} (Input V_{CC}) | 6- V_{CCO} (Output V_{CC}) |
| 2- V_{IN} (Data In) | 5- V_O (Data Out) |
| 3-GND, (Input GND) | 4-GND _O (Output GND) |

| DEVICE CONFIGURATION | | | | |
|----------------------|---------------------|--------|----------------|----------------------|
| Part Number | Logic Compatibility | | Logic Function | Output Configuration |
| | Input | Output | | |
| 74OL 6000 | LSTTL | TTL | BUFFER | TOTEM POLE |
| 74OL 6001 | LSTTL | TTL | INVERTER | TOTEM POLE |
| 74OL 6010 | LSTTL | CMOS | BUFFER | OPEN COLLECTOR |
| 74OL 6011 | LSTTL | CMOS | INVERTER | OPEN COLLECTOR |

LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

SCHEMATIC



LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C Unless otherwise specified)

| Parameter | Symbol | Min | Typ* | Max | Units | Test Conditions | | | Notes |
|-------------------------------|------------|------|--------|--|---------------|-------------------------|-------------------------|---|-------|
| | | | | | | 74OL6000 | 74OL6001 | 74OL6000/01 | |
| TTL OUTPUT 74OL6000/01 | | | | | | | | | |
| Input Supply Voltage | V_{CCI} | 4.5 | 5.0 | 5.5 | V | | | | 1 |
| Output Supply Voltage | V_{CCO} | 4.5 | 5.0 | 5.5 | V | | | | 1 |
| High-Level Input Voltage | V_{IH} | 2.0 | | | V | | | | 1 |
| Low-Level Input Voltage | V_{IL} | | | 0.8 | V | | | | 1 |
| Input Clamp Voltage | V_{IK} | | | -1.2 | V | | | $V_{CCI} = 4.5\text{ V}, I_I = -18\text{ mA}$ | 1 |
| High-Level Input Current | I_{IH} | | 1.0 | 40.0 | μA | | | $V_{CCI} = 5.5\text{ V}, V_{IH} = 4.5\text{ V}$ | 1 |
| Low-Level Input Current | I_{IL} | | -200.0 | -400.0 | μA | | | $V_{CCI} = 5.5\text{ V}, V_{IL} = 0.4\text{ V}$ | 1 |
| Input Supply Current (high) | I_{CCIH} | | 10.0 | 14.0 | mA | | | $V_{CCI} = 5.5\text{ V}, V_{IN} = V_{IH}$ | 1 |
| Input Supply Current (low) | I_{CCIL} | | 10.0 | 14.0 | mA | | | $V_{CCI} = 5.5\text{ V}, V_{IN} = V_{IL}$ | 1 |
| High-Level Output Voltage | V_{OH} | 2.4 | 3.0 | | V | $V_{IN} = 2.0\text{ V}$ | $V_{IN} = 0.8\text{ V}$ | $V_{CCI} = 4.5\text{ V}, V_{CCO} = 4.5\text{ V}, I_{OH} = -400\text{ mA}$ | 1 |
| Low-Level Output Voltage | V_{OL} | | 0.6 | | V | $V_{IN} = 0.8\text{ V}$ | $V_{IN} = 2.0\text{ V}$ | $V_{CCI} = 4.5\text{ V}, V_{CCO} = 4.5\text{ V}, I_{OL} = 16\text{ mA}$ | 1 |
| | | | 0.5 | $V_{CCI} = 4.5\text{ V}, V_{CCO} = 4.5\text{ V}, I_{OL} = 4\text{ mA}$ | | | | | |
| High-Level Output Current | I_{OH} | | -8.0 | -10.0 | mA | $V_{IN} = V_{IH}$ | $V_{IN} = V_{IL}$ | $V_{CCI} = 4.5\text{ V}, V_{CCO} = 4.5\text{ V}, V_{OH} = 2.4\text{ V}$ | 1 |
| Low-Level Output Current | I_{OL} | 16.0 | | | mA | $V_{IN} = 0.8\text{ V}$ | $V_{IN} = 2.0\text{ V}$ | $V_{CCI} = 4.5\text{ V}, V_{CCO} = 4.5\text{ V}, V_{OL} = 0.6\text{ V}$ | 1 |
| Short-Circuit Output Current | I_{OS} | -5.0 | -25.0 | -40.0 | mA | $V_{IN} = V_{IH}$ | $V_{IN} = V_{IL}$ | $V_{CCI} = 5.5\text{ V}, V_{CCO} = 5.5\text{ V}$ | 1 |
| Output Supply Current (high) | I_{CCOH} | | 9.0 | 15.0 | mA | $V_{IN} = V_{IH}$ | $V_{IN} = V_{IL}$ | $V_{CCI} = 5.5\text{ V}, V_O = V_{OH}, V_{CCO} = 5.5\text{ V}$ | 1 |
| Output Supply Current (low) | I_{CCOL} | | 8.0 | 12.0 | mA | $V_{IN} = V_{IL}$ | $V_{IN} = V_{IH}$ | $V_{CCI} = 5.5\text{ V}, V_O = V_{OL}, V_{CCO} = 5.5\text{ V}$ | 1 |

*All typical values are at $T_A = 25^\circ\text{C}$

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise specified)

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions | Fig. | Notes |
|--|-----------|-----|-----|-----|-------|--|--------|-------|
| TTL OUTPUT 74OL6000/01 | | | | | | | | |
| Propagation Delay Time For Output Low Level | t_{PHL} | | 60 | 100 | ns | $V_{CCI} = 5\text{ V}, V_{CCO} = 5\text{ V}$ | 15, 17 | 1 |
| Propagation Delay Time For Output High Level | t_{PLH} | | 70 | 100 | ns | | 15, 17 | 1 |
| Output Rise Time For Output High Level | t_r | | 45 | | n | | 15, 17 | 1 |
| Output Fall Time For Output Low Level | t_f | | 5 | | ns | | 15, 17 | 1 |

LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C Unless otherwise specified)

| Parameter | Symbol | Min | Typ* | Max | Units | Test Conditions | | | Notes |
|--------------------------------|------------|------|--------|--------|---------------|-------------------------|-------------------------|--|-------|
| | | | | | | 74OL6010 | 74OL6011 | 74OL6010/11 | |
| CMOS OUTPUT 74OL6010/11 | | | | | | | | | |
| Input Supply Voltage | V_{CCI} | 4.5 | 5.0 | 5.5 | V | | | | 1 |
| Output Supply Voltage | V_{CCO} | 4.5 | | 15.0 | V | | | | 1,3 |
| High-Level Input Voltage | V_{IH} | 2.0 | | | V | | | | 1 |
| Low-Level Input Voltage | V_{IL} | | | 0.8 | V | | | | 1 |
| Input Clamp Voltage | V_{IK} | | | -1.2 | V | | | $V_{CCI} = 4.5\text{ V}, I_I = -18\text{ mA}$ | 1 |
| High-Level Input Current | I_{IH} | | 1.0 | 40.0 | μA | | | $V_{CCI} = 5.5\text{ V}, V_{IH} = 4.5\text{ V}$ | 1 |
| Low-Level Input Current | I_{IL} | | -200.0 | -400.0 | μA | | | $V_{CCI} = 5.5\text{ V}, V_{IL} = -0.4\text{ V}$ | 1 |
| Input Supply Current (high) | I_{CCIH} | | 10.0 | 14.0 | mA | | | $V_{CCI} = 5.5\text{ V}, V_{IN} = V_{IH}$ | 1 |
| Input Supply Current (low) | I_{CCIL} | | 10.0 | 14.0 | mA | | | $V_{CCI} = 5.5\text{ V}, V_{IN} = V_{IL}$ | 1 |
| Low-Level Output Voltage | V_{OL} | 0.4 | 0.6 | 100.0 | V | $V_{IN} = 0.8\text{ V}$ | $V_{IN} = 2.0\text{ V}$ | $V_{CCI} = 4.5\text{ V}, V_{CCO} = 4.5\text{ V}, I_{OL} = 16\text{ mA}$ | 1 |
| | | | 0.5 | | | | | $V_{CCI} = 4.5\text{ V}, V_{CCO} = 4.5\text{ V}, I_{OL} = 4\text{ mA}$ | |
| High-Level Output Current | I_{OH} | | 1.0 | | μA | $V_{IN} = V_{IH}$ | $V_{IN} = V_{IL}$ | $V_{CCI} = 4.5\text{ V}, V_{OH} = 15\text{ V}, V_{CCO} = 4.5 - 15\text{ V}$ | 1 |
| Low-Level Output Current | I_{OL} | 16.0 | | | mA | $V_{IN} = 0.8\text{ V}$ | $V_{IN} = 2.0\text{ V}$ | $V_{CCI} = 4.5\text{ V}, V_{OL} = 0.6\text{ V}, V_{CCO} = 4.5 - 15\text{ V}$ | 1 |
| Output Supply Current (high) | I_{CCOH} | | 9.0 | 12.0 | mA | $V_{IN} = V_{IH}$ | $V_{IN} = V_{IL}$ | $V_{CCI} = 5.5\text{ V}, V_O = V_{OH}, V_{CCO} = 4.5\text{ V}$ | 1 |
| | | | 11.0 | 18.0 | | | | $V_{CCI} = 5.5\text{ V}, V_O = V_{OL}, V_{CCO} = 15\text{ V}$ | |
| Output Supply Current (low) | I_{CCOL} | | 8.0 | 12.0 | mA | $V_{IN} = V_{IL}$ | $V_{IN} = V_{IH}$ | $V_{CCI} = 5.5\text{ V}, V_O = V_{OL}, V_{CCO} = 4.5\text{ V}$ | 1 |
| | | | 11.0 | 18.0 | | | | $V_{CCI} = 5.5\text{ V}, V_O = V_{OL}, V_{CCO} = 15\text{ V}$ | |

*All typical values are at $T_A = 25^\circ\text{C}$

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$ Unless otherwise specified)

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions | Fig. | Notes |
|--|-----------|-----|-----|-----|-------|---|--------|-------|
| TTL OUTPUT 74OL6010/11 | | | | | | | | |
| Propagation Delay Time For Output Low Level | t_{PHL} | | 60 | 120 | ns | $V_{CCI} = 5\text{ V}, V_{CCO} = 5\text{ V}, R_L = 470\ \Omega$ | 15, 18 | 1 |
| Propagation Delay Time For Output High Level | t_{PLH} | | 100 | 180 | ns | | 15, 18 | 1 |
| Output Rise Time For Output High Level | t_r | | 50 | | ns | | 15, 18 | 1 |
| Output Fall Time For Output Low Level | t_f | | 5 | | ns | | 15, 18 | 1 |

| | | |
|-----------------|---------------|----------|
| LSTTL TO | TTL BUFFER | 74OL6000 |
| | TTL INVERTER | 74OL6001 |
| | CMOS BUFFER | 74OL6010 |
| | CMOS INVERTER | 74OL6011 |

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Device | Value | Units |
|-------------------------|-------------|-------------|----------------|------------------|
| TOTAL DEVICE | | | | |
| Storage Temperature | T_{STG} | All | -55 to +125 | $^\circ\text{C}$ |
| Operating Temperature | T_{OPR} | All | 0 to +70 | $^\circ\text{C}$ |
| Lead Solder Temperature | T_{SOL} | All | 260 for 10 sec | $^\circ\text{C}$ |
| Power Dissipation | P_D | All | 350 | mW |
| EMITTER | | | | |
| Input Supply Voltage | V_{CCI} | All | 7 | V |
| Input Voltage | V_{IN} | All | 7 | V |
| DETECTOR | | | | |
| Average Output Current | I_O (avg) | All | 40 | mA |
| Output Supply Voltage | V_{CCO} | 74OL6000/01 | 7 | V |
| | | 74OL6010/11 | 18 | |
| Output Voltage | V_O | 74OL6000/01 | 7 | V |
| | | 74OL6010/11 | 18 | |

ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C Unless otherwise specified)

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions | Fig. | Notes |
|---|-----------|-------|-----------|-----|------------------|---|--------|-------|
| 74OL6000/01/10/11 | | | | | | | | |
| Common Mode Transient Immunity at Logic High Level Output | CM_H | 5000 | 15000 | | V/ μS | $V_{CCI} = 5\text{ V}, V_{CCO} = 5\text{ V}, V_{CM} = 50\text{ Vp-p}$ | 16, 19 | |
| Common Mode Transient Immunity at Logic Low Level Output | CM_L | -5000 | -15000 | | V/ μS | | 16, 19 | |
| Common Mode Coupling Capacitance | C_{CM} | | 0.005 | | pF | | | |
| Capacitance (input-output) | C_{I-O} | | 0.7 | | pF | $V_{I-O} = 0, f = 1\text{ MHz}$ | | 2 |
| Withstand Insulation Test Voltage | V_{ISO} | 5300 | | | VRMS | $T_A = 25^\circ\text{C}, t = 1\text{ min}, I_{I-O} \leq 1\text{ mA}$ | | 2 |
| Insulation Resistance | R_{ISO} | | 10^{11} | | Ω | $V_{I-O} = 500\text{ VDC}$ | | 2 |

LSTTL TO

| | |
|----------------------|-----------------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

Figure 1. Input Current vs. Ambient Temperature

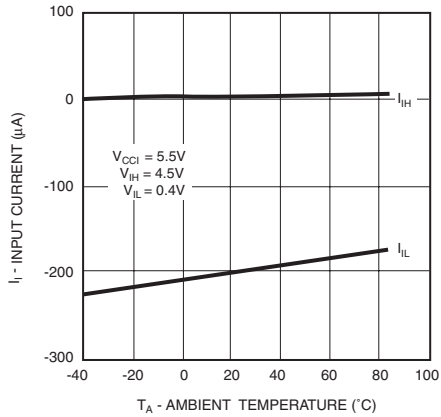


Figure 2. Input Supply Current vs. Ambient Temperature

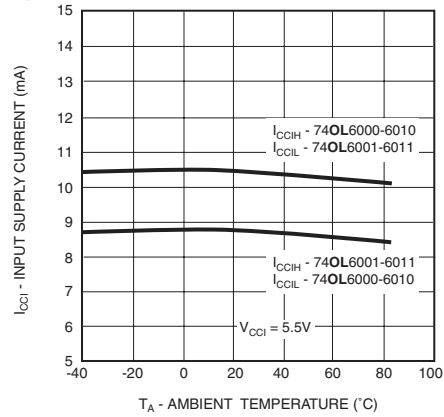


Figure 3. Output Supply Current vs. Ambient Temperature

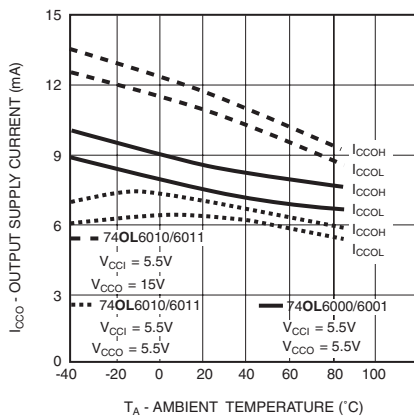


Figure 4. Output Current vs. Ambient Temperature

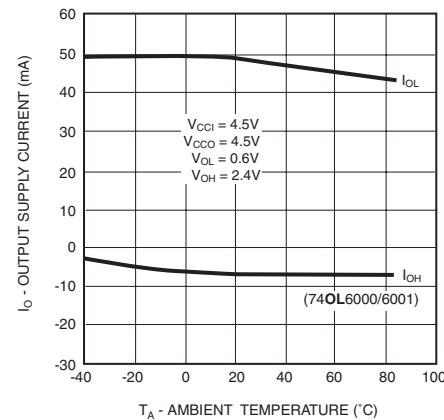


Figure 5. High-Level Output Voltage vs. Ambient Temperature

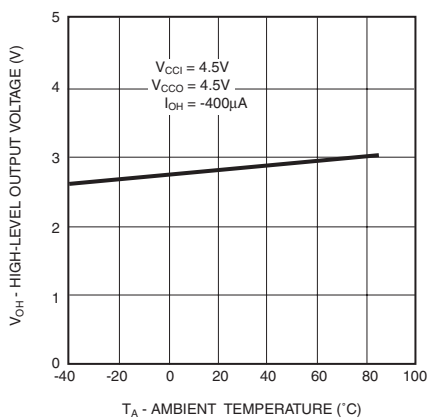
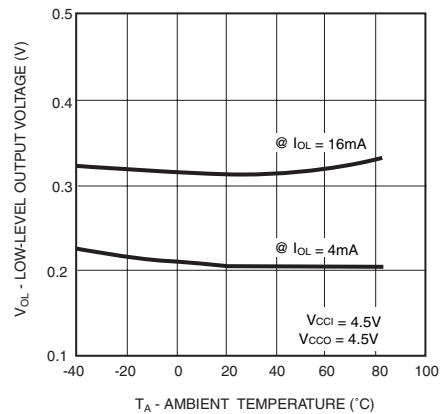


Figure 6. Low-Level Output Voltage vs. Ambient Temperature



LSTTL TO

| | |
|----------------------|-----------------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

Figure 7. 74OL6010/11 Leakage Current vs. Ambient Temperature

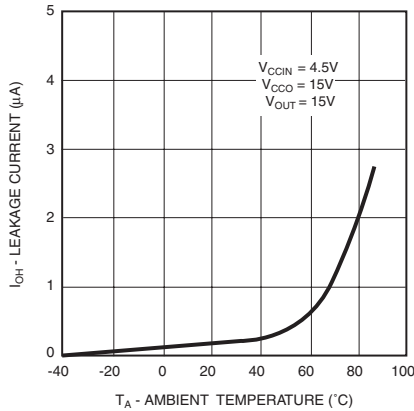


Figure 8. 74OL6000/01 Switching Times vs. Ambient Temperature

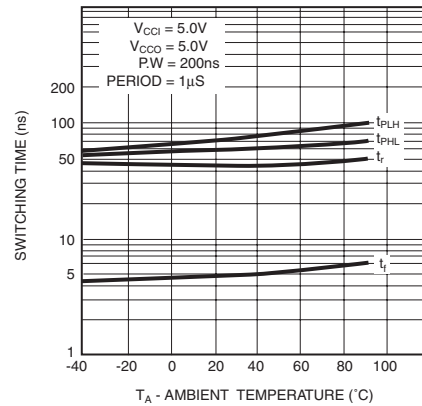


Figure 9. 74OL6010/11 Switching Times vs. Ambient Temperature

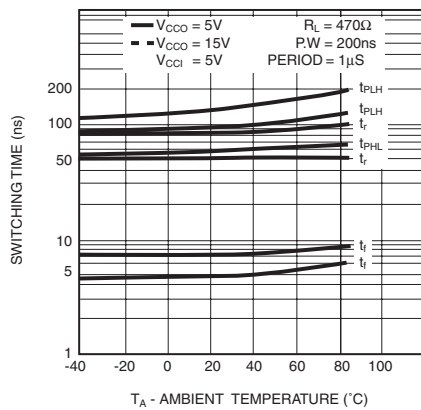


Figure 10. Common Mode Rejection vs. Common Mode Voltage

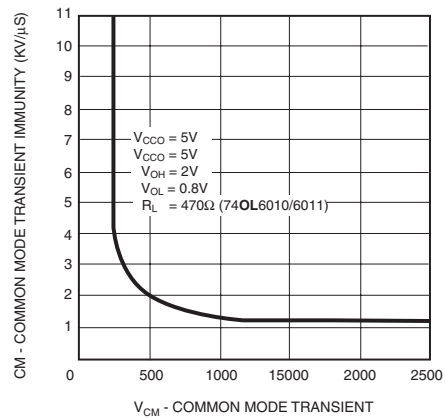


Figure 11. Supply Current vs. Supply Voltage

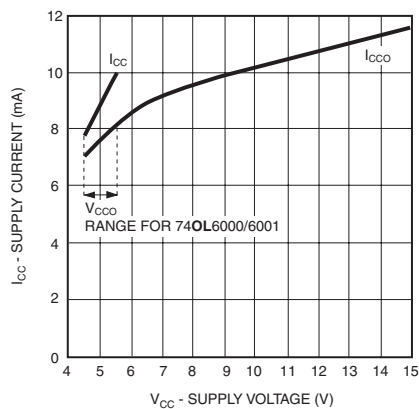
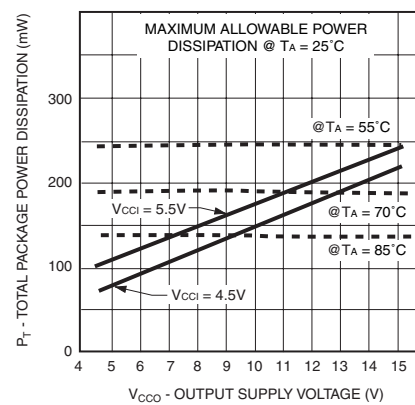


Figure 12. Power Dissipation vs. Ambient Temperature



LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

Figure 13. Input Threshold Voltage vs. Ambient Temperature

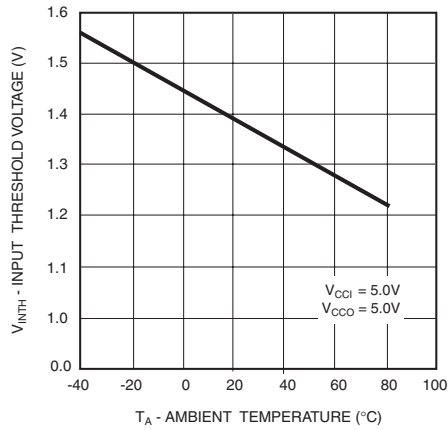


Figure 14. Input Current vs. Input Voltage

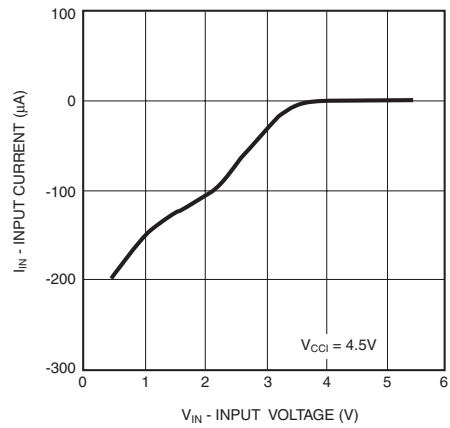


Figure 15. Switching Time Test Circuit

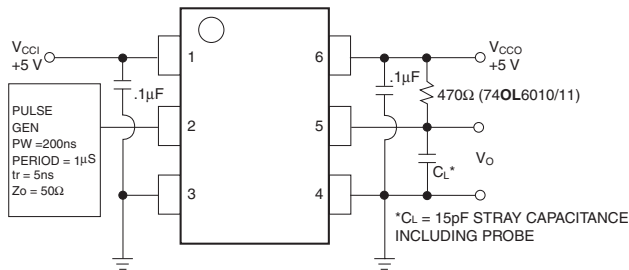
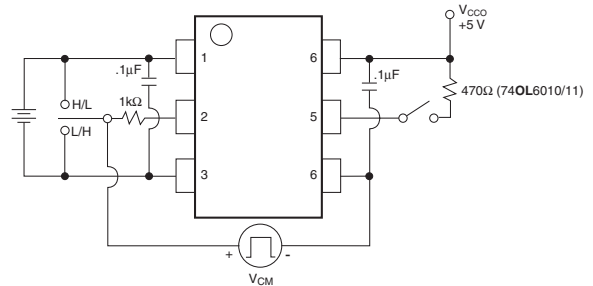


Figure 16. Common Mode Rejection Test Circuit



LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

Figure 17. 74OL6000/01 Switching Times vs. Ambient Temperature

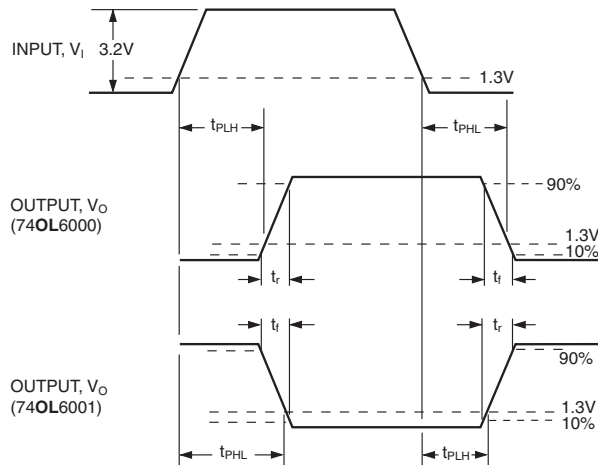


Figure 18. Switching Parameters 74OL6010/11

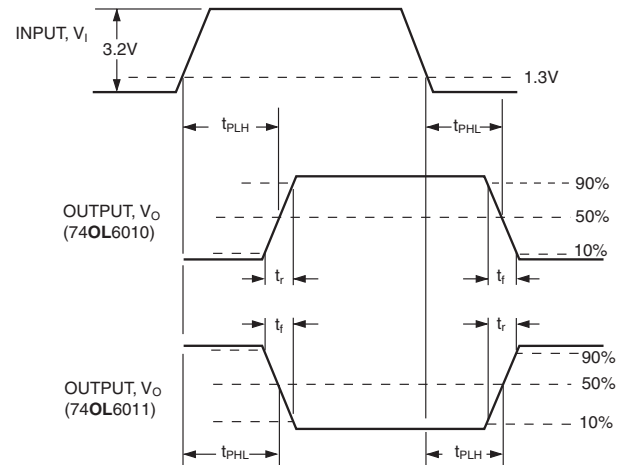


Figure 19. Common Mode Rejection Waveforms

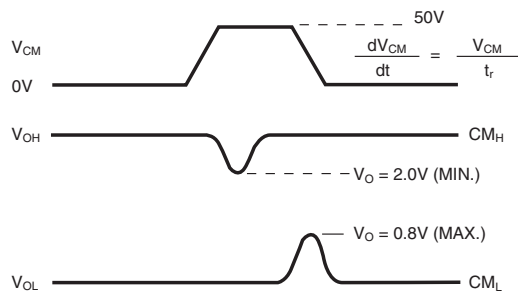
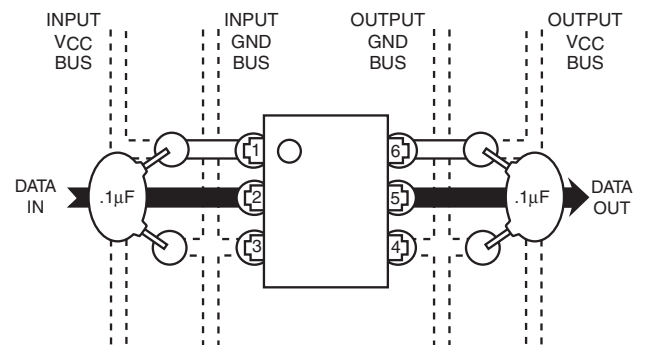


Figure 20. Suggested PCB Lay-Out



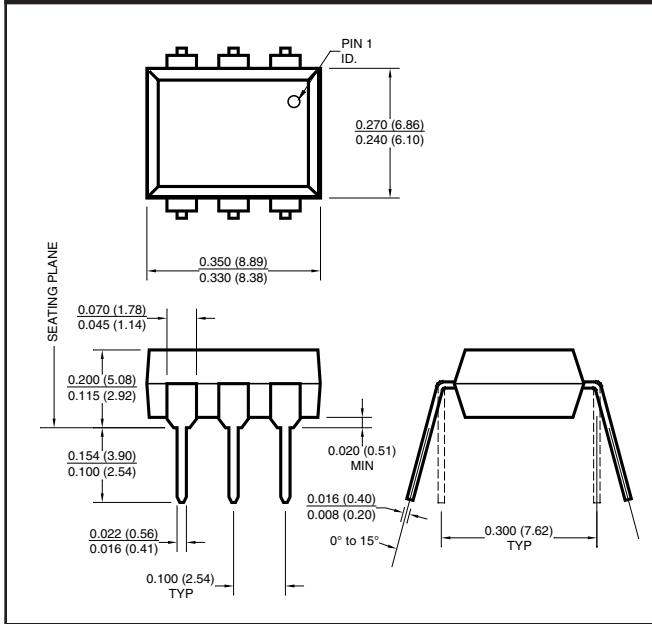
NOTE

1. The VCCO and VCCI supply voltages to the device must each be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristics. Its purpose is to stabilize the operation of the high-gain amplifiers. Failure to provide the bypass will impair the DC and switching properties. The total lead length between capacitor and optocoupler should not exceed 1.5mm. See Fig. 20.
2. Device considered a two-terminal device. Pins 1, 2 and 3 shorted together, and Pins 4, 5 and 6 shorted together.
3. For example, assuming a V_{CCI} of 5.0V, and an ambient temperature of 70°C, the maximum allowable V_{CCO} is 12.1V.

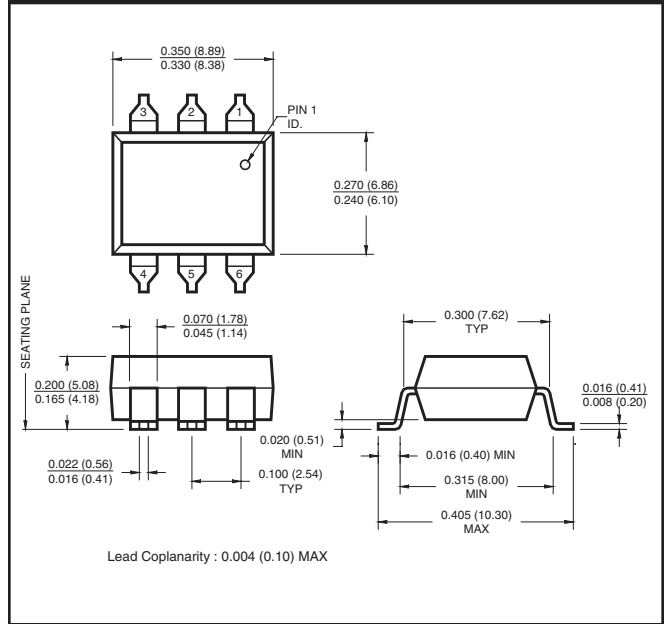
LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

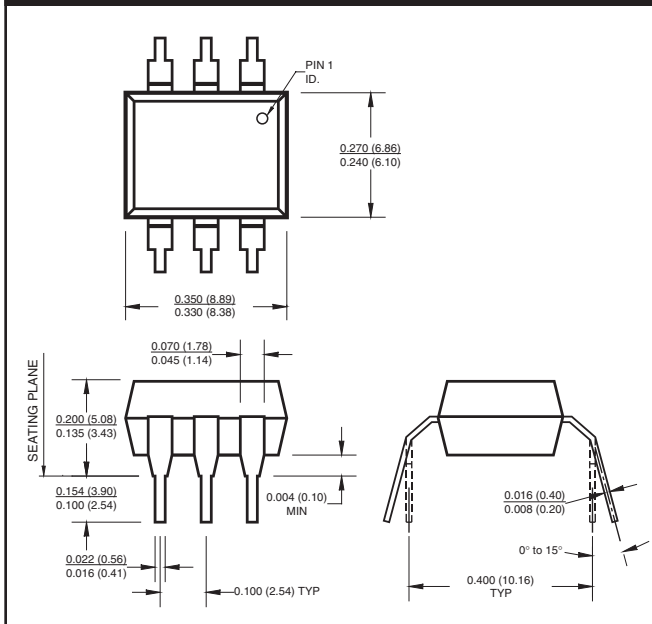
Package Dimensions (Through Hole)



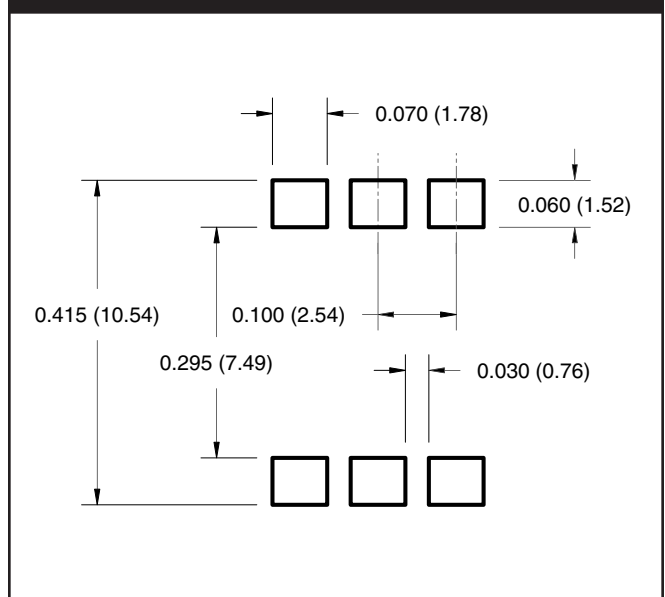
Package Dimensions (Surface Mount)



Package Dimensions (0.4" Lead Spacing)



**Recommended Pad Layout for
Surface Mount Leadform**



NOTE

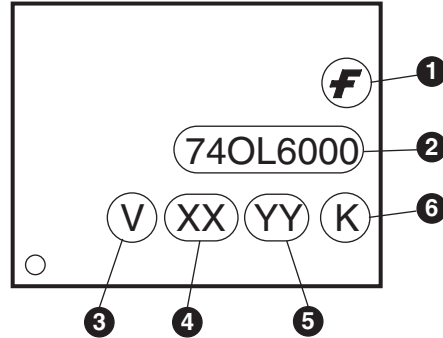
All dimensions are in inches (millimeters)

| | | |
|-----------------|---------------|----------|
| LSTTL TO | TTL BUFFER | 74OL6000 |
| | TTL INVERTER | 74OL6001 |
| | CMOS BUFFER | 74OL6010 |
| | CMOS INVERTER | 74OL6011 |

ORDERING INFORMATION

| Option | Order Entry Identifier | Description |
|--------|------------------------|--|
| S | .S | Surface Mount Lead Bend |
| SD | .SD | Surface Mount; Tape and Reel |
| W | .W | 0.4" Lead Spacing |
| 300 | .300 | VDE 0884 |
| 300W | .300W | VDE 0884, 0.4" Lead Spacing |
| 3S | .3S | VDE 0884, Surface Mount |
| 3SD | .3SD | VDE 0884, Surface Mount, Tape and Reel |

MARKING INFORMATION

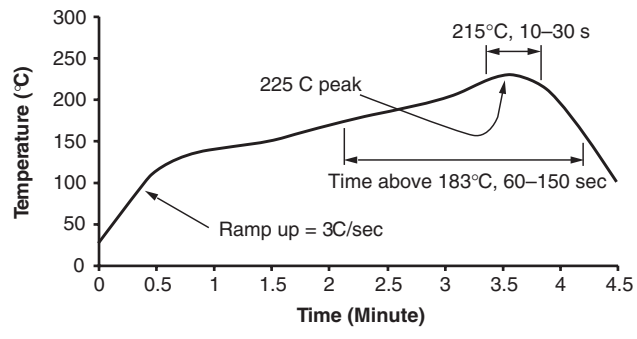


| Definitions | |
|-------------|--|
| 1 | Fairchild logo |
| 2 | Device number |
| 3 | VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table) |
| 4 | Two digit year code, e.g., '03' |
| 5 | Two digit work week ranging from '01' to '53' |
| 6 | Assembly package code |

LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

Reflow Profile (Black Package, No Suffix)



- Peak reflow temperature: 225°C (package surface temperature)
- Time of temperature higher than 183°C for 60–150 seconds
- One time soldering reflow is recommended

LSTTL TO

| | |
|---------------|----------|
| TTL BUFFER | 74OL6000 |
| TTL INVERTER | 74OL6001 |
| CMOS BUFFER | 74OL6010 |
| CMOS INVERTER | 74OL6011 |

APPLICATION

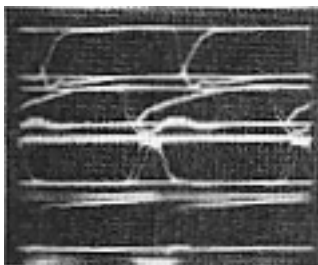
Local area data communication systems can greatly improve their noise immunity by including OPOTOLOGIC gates in the design.

The Optologic input amplifier offers the feature of very high input impedance that permits their use as bridged line receivers. The system show above illustrates an optically isolated transmitter and multidrop receiver system. The network uses a 74OL6000 and buffer (Figure D) to isolate the transmitter and drive the 75Ω coax cable. This application uses a 1000 ft. aerial suspension 75Ω CATV coax cable with data taps at 250 ft. intervals. The 74OL6001s function as bridged receivers, and as many as 30 receivers could be placed along the line with minimal signal degradation. The communication cable is terminated with a single 75Ω load at the far end of the line.

Signal quality "Eye Pattern" is shown in Figures A, B and C with a 10Mbaud NRZ Psuedo-Random Sequence (PRS). Traces 1-3 in Figure A describes the transmitter section. Traces 4-7 in Figure B show the output of the four Optologic bridged terminations. Traces 8-11 in Figure C illustrate "Eye Pattern" as seen at the output of a 74LS04 logic gate. The data quality is well preserved in that only a 30% Eye closure is seen at the receiver located 1000 ft. from the transmitter.

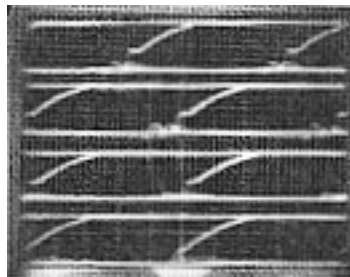
The data communication system is completely optically isolated from all of the terminal equipments. Power for the transmitter (V_{CCO}) and receiver (V_{CC}) is taken from an isolated power supply and distributed through a drain or messenger wire.

Figure A



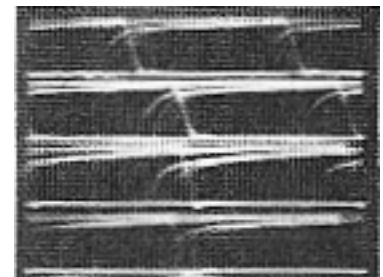
HORIZONTAL = 20 ns/DIV 42-11
VERTICAL = 2 V/DIV

Figure B



HORIZONTAL = 20 ns/DIV 42-12, 02
VERTICAL = 2 V/DIV

Figure C



HORIZONTAL = 20 ns/DIV 42-13/03
VERTICAL = 2 V/DIV

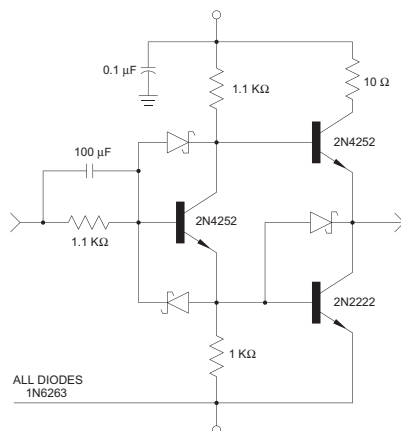
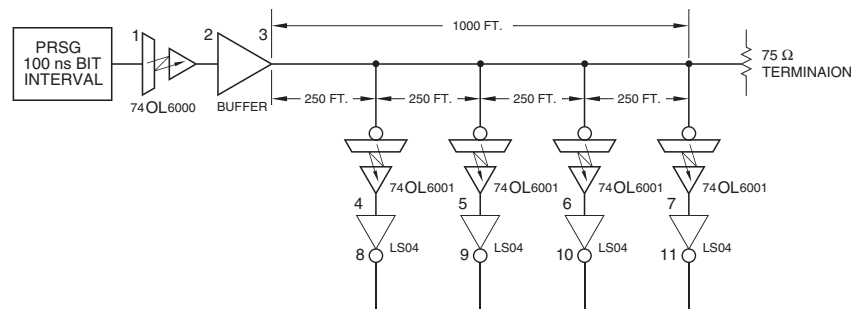


Figure D Buffer



| | | |
|-----------------|----------------------|-----------------|
| LSTTL TO | TTL BUFFER | 74OL6000 |
| | TTL INVERTER | 74OL6001 |
| | CMOS BUFFER | 74OL6010 |
| | CMOS INVERTER | 74OL6011 |

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