M62354AGP

8-bit 6ch D/A Converter with Buffer Amplifiers

REJ03D0871-0201
Rev.2.01
Dec 27, 2007

Description

M62354A is a CMOS structured semiconductor integrated circuit integrating 6 channels of built-in D/A converters with high performance buffer operational amplifier for each channel output.

3-wire serial interface (DI, CLK, LD) method is used for the transfer format of digital data to allow connection with microcomputer with minimum wiring DO terminal is provided to allow cascading serial use.

Built-in buffer operational amplifiers are designed to operate or full swing in the whole voltage range from V_{CC} to GND for each input/output. And their higher stability for capacitive load perfectly fits in to the use for electronic volume (VCA) or the replacement for semi-variable resistor for tuning.

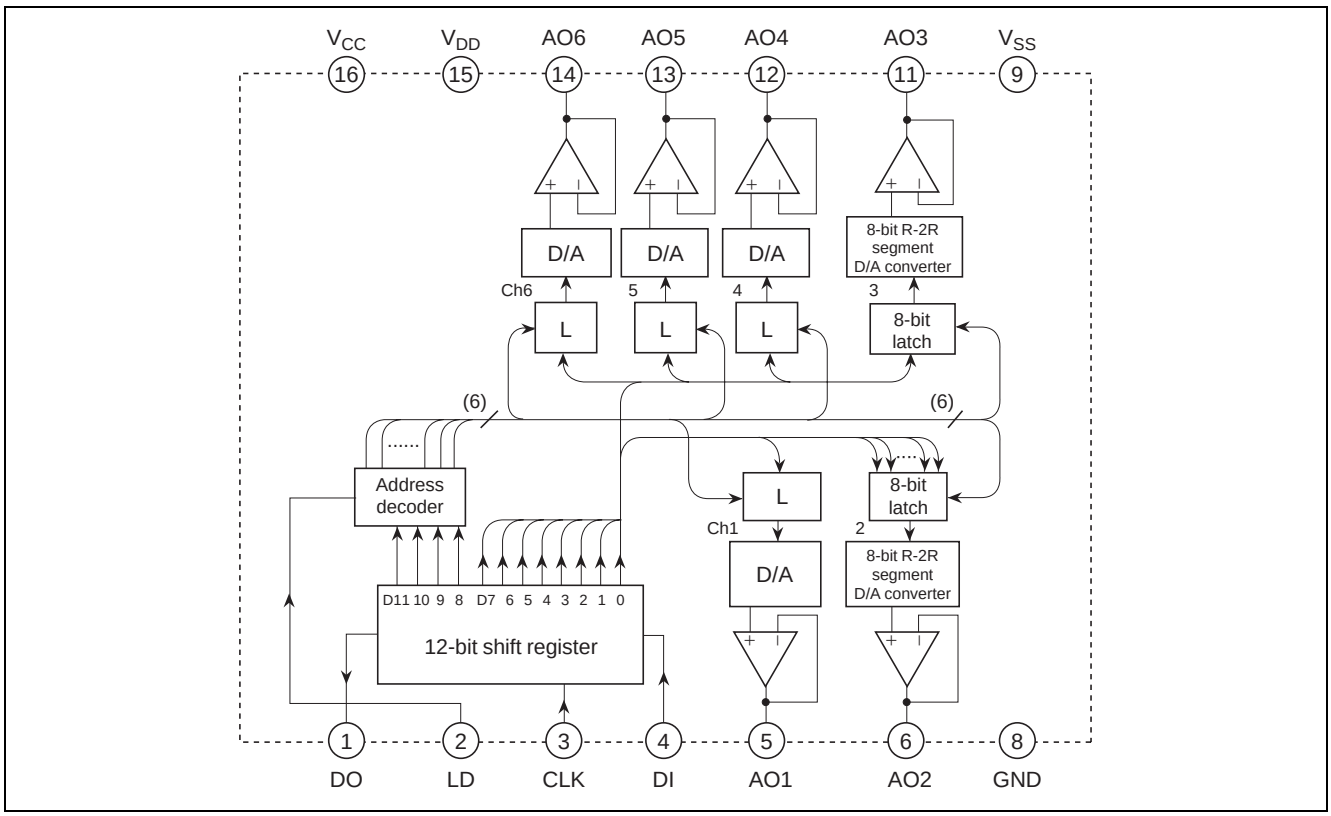
Features

- 12-bit serial data input (3 wire serial data transfer method, DI, CLK, LD)
- Corresponds to TTL input for digital input (VINH ≥ 2 V, VINL ≤ 0.8 V)
- R-2R + segment method high performance 6ch 8-bit D/A converters
- 6ch buffer operational amplifiers operating in the whole voltage range from V_{CC} to GND
- Buffer operational amplifiers with high oscillation stability for capacitive load

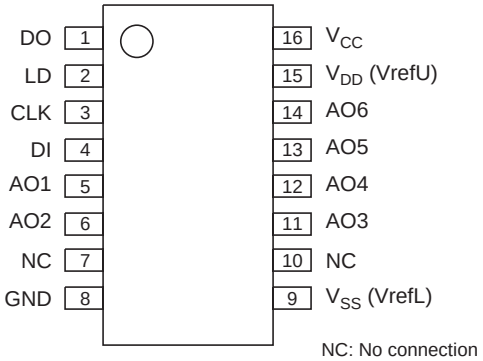
Application

Adjustment or control of industrial or home-use electronic equipments such as VTR camera, VTR set, TV, and CRT display.

Block Diagram



Pin Arrangement

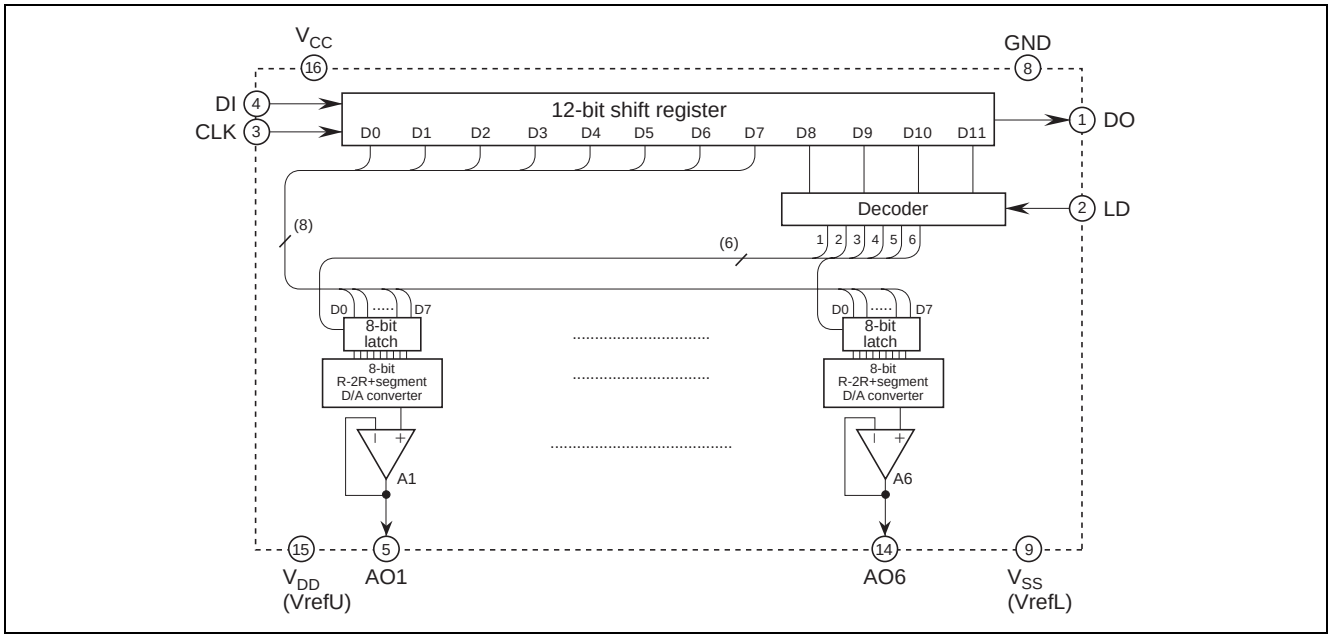


Outline: PLSP0016JA-A (16P2E-A)

Pin Description

Pin No.	Pin Name	Function
4	DI	Serial data input terminal. 12-bit serial data is input to this terminal.
1	DO	Serial data output terminal. Serial data of 12-bit shift register is output from this terminal.
3	CLK	Serial clock input terminal. Input signal from DI terminal is input to 12-bit shift register upon the rise of shift clock.
2	LD	Data is loaded to register when "H" is input to LD terminal.
5	AO1	8-bit D/A converter output terminal. Built-in buffer amp. is connected to V_{CC}. D/A converted voltage between V_{DD} and V_{SS} is output to each terminal.
6	AO2	
11	AO3	
12	AO4	
13	AO5	
14	AO6	
16	V_{CC}	Power supply terminal.
8	GND	Digital and analog common GND
15	V_{DD}	D/A converter High level reference voltage input terminal.
9	V_{SS}	D/A converter Low level reference voltage input terminal.

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
D/A converter High level reference voltage	V_{DD}	–0.3 to +7.0	V
Digital input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	Vout	–0.3 to V_{CC} + 0.3	V
Power dissipation	Pd	150	mW
Operating temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–40 to +125	°C

Electrical Characteristics

<Digital Part>

(V_{CC}, VrefU = 5 V ± 10%, V_{CC} ≥ VrefU, GND, VrefL = 0.0 V, Ta = –20 to +85°C unless otherwise specified.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Supply current	I_{CC}	—	0.7	2.5	mA	CLK = 1 MHz operation V_{CC} = 5 V, I_{AO} = 0 µA
Input leak current	I_{ILK}	–10	—	10	µA	V_{IN} = 0 to V_{CC}
Digital input Low voltage	V_{IL}	—	—	0.8	V	
Digital input High voltage	V_{IH}	2.0	—	—	V	
Digital output Low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.5 mA
Digital output High voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –400 µA

Note: Typical value is for Ta = 25°C

Changes from M62354GP: Digital input voltage corresponds to TTL spec.

<Analog Part>

(V_{CC}, VrefU = 5 V ± 10%, V_{CC} ≥ VrefU, GND, VrefL = 0.0 V, Ta = –20 to +85°C unless otherwise specified.)

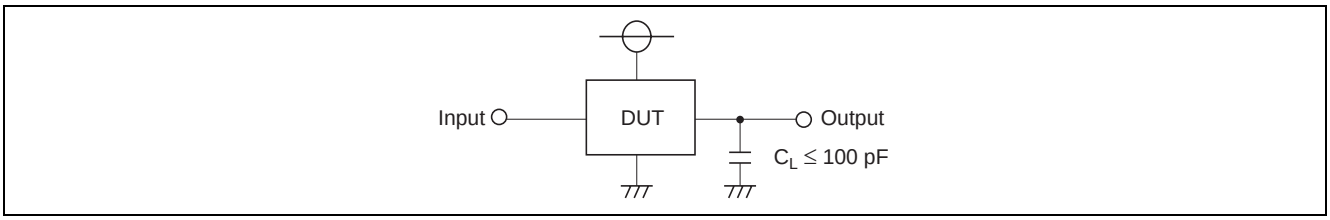
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Reference voltage pin current	IrefU	—	0.7	1.3	mA	VrefU = 5 V, VrefL = 0 V, I_{AO} = 0 µA Data condition: at maximum current
D/A converter High level reference voltage range	V_{DD} (VrefU)	3.5	—	V_{CC}	V	The output does not necessarily be the Values within the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range (V_{AO}).
D/A converter Low level reference voltage range	V_{SS} (VrefL)	GND	—	V_{CC} – 3.5	V	
Buffer amplifier output drive range	V_{AO}	0.1	—	V_{CC} – 0.1	V	I_{AO} = ± 100 µA
		0.2	—	V_{CC} – 0.2		I_{AO} = ± 500 µA
Buffer amplifier output drive range	I_{AO}	–1	—	1	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity	S_{DL}	–1.0	—	1.0	LSB	VrefU = 4.79 V VrefL = 0.95 V (15 mV/LSB) V_{CC} = 5.5 V Without load (I_{AO} = +0 µA)
Nonlinearity	S_L	–1.5	—	1.5	LSB	
Zero code error	S_{ZERO}	–2.0	—	2.0	LSB	
Full scale error	S_{FULL}	–2.0	—	2.0	LSB	
Output capacitive load	C_O	—	—	0.1	µF	
Buffer Amp. output impedance	R_O	—	5	—	Ω	

AC Characteristics

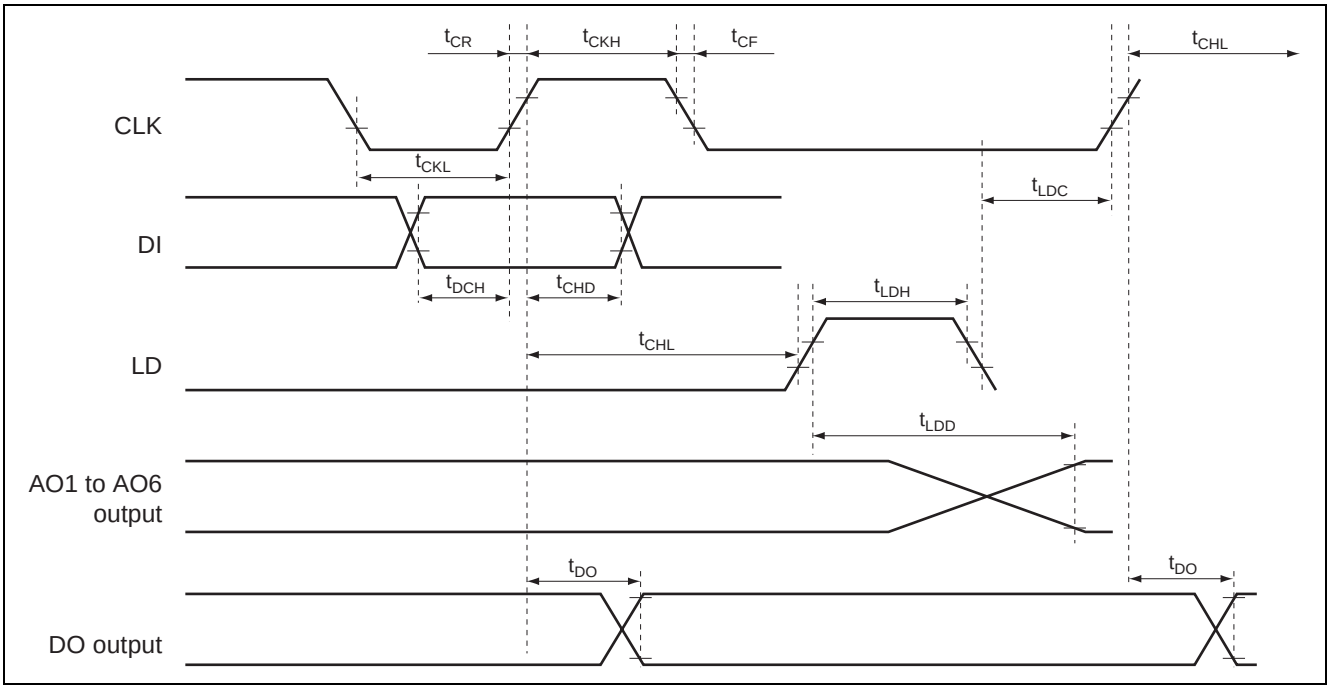
(V_{CC}, VrefU = 5 V ± 10%, V_{CC} ≥ VrefU, GND, VrefL = 0.0 V, Ta = –20 to +85°C unless otherwise specified.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}					
Data setup time	t_{DCH}	30	—	—	ns	
Data hold time	t_{CHD}	60	—	—	ns	
LD setup time	t_{CHL}	200	—	—	ns	
LD hold time	t_{LDC}	100	—	—	ns	
LD "H" hold time	t_{LDH}	100	—	—	ns	
Data output delay time	t_{DO}	70	—	350	ns	C_L ≤ 100 pF
D/A output setting time	t_{LDD}	—	—	300	µs	C_L ≤ 100 pF, V_{AO}: 0.5 ↔ 4.5 V The time until the output becomes the final value of 1/2 LSB

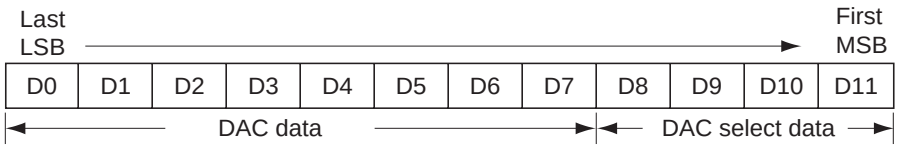
Measurement Circuit



Timing Chart



Digital Data Format



DAC Data

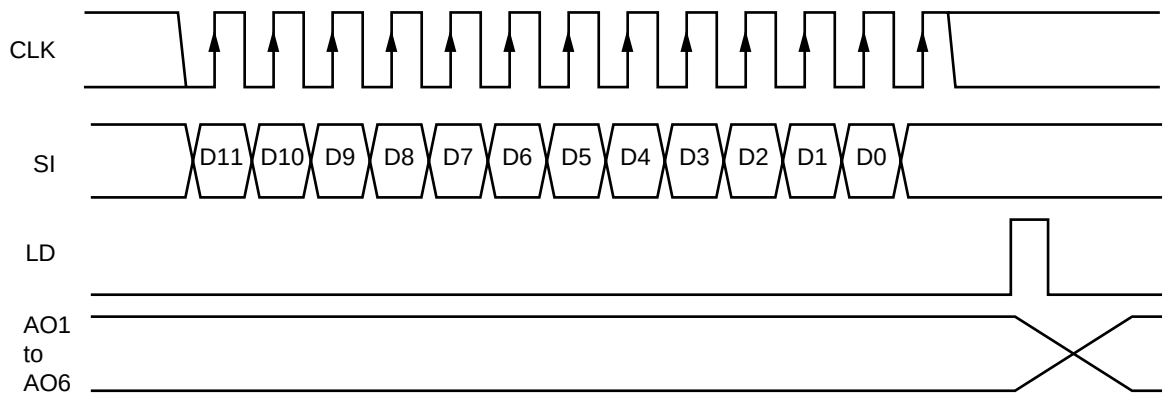
D0	D1	D2	D3	D4	D5	D6	D7	D/A Output	
0	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 1 + VrefL [V]	(1 LSB)
1	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 2 + VrefL [V]	(2 LSB)
0	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 3 + VrefL [V]	(3 LSB)
1	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 4 + VrefL [V]	(4 LSB)
:	:	:	:	:	:	:	:	:	
0	1	1	1	1	1	1	1	(VrefU – VrefL) / 256 × 255 + VrefL [V]	(255 LSB)
1	1	1	1	1	1	1	1	VrefU [V]	(256 LSB)

Note: VrefU = V_{DD}, VrefL = V_{SS}

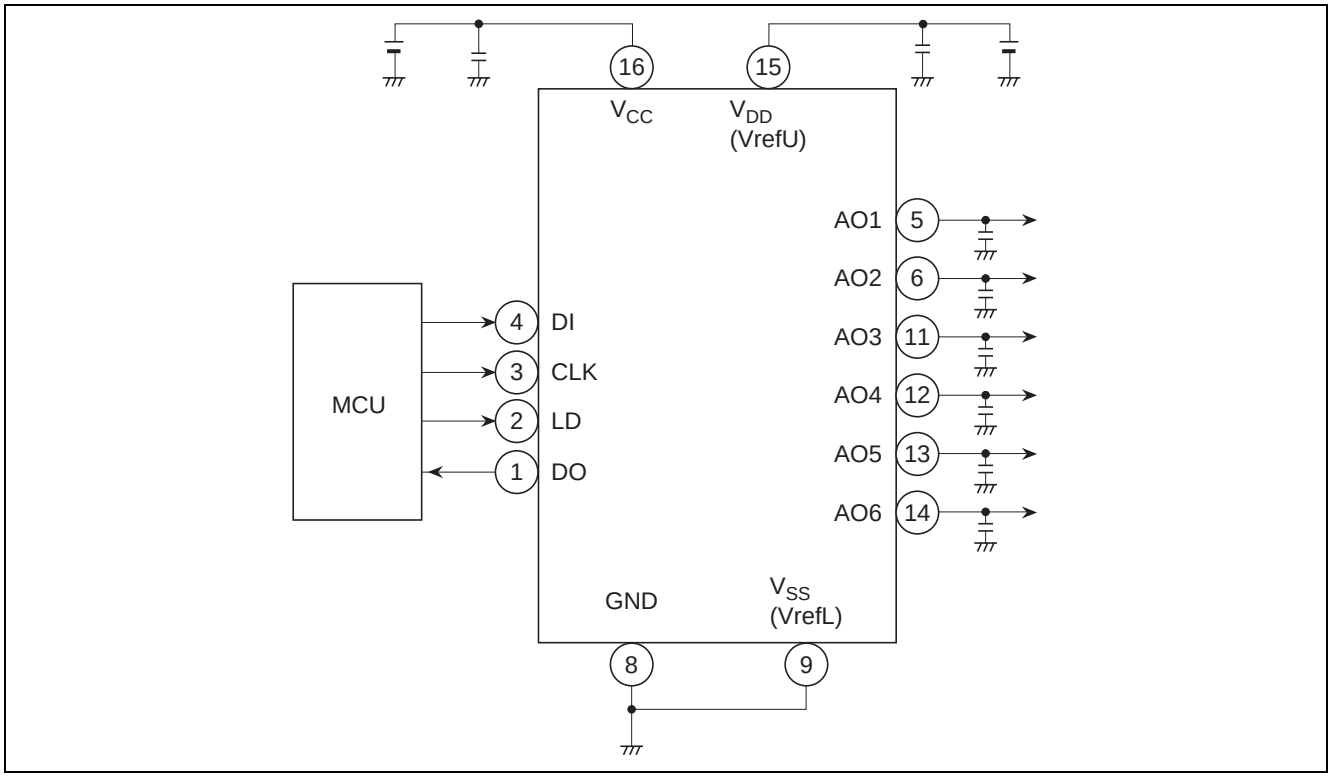
DAC Select Data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	AO1 select
0	0	1	0	AO2 select
0	0	1	1	AO3 select
0	1	0	0	AO4 select
0	1	0	1	AO5 select
0	1	1	0	AO6 select
0	1	1	1	Don't care
1	0	0	0	Don't care
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)



Typical Application



Precaution for Use

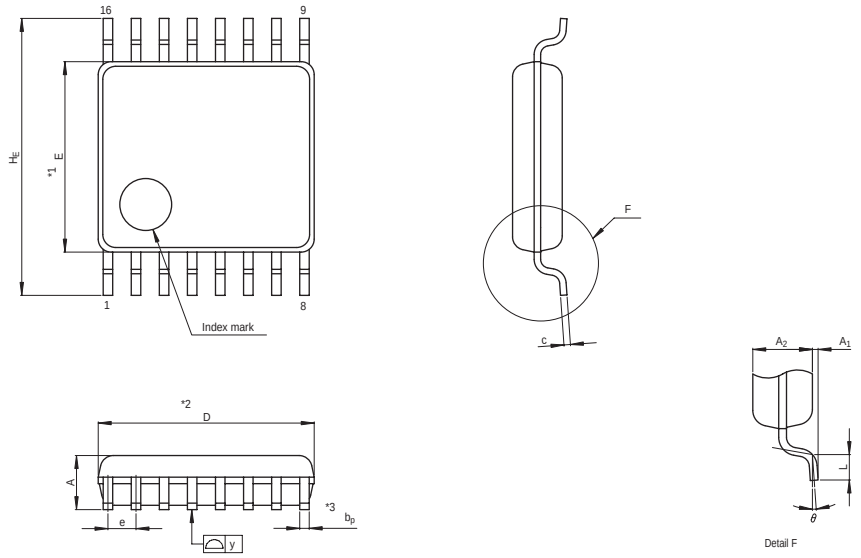
M62354AGP has 3 terminals (V_{DD}, V_{CC}, and V_{SS}) to which constant voltage is to be applied. Ripple voltage or spike noise to these terminals may worsen converting precision or cause erroneous operations. So be sure to use this device by putting capacitor between each terminal and GND to get D/A conversion operation stabilized.

Output buffer amplifiers have high oscillation stability against capacitive load. This means that jitters by wirings around output terminals or capacitor between output and GND (0.1 μF Max) do not cause any problems with DAC operations.

Connect capacitor (0.1 μF or around) between output and GND for protection from spark discharge when this device is used under such high electric field as that for instance of instruments with cathode ray tube.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP16-4.4x5-0.65	PLSP0016JA-A	16P2E-A	0.06g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

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