DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD77115, 77115A

16-BIT FIXED-POINT DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The μPD77115 and μPD77115A are 16-bit fixed-point digital signal processors (DSP).

The μPD77115 and μPD77115A are RAM based DSP and have the specific circuit for audio application.

Unless otherwise specified, the μPD77115 refers to μPD77115 and 77115A.

For details of the functions of the μPD77115, refer to the following User's Manuals:

μPD77111 Family User's Manual - Architecture : U14623E

μPD77016 Family User's Manual - Instructions : U13116E

FEATURES

- Instruction cycle (operating clock) 13.3 ns MIN. (75 MHz MAX.)
- Memory
  - Internal instruction RAM 11.5K words × 32 bits
  - Internal data RAM 16K words × 16 bits × 2 banks
- Peripherals
  - Audio serial interface
  - Secure Digital (SD) card interface
  - 16-bit timer
  - 16-bit host interface
  - 8-bit port
- Supply voltage
  - DSP core voltage
    2.0 to 2.7 V (MAX. operation speed 50 MHz)
    2.3 to 2.7 V (MAX. operation speed 75 MHz)
  - I/O pin voltage
    2.7 to 3.6 V
- Power consumption TYP. 50 mW (2.0 V, 50 MHz operation)

ORDERING INFORMATION

	Part Number	Package
★	μPD77115F1-CN6	80-pin plastic FBGA (9 × 9)
	μPD77115GK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
★	μPD77115AF1-xxx-CN6	80-pin plastic FBGA (9 × 9)

Remark xxx indicates ROM code suffix.

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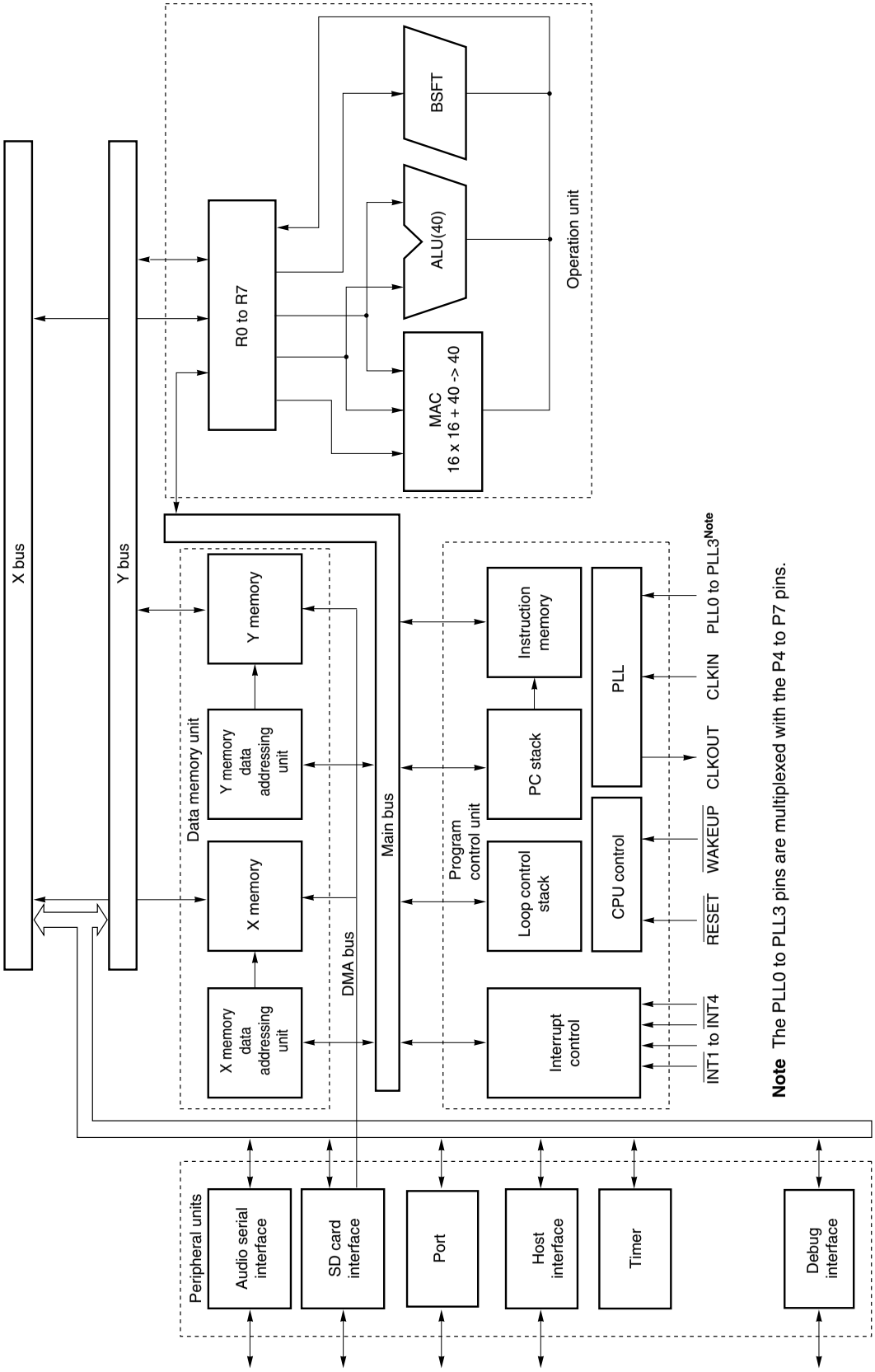
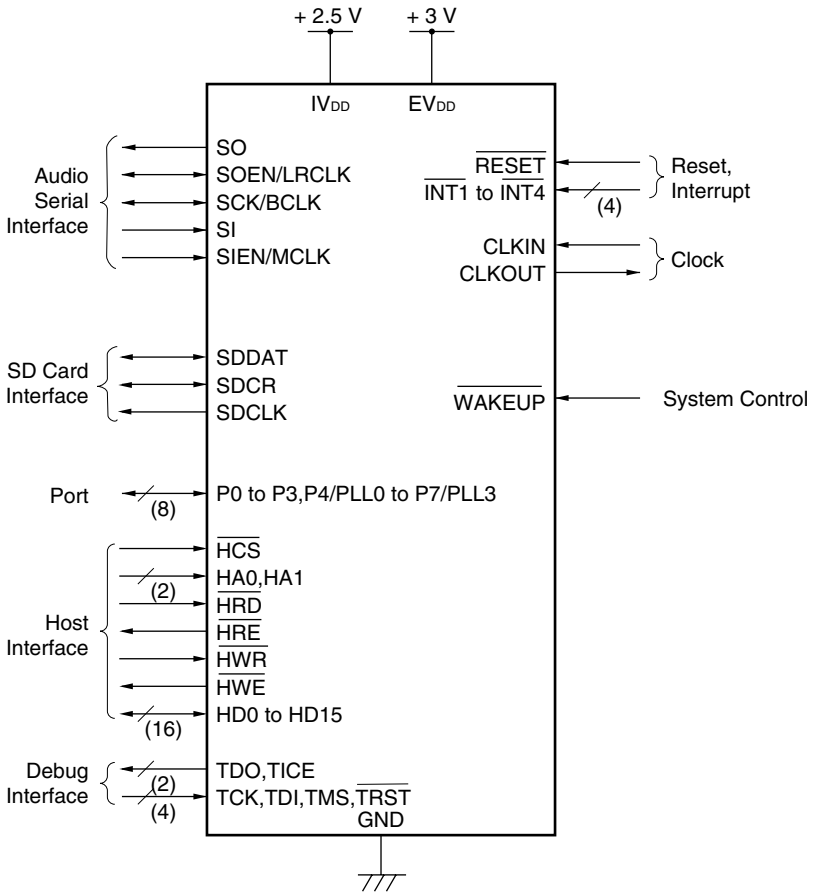
The mark ★ shows major revised points.

BLOCK DIAGRAM



FUNCTION PIN GROUPS



Remark The P4 to P7 pins are multiplexed with PLL0 to PLL3 pins.

★ DSP FUNCTION LIST

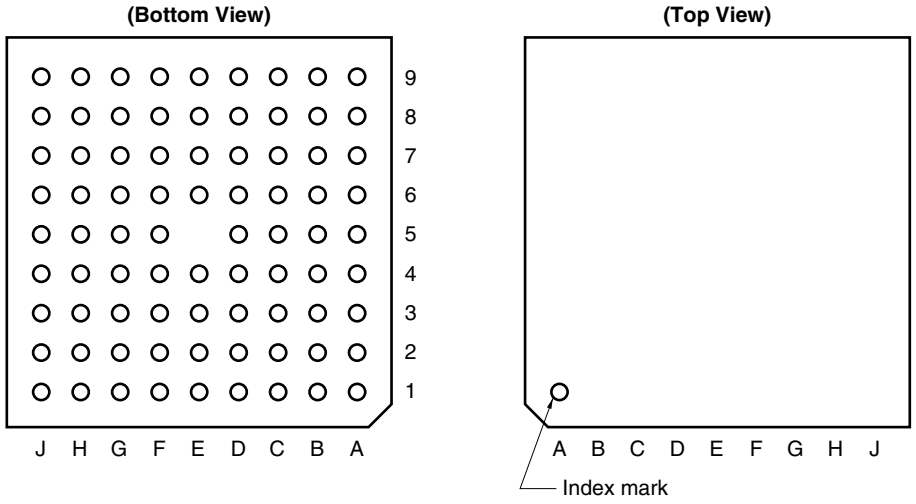
Item		μPD77110	μPD77111	μPD77112	μPD77113A	μPD77114	μPD77115,77115A	μPD77210	μPD77213
Memory space (words × bits)	Int. instruction RAM	35.5 K × 32	1 K × 32		3.5 K × 32		11.5 K × 32	31.5 K × 32	15.5 K × 32
	Int. instruction ROM	None	31.75 K × 32		48 K × 32		None		64K × 32
	Data RAM (X/Y memory)	24 K × 16 each	3 K × 16 each		16 K × 16 each		16 K × 16 each	30 K × 16 each	18 K × 16 each
	Data ROM (X/Y memory)	None	16 K × 16 each		32 K × 16 each		None		32 K × 16 each
	Ext. instruction	None							
	Ext. data memory (X/Y memory)	32 K × 16 each	None	16 K × 16 each	None	8 K × 16 each	None	1 M × 16	1 M × 16 (8 K × 16, using SD I/F)
Instruction cycle (at maximum operating speed)		15.3 ns (65 MHz)	13.3 ns (75 MHz)					6.25 ns (160 MHz)	8.33 ns (120 MHz)
Multiple		Integer multiple of ×1 to 8 (external pin)	Integer multiple of ×1 to 16 (mask option)				Integer multiple of ×1 to 16 (external pin)	Integer multiple of ×10 to 64 (external pin)	
Peripheral	Serial interface	2 channels (speech CODEC)					1 channel (audio CODEC)	2 channels (time-division, audio)	
	Host interface	8-bit bus					16-bit bus		
	General-purpose port (I/O programmable)	4 bits					8 bits	16 bits (some are alternative with host)	
	Timer	None					1 channel (16-bit resolution)	2 channels (16-bit resolution)	
	Others	–	–	–	–	–	SD card I/F	–	SD card I/F
Supply voltage		DSP core: 2.5 V I/O pins: 3 V						DSP core: 1.5 V I/O pins: 3 V	
Package		100-pin TQFP	80-pin TQFP 80-pin FBGA	100-pin TQFP	80-pin FBGA	100-pin TQFP	80-pin TQFP 80-pin FBGA	161-pin FBGA 144-pin LQFP	

PIN CONFIGURATIONS

80-pin plastic fine pitch BGA (9 × 9)

★ **μPD77115F1-CN6**

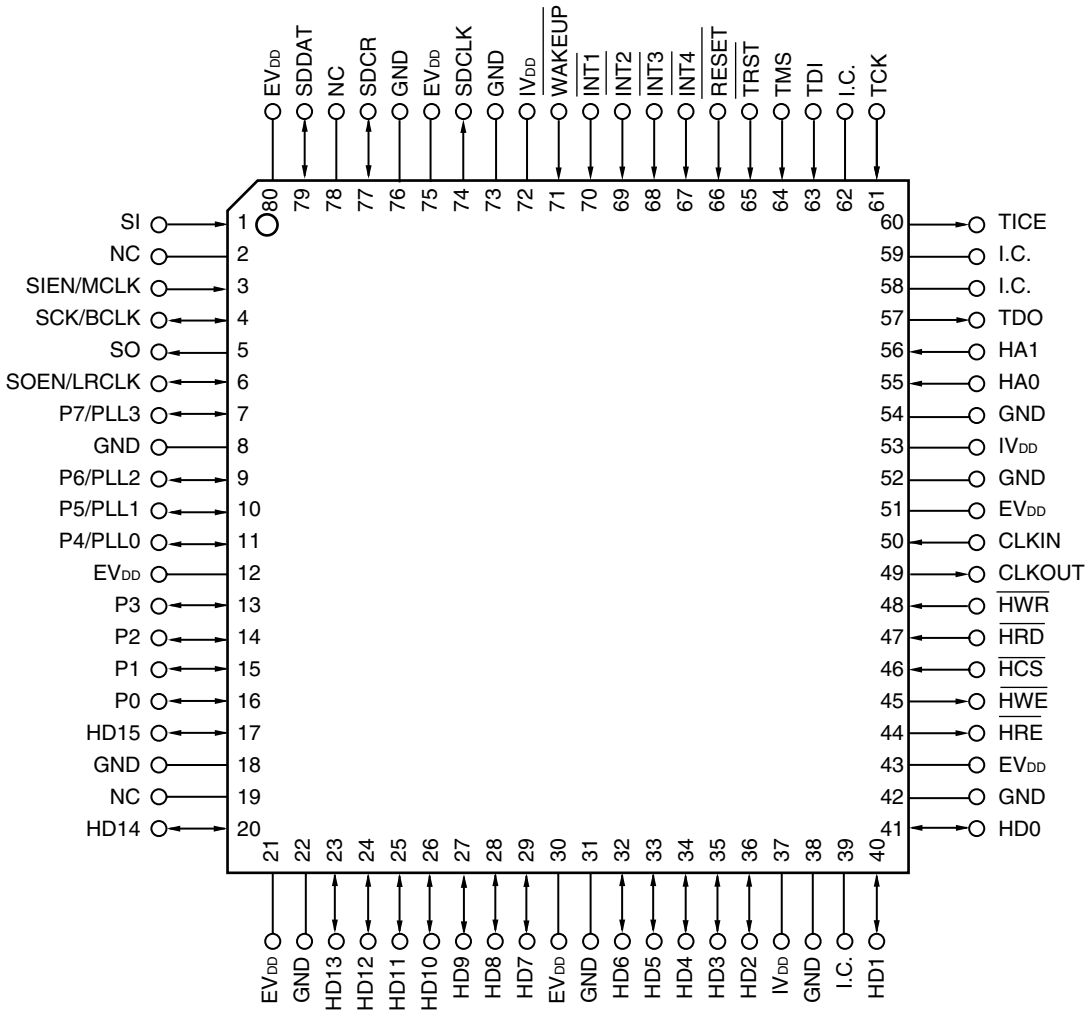
★ **μPD77115AF1-xxx-CN6**



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	EV_{DD}	C3	SDDAT	E6	GND	G8	$\overline{HRE}$
A2	NC	C4	GND	E7	$\overline{HWR}$	G9	EV_{DD}
A3	EV_{DD}	C5	$\overline{INT3}$	E8	EV_{DD}	H1	GND
A4	IV_{DD}	C6	$\overline{TRST}$	E9	CLKOUT	H2	EV_{DD}
A5	$\overline{INT2}$	C7	TICE	F1	EV_{DD}	H3	HD12
A6	$\overline{RESET}$	C8	TDO	F2	P0	H4	EV_{DD}
A7	TDI	C9	HA0	F3	P3	H5	GND
A8	I.C.	D1	SOEN/LRCLK	F4	HD9	H6	HD2
A9	I.C.	D2	P5/PLL1	F5	HD4	H7	IV_{DD}
B1	NC	D3	SO	F6	$\overline{HRD}$	H8	HD0
B2	SI	D4	P7/PLL3	F7	$\overline{HWE}$	H9	GND
B3	SDCR	D5	SDCLK	F8	CLKIN	J1	NC
B4	GND	D6	$\overline{INT4}$	F9	$\overline{HCS}$	J2	GND
B5	$\overline{WAKEUP}$	D7	IV_{DD}	G1	P1	J3	HD13
B6	$\overline{INT1}$	D8	HA1	G2	HD15	J4	HD10
B7	TMS	D9	GND	G3	HD14	J5	HD7
B8	TCK	E1	P6/PLL2	G4	HD11	J6	HD6
B9	I.C.	E2	P4/PLL0	G5	HD8	J7	HD3
C1	SIEN/MCLK	E3	GND	G6	HD5	J8	GND
C2	SCK/BCLK	E4	P2	G7	HD1	J9	I.C.

80-pin plastic TQFP (fine pitch) (12 × 12) (Top view)

μPD77115GK-9EU



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	SI	21	EV_{DD}	41	HD0	61	TCK
2	NC	22	GND	42	GND	62	I.C.
3	SIEN/MCLK	23	HD13	43	EV_{DD}	63	TDI
4	SCK/BCLK	24	HD12	44	$\overline{HRE}$	64	TMS
5	SO	25	HD11	45	$\overline{HWE}$	65	$\overline{TRST}$
6	SOEN/LRCLK	26	HD10	46	$\overline{HCS}$	66	$\overline{RESET}$
7	P7/PLL3	27	HD9	47	$\overline{HRD}$	67	$\overline{INT4}$
8	GND	28	HD8	48	$\overline{HWR}$	68	$\overline{INT3}$
9	P6/PLL2	29	HD7	49	CLKOUT	69	$\overline{INT2}$
10	P5/PLL1	30	EV_{DD}	50	CLKIN	70	$\overline{INT1}$
11	P4/PLL0	31	GND	51	EV_{DD}	71	$\overline{WAKEUP}$
12	EV_{DD}	32	HD6	52	GND	72	IV_{DD}
13	P3	33	HD5	53	IV_{DD}	73	GND
14	P2	34	HD4	54	GND	74	SDCLK
15	P1	35	HD3	55	HA0	75	EV_{DD}
16	P0	36	HD2	56	HA1	76	GND
17	HD15	37	IV_{DD}	57	TDO	77	SDCR
18	GND	38	GND	58	I.C.	78	NC
19	NC	39	I.C.	59	I.C.	79	SDDAT
20	HD14	40	HD1	60	TICE	80	EV_{DD}

PIN NAME

CLKIN : Clock Input
CLKOUT : Clock Output
EV_{DD} : Power Supply for I/O Pins
GND : Ground
HA0, HA1 : Host Data Access
$\overline{HCS}$: Host Chip Select
HD0 to HD15 : Host Data Bus
$\overline{HRD}$: Host Read
$\overline{HRE}$: Host Read Enable
$\overline{HWE}$: Host Write Enable
$\overline{HWR}$: Host Write
I.C. : Internally Connected
$\overline{INT1}$ to $\overline{INT4}$: Interrupt
IV_{DD} : Power Supply for DSP Core
NC : Non-Connection
P0 to P3 : Port
P4/PLL0 to P7/PLL3 : Port/ PLL Setting Input
$\overline{RESET}$: Reset
SCK/BCLK : Serial Clock Input/ Output
SDCLK : SD Card Clock Output
SDCR : SD Card Command Output/ Response Input
SDDAT : SD Card Data Input/ Output
SI : Serial Data Input
SIEN/MCLK : Serial Input Enable/ Master Clock Input
SO : Serial Data Output
SOEN/LRCLK : Serial Output Enable/ Left Right Clock Input/ Output
TCK : Test Clock Input
TDI : Test Data Input
TDO : Test Data Output
TICE : Test In-Circuit Emulator
TMS : Test Mode Select
$\overline{TRST}$: Test Reset
$\overline{WAKEUP}$: Wakeup from STOP Mode

CONTENTS

1. PIN FUNCTION

Because the pin numbers differ depending on the package, refer to the diagram of the package to be used.

1.1 Pin Function Description

- **Power supply**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
IV_{DD}	A4,D7,H7	37,53,72	–	Power to DSP core (+2.5 V)	–
EV_{DD}	A1,A3,E8,F1, G9,H2,H4	12,21,30,43,51, 75,80	–	Power to I/O pins (+3 V)	–
GND	B4,C4,D9,E3, E6,H1,H5,H9, J2,J8	8,18,22,31, 38,42,52,54, 73,76	–	Ground	–

- **System control**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
CLKIN	F8	50	Input	System clock input	–
CLKOUT	E9	49	Output	Internal system clock output	–
PLL0 to PLL3	E2,D2,E1,D4	11,10,9,7	Input	PLL multiple rate setting pin PLL3 to PLL0: 0000 : x16, 0001 : x1, 0010 : x2, 0011 : x3, 0100 : x4, 0101 : x5, 0110 : x6, 0111 : x7, 1000 : x8, 1001 : x9, 1010 : x10, 1011 : x11, 1100 : x12, 1101 : x13, 1110 : x14, 1111 : x15	P4 to P7
$\overline{\text{RESET}}$	A6	66	Input	Internal system reset signal input	–
$\overline{\text{WAKEUP}}$	B5	71	Input	Stop mode release signal input. • When this pin is asserted active, the stop mode is released.	–

- **Interrupt**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
$\overline{\text{INT1}}$ to $\overline{\text{INT4}}$	B6,A5,C5,D6	70,69,68,67	Input	External maskable interrupt input. • Detected at the falling edge.	–

• **Serial interface**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
SCK/BCLK	C2	4	I/O	Serial clock input/output SCK : Standard serial interface(input) BCLK : Audio serial interface(I/O)	–
SOEN/LRCLK	D1	6	I/O	Serial output enable / Left Right clock input/output SOEN : Standard serial interface(input) LRCLK : Audio serial interface(I/O)	–
SO	D3	5	Output (3S)	Serial data output	–
SIEN/MCLK	C1	3	Input	Serial input enable / Master clock input SIEN : Standard serial interface MCLK : Audio serial interface (Master clock input when master mode)	–
SI	B2	1	Input	Serial data input	–

Remark The pins marked “3S” under the heading “I/O” go into a high-impedance state on completion of data transfer and input of the hardware reset ($\overline{\text{RESET}}$) signal.

• **SD card interface**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
SDCLK	D5	74	Output	SD card clock output	–
SDCR	B3	77	I/O (3S)	SD card command/response Input : Response Output : Command •Leave pulled up.	–
SDDAT	C3	79	I/O (3S)	SD card data input/output Input : Read data Output : Write data •Leave pulled up.	–

Remark The pins marked “3S” under the heading “I/O” go into a high-impedance state when the SD card interface is not being accessed.

• **Host interface**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
HA1	D8	56	Input	Specifies the register to be accessed by HD15 to HD0. • 1: Accesses the host interface status register (HST). • 0: Accesses the host transmit data register (HDT (out)) when read ($\overline{HRD}$ = 0), and host receive data register (HDT (in)) when written ($\overline{HWR}$ = 0).	–
HA0	C9	55	Input	Specifies the register to be accessed by HD15 to HD0. • 1: Accesses bits 15 to 8 of HST, HDT (in), and HDT (out). • 0: Accesses bits 7 to 0 of HST, HDT (in), and HDT (out). When 8-bit mode, this signal becomes valid. When 16-bit mode, this signal becomes invalid.	–
$\overline{HCS}$	F9	46	Input	Chip select input	–
$\overline{HRD}$	F6	47	Input	Host read input	–
$\overline{HWR}$	E7	48	Input	Host write input	–
$\overline{HRE}$	G8	44	Output	Host read enable output	–
$\overline{HWE}$	F7	45	Output	Host write enable output	–
HD0 to HD15	H8,G7,H6,J7, F5,G6,J6,J5, G5,F4,J4,G4, H3,J3,G3,G2	41,40,36,35, 34,33,32,29, 28,27,26,25, 24,23,20,17	I/O (3S)	16-bit host data bus	–

Remark The pins marked “3S” under the heading “I/O” go into a high-impedance state when the host interface is not being accessed.

• **I/O ports**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
P0	F2	16	I/O	General-purpose I/O port	–
P1	G1	15	I/O		–
P2	E4	14	I/O		–
P3	F3	13	I/O		–
P4	E2	11	I/O		PLL0
P5	D2	10	I/O		PLL1
P6	E1	9	I/O		PLL2
P7	D4	7	I/O		PLL3

• **Debugging interface**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
TDO	C8	57	Output	For debugging	–
TICE	C7	60	Output		–
TCK	B8	61	Input		–
TDI	A7	63	Input		–
TMS	B7	64	Input		–
$\overline{\text{TRST}}$	C6	65	Input		–

• **Others**

Pin Name	Pin No.		I/O	Function	Shared by:
	80-pin FBGA	80-pin TQFP			
I.C.	A8,A9,B9,J9	39,58,59,62	–	Internally connected. Leave this pin unconnected.	–
NC	A2,B1,J1	2,19,78	–	No-connect pins. Leave these pins unconnected.	–

Caution If any signal is input to these pins or if an attempt is made to read these pins, the normal operation of the μPD77115 is not guaranteed.

1.2 Connection of Unused Pins

1.2.1 Connection of function pins

When mounting, connect unused pins as follows:

Pin	I/O	Recommended Connection
$\overline{\text{INT1}}$ to $\overline{\text{INT4}}$	Input	Connect to EV_{DD}.
SCK/BCLK	I/O	Connect to EV_{DD} or GND.
SI	Input	
SIEN/MCLK	Input	Connect to GND.
SOEN/LRCLK	I/O	
SO	Output	Leave unconnected
SDCLK	Output	
SDCR	I/O	Connect to EV_{DD} via pull-up resistor, or connect to GND via pull-down resistor.
SDDAT	I/O	
HA0, HA1	Input	Connect to EV_{DD} or GND.
$\overline{\text{HCS}}$, $\overline{\text{HRD}}$, $\overline{\text{HWR}}$	Input	Connect to EV_{DD}.
$\overline{\text{HRE}}$, $\overline{\text{HWE}}$	Output	Leave unconnected.
HD0 to HD15[Note]	I/O	Connect to EV_{DD} via pull-up resistor, or connect to GND via pull-down resistor.
P0 to P3	I/O	
TCK	Input	Connect to GND via pull-down resistor.
TDO, TICE	Output	Leave unconnected.
TMS, TDI	Input	Leave unconnected. (internally pulled up).
$\overline{\text{TRST}}$	Input	Leave unconnected. (internally pulled down).
CLKOUT	Output	Leave unconnected.
$\overline{\text{WAKEUP}}$	Input	Connect to EV_{DD}.

Note These pins may be left unconnected if $\overline{\text{HCS}}$, $\overline{\text{HRD}}$, and $\overline{\text{HWR}}$ are fixed to the high level. However, connect these pins as recommended in the halt and stop modes when the power consumption must be lowered.

1.2.2 Connection of no-function pins

Pin	I/O	Recommended Connection
I.C.	–	Leave unconnected.
NC	–	Leave unconnected.

2. FUNCTION OUTLINE

2.1 Program Control Unit

This unit is used to execute instructions, and control branching, loops, interrupts, the clock, and the standby mode of the DSP.

2.1.1 CPU control

A three-stage pipeline architecture is employed and almost all the instructions, except some instructions such as branch instructions, are executed in one system clock.

2.1.2 Interrupt control

Interrupt requests input from external pins ($\overline{INT1}$ to $\overline{INT4}$) or generated by the internal peripherals (serial interface and host interface) are serviced. The interrupt of each interrupt source can be enabled or disabled. Multiple interrupts are also supported.

2.1.3 Loop control task

A loop function without any hardware overhead is provided. A loop stack with four levels is provided to support multiple loops.

2.1.4 PC stack

A 15-level PC stack that stores the program counter supports multiple interrupts and subroutine calls.

2.1.5 PLL

A PLL is provided as a clock generator that can multiply an external clock input to supply an operating clock to the DSP. A multiple of ×1 to ×16 can be set by pins(PLL0 to PLL3).

Two standby modes are available for lowering the power consumption while the DSP is not in use.

- HALT mode : Set by execution of the HALT instruction. The current consumption drops to several mA. The normal operation mode is recovered by an interrupt or hardware reset.
- STOP mode: Set by execution of the STOP instruction. The current consumption drops to several 10 μA. The normal operation mode is recovered by hardware reset or $\overline{WAKEUP}$ pin.

2.1.6 Instruction memory

64 words of the instruction RAM are allocated to interrupt vectors.

A boot-up ROM that boots up the instruction RAM is provided, and the instruction RAM can be initialized or rewritten by host boot (boot via host interface).

The μPD77115 has 11.5K-word instruction RAM.

2.2 Arithmetic Unit

This unit performs multiplication, addition, logical operations, and shift, and consists of a 40-bit multiply accumulator, 40-bit data ALU, 40-bit barrel shifter, and eight 40-bit general-purpose registers.

2.2.1 General-purpose registers (R0 to R7)

These eight 40-bit registers are used to input/output data for arithmetic operations, and load or store data from/to data memory.

A general-purpose register (R0 to R7) is made up of three parts: R0L to R7L (bits 15 to 0), R0H to R7H (bits 31 to 16), and R0E to R7E (bits 39 to 32). Depending on the type of operation, RnL, RnH, and RnE are used as one register or in different combinations.

2.2.2 Multiply accumulator (MAC)

The MAC multiplies two 16-bit values, and adds or subtracts the multiplication result from one 40-bit value, and outputs a 40-bit value.

The MAC is provided with a shifter (MSFT: MAC ShiFTer) at the stage preceding the input stage. This shifter can arithmetically shift the 40-bit value to be added to or subtracted from the multiplication result 1 or 16 bits to the right .

2.2.3 Arithmetic logic unit (ALU)

This unit inputs one or two 40-bit values, executes an arithmetic or logical operation, and outputs a 40-bit value.

2.2.4 Barrel shifter (BSFT: Barrel ShiFTer)

The barrel shifter inputs a 40-bit value, shifts it to the left or right by any number of bits, and outputs a 40-bit value. The data may be arithmetically shifted to the right shifted to the right, in which case the data is sign-extended, or logically shifted to the right, in which case 0 is inserted from the MSB.

2.3 Data Memory Unit

The data memory unit consists of two banks of data memory and two data addressing units.

2.3.1 Data memory

The DSP have two banks of data memory (X data memory and Y data memory). A 64-word peripheral area is assigned in the data memory space.

The μPD77115 has 16K words × 2 banks data RAM.

2.3.2 Data addressing unit

An independent data addressing unit is provided for each of the X data memory and Y data memory spaces.

Each data addressing unit has four data pointers (DPn), four index registers (DNn), one modulo register (DMX or DMY), and an address ALU.

2.4 Peripheral Unit

A serial interface, host interface, general-purpose I/O port, and wait cycle register are provided. All these internal peripherals are mapped to the X data memory and Y data memory spaces, and are accessed from program as memory-mapped I/Os.

2.4.1 Audio Serial interface (ASIO)

One serial interface is provided. This serial interface has two mode which are the audio serial and the standard serial. The standard serial is compatible other μPD77111 family DSP.

The audio serial interfaces have the following features:

- Mode : Master mode or Slave mode
  Master mode : MCLK (input), BCLK (output), LRCLK (output), support 256 fs, 384 fs and 512 fs
  Slave mode : MCLK (unused), BCLK (input), LRCLK (input)
- Frame format : 32 or 64 bits audio format (LRCLK format), MSB first input/output.
- Handshake : Handshaking with the external devices is implemented with a dedicated frame signal (LRCLK). Handshaking with the internal units, polling, wait, or interrupt are used.

The standard serial interfaces have the following features:

- Serial clock : Supplied from external source to each interface. The same clock is used for input and output on the interface.
- Frame length : 8 or 16 bits, and MSB or LSB first selectable for each input or output
- Handshake : Handshaking with external devices is implemented with a dedicated status signal. With the internal units, polling, wait, or interrupt are used.

2.4.2 Host interface (HIO)

This is an 16-bit parallel port that inputs data from or outputs data to an external host CPU or DMA controller. In the DSP, a 16-bit register is mapped to memory for input data, output data, and status. Handshaking with an external device is implemented by using a dedicated status signal or a dedicated status register. Handshaking with internal units is achieved by means of polling, wait, or interrupts.

2.4.3 General-purpose I/O port (PIO)

This is a 8-bit I/O port that can be set in the input or output mode in 1-bit units.

2.4.4 SD card interface (SDCIF)

This interface is for access SD card. It supports the DMA transfer for input data to internal data RAM. The SD card is accessed by using a dedicated routine of system ROM.

2.4.5 Timer

This is 16-bit timer unit. The count source can be selected from system clock, SD card clock, serial clock and $\overline{\text{INT4}}$ input. Timer unit generates interrupt for interface internal units.

3. RESET FUNCTION

When a low level of a specified width is input to the $\overline{\text{RESET}}$ pin, the device is initialized.

3.1 Hardware Reset

If the $\overline{\text{RESET}}$ pin is asserted active (low level) for a specified period, the internal circuitry of the DSP is initialized. If the $\overline{\text{RESET}}$ pin is then deasserted inactive (high level), boot processing of the instruction RAM is performed according to the status of the port pins (P0 and P1). After boot processing, processing is executed starting from the instruction at address 0x200 of instruction memory (reset entry).

No power-ON reset function is available.

3.2 Initializing PLL

Initializing the PLL starts during boot up program at reset. The pins (PLL0 to PLL3) that specify the PLL multiple rate must be kept stable for the duration of 3 clocks before and for the duration of 50 clocks after reset has been cleared (the clock is input from CLKIN). It takes the PLL 100 μs to be locked. Until the PLL is lacked, the DSP internal is operated by the CLKIN clock.

To use the PLL clock as an internal operating clock, set the clock control register (internal peripheral) by user program.

4. FUNCTIONS OF BOOT-UP ROM

To rewrite the contents of the instruction memory on power application or from program, boot up the instruction RAM by using the internal boot-up ROM.

The μPD77115 has a function to verify the contents of the internal instruction RAM.

4.1 Boot at Reset

After hardware reset has been cleared, the boot program first reads the general-purpose I/O ports P0 and P1 and, depending on their bit pattern, determines the boot mode (host boot or non boot). After boot processing, processing is executed starting from the instruction at address 0x200 (reset entry) of the instruction memory.

The pins (P0 and P1) that specify the boot mode must be kept stable for the duration of 3 clocks before and for the duration of 12 clocks after reset has been cleared (the clock is input from CLKIN).

P1	P0	Boot Mode
0	0	Does not execute boot but branches to address 0x200[Note].
0	1	Executes host byte boot and then branches to address 0x200.
1	0	Setting prohibited
1	1	Executes host word boot and then branches to address 0x200.

Note This setting is used when the DSP must be reset to recover from the standby mode after reset boot has been executed once.

A boot parameter and instruction code are obtained via the host interface, and transferred to the instruction RAM. The data transfer support byte mode and word mode.

4.2 Reboot

By calling the reboot entry address from the program, the contents of the instruction RAM can be rewritten. An instruction code is obtained via the host interface and transferred to the instruction RAM. The data transfer support byte mode and word mode.

The entry address is 0x6. Host reboot is executed by calling this address after setting the following parameter:

- R7L : Number of instruction steps for rebooting
- DP3: First address of instruction memory to be loaded

4.3 Signature Operation

The μPD77115 has a signature operation function so that the contents of the internal instruction RAM can be verified. The signature operation performs a specific arithmetic operation on the data in the instruction RAM booted up, and returns the result to a register. Perform the signature operation in advance on the device when it is operating normally, and repeat the signature operation later to check whether the data in RAM is correct by comparing the operation result with the previous result. If the results are identical, there is no problem.

The entry address is 0x9. Execute the operation by calling this address after setting the following parameter. The operation result is stored in register R7.

- R7L: Number of instruction steps for operation
- DP3: First address of instruction memory for operation

5. STANDBY MODES

Two standby modes are available. By executing the corresponding instruction, each mode is set and the power consumption can be reduced.

5.1 HALT Mode

To set this mode, execute the HALT instruction. In this mode, functions other than clock circuit and PLL are stopped to reduce the current consumption.

To release the HALT mode, use an interrupt or hardware reset. When releasing the HALT mode using an interrupt, the contents of the internal registers and memory are retained. It takes several 10 system clocks to release the HALT mode when the HALT mode is released using an interrupt.

In the HALT Mode, the clock circuit of the μPD77115 supplies the following clock as the internal system clock. The clock output from the CLKOUT pin is also as follows.

The clock output from the CLKOUT pin, however, has a high-level width that is equivalent to 1 cycle of the normal operation (i.e., the duty factor is not 50%).

- μPD77115: 1/I of internal system clock (I = integer from 1 to 16, specified by register)

5.2 STOP Mode

To set the STOP mode, execute the STOP instruction. In the STOP mode, all the functions, including the clock circuit and PLL, can be stopped and the power consumption is minimized with only leakage current flowing.

To release the STOP mode, use hardware reset or $\overline{\text{WAKEUP}}$ pin.

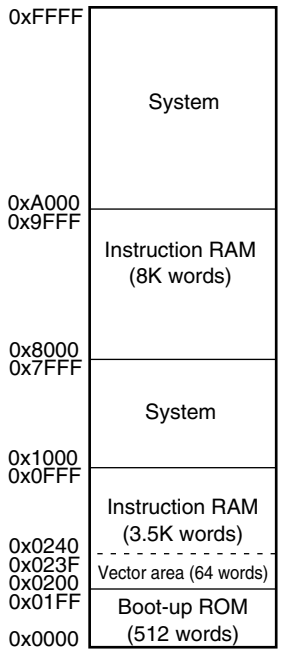
When releasing the STOP mode by using the $\overline{\text{WAKEUP}}$ pin, the contents of the internal registers and memory are retained, but it takes several 100 μs to release the mode.

6. MEMORY MAP

A Harvard architecture, in which the instruction memory space and data memory space are separated is employed.

6.1 Instruction Memory

★ #### 6.1.1 Instruction memory map



Caution Programs and data cannot be placed at addresses reserved for the system, nor can these addresses be accessed. If these addresses are accessed, the normal operation of the device cannot be guaranteed.

6.1.2 Interrupt vector table

Addresses 0x200 to 0x23F of the instruction memory are entry points (vectors) of interrupts. Four instruction addresses are assigned to each interrupt source.

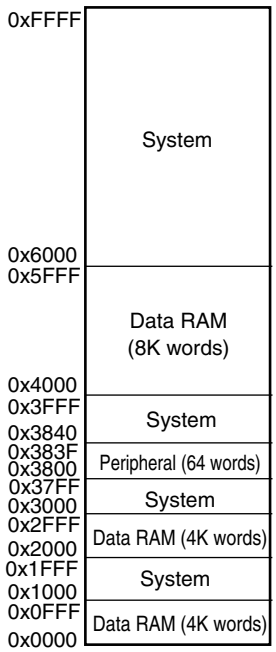
Vector	Interrupt Source
0x200	Reset
0x204	Reserved
0x208	
0x20C	
0x210	INT1
0x214	INT2
0x218	INT3
0x21C	INT4
0x220	SI input
0x224	SO output
0x228	SDDAT input / PBU
0x22C	SDDAT output
0x230	HI input
0x234	HO output
0x238	SDCR input
0x23C	Timer

Cautions 1. Although reset is not an interrupt, it is handled like an interrupt as an entry to a vector.

2. It is recommended that unused interrupt source vectors be used to branch an error processing routine.

6.2 Data Memory

6.2.1 Data memory map



Caution Programs and data cannot be placed at addresses reserved for the system, nor can these addresses be accessed. If these addresses are accessed, the normal operation of the device cannot be guaranteed.

6.2.2 Internal peripherals

The internal peripherals are mapped to the internal data memory space.

X/Y Memory Address	Register Name	Function	Peripheral Name
0x3800	SDT/ASDT	Serial data register	ASIO
0x3801	SST	Serial status register	
0x3802	ASST	Audio serial status register	
0x3803	Reserved area	**Caution Do not access this area.**	–
0x3804	PDT	Port data register	PIO
0x3805	PCD	Port command register	
0x3806	HDT	Host data register	HIO
0x3807	HST	Host status register	
0x3808 to 0x380F	Reserved area	**Caution Do not access this area.**	–
0x3810	SDDR	SD card data register	SDCIF
0x3811	SDCMD_IDX	SD card command register index	
0x3812	SDCMD_AGH	SD card command register argument high	
0x3813	SDCMD_AGL	SD card command register argument low	
0x3814	SDCTL	SD card control register	
0x3815	SDRPR	SD card response register	
0x3816	SDSBR	SD card CRC status busy register	
0x3817 to 0x381F	Reserved area	**Caution Do not access this area.**	–
0x3820	TIR	Timer initialize value register	Timer
0x3821	TCR	Timer count register	
0x3822	TCSR	Timer control / status register	
0x3823	TENR	Timer count enable register	
0x3824 to 0x382D	Reserved area	**Caution Do not access this area.**	–
0x382E	CLKCNTL	Clock control register	PLL
0x382F	Reserved area	**Caution Do not access this area.**	–
0x3830	PSAR	DMA start address register	SDCIF
0x3831	PSR	DMA size register	
0x3832	PRR	DMA pointer register	
0x3833	PCR	DMA control register	
0x3834 to 0x383F	Reserved area	**Caution Do not access this area.**	–

Cautions 1. The register names listed in this table are not reserved words of the assembler or the C language. Therefore, when using these names in assembler or C, the user must define them.

2. The same register is accessed, as long as the address is the same, regardless of whether the X memory space or Y memory space is accessed.

3. Even different registers cannot be accessed at the same time from both the X and Y memory spaces.

7. INSTRUCTIONS

7.1 Outline of Instructions

An instruction consists of 32 bits. Almost all the instructions, except some such as branch instructions, are executed with one system clock. The maximum instruction cycle of the μPD77115 is 13.3 ns. The following nine types of instructions are available:

(1) Trinomial operation instructions

These instructions specify an operation by the MAC. As the operands, three general-purpose registers can be specified.

(2) Binomial operation instructions

These instructions specify an operation by the MAC, ALU, or BSFT. As the operands, two general-purpose registers can be specified. An immediate value can be specified for some of these instructions, instead of a general-purpose register, for one input.

(3) Uninominal operation instructions

These instructions specify an operation by the ALU. As the operands, one general-purpose register can be specified.

(4) Load/store instructions

These instructions transfer 16-bit values between memory and a general-purpose register. Any general-purpose register can be specified as the transfer source or destination.

(5) Register-to-register transfer instructions

These instructions transfer data from one general-purpose register to another.

(6) Immediate value setting instructions

These instructions write an immediate value to a general-purpose register and the registers of the address operation unit.

(7) Branch instructions

These instruction specify branching of program execution.

(8) Hardware loop instructions

These instruction specify repetitive execution of an instruction.

(9) Control instructions

These instructions are used to control the program.

7.2 Instruction Set and Operation

An operation is written in the operation field for each instruction in accordance with the operation representation format of that instruction. If two or more parameters can be written, select one of them.

(a) Representation formats and selectable registers

The following table shows the representation formats and selectable registers.

Representation Format	Selectable Register
r0, r0', r0"	R0 to R7
rl, rl'	R0L to R7L
rh, rh'	R0H to R7H
re	R0E to R7E
reh	R0EH to R7EH
dp	DP0 to DP7
dn	DN0 to DN7
dm	DMX, DMY
dpx	DP0 to DP3
dpy	DP4 to DP7
dpx_mod	DPn, DPn++, DPn– –, DPn##, DPn%%, !DPn## (n = 0 to 3)
dpy_mod	DPn, DPn++, DPn– –, DPn##, DPn%%, !DPn## (n = 4 to 7)
dp_imm	DPn##imm (n = 0 to 7)
*xxx	Contents of memory with address xxx <Example> If the contents of the DP0 register are 1000, *DP0 indicates the contents of address 1000 of the memory.

(b) Modifying data pointer

The data pointer is modified after the memory has been accessed. The result of modification becomes valid starting from the instruction that immediately follows. The data pointer cannot be modified.

Example	Operation
DPn	Nothing is done (value of DPn is not changed.)
DPn++	DPn ← DPn + 1
DPn– –	DPn ← DPn – 1
DPn##	DPn ← DPn + DNn (Adds value of corresponding DN0 to DN7 to DP0 to DP7.) Example: DP0 ← DP0 + DN0
DPn%%	(n = 0 to 3) DPn = ((DP$_L$ + DNn) mod (DMX + 1)) + DP$_H$
	(n = 4 to 7) DPn = ((DP$_L$ + DNn) mod (DMY + 1)) + DP$_H$
!DPn##	Reverses bits of DPn and then accesses memory. After memory access, DPn ← DPn + DNn
DPn##imm	DPn ← DPn + imm

(c) Instructions that can be simultaneously written

Instructions that can be simultaneously written are indicated by O.

(d) Status of overflow flag (OV)

The status of the overflow flag is indicated by the following symbol:

- • : Not affected
- ↕ : Set to 1 when overflow occurs

Caution If an overflow does not occur as a result of an operation, the overflow flag is not reset but retains the status before the operation.

Instruction Set

Instruction	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trinomial	Binomial	Uninominal	Load/store	Transfer	Immediate value	Branch	Loop	Control	OV
Trinomial operation	Multiply add	ro = ro + rh * rh'	ro ← ro + rh * rh'				√						↕
	Multiply sub	ro = ro – rh * rh'	ro ← ro – rh * rh'				√						↕
	Sign unsign multiply add	ro = ro + rh * rl (rl is in positive integer format.)	ro ← ro + rh * rl				√						↕
	Unsign unsign multiply add	ro = ro + rl * rl' (rl and rl' are in positive integer format.)	ro ← ro + rl * rl'				√						↕
	1-bit shift multiply add	ro = (ro>>1) + rh * rh'	ro ← $\frac{ro}{2}$ + rh * rh'				√						↕
	16-bit shift multiply add	ro = (ro>>16) + rh * rh'	ro ← $\frac{ro}{2^{16}}$ + rh * rh'				√						•
Binomial operation	Multiply	ro = rh * rh'	ro ← rh * rh'				√						•
	Add	ro" = ro + ro'	ro" ← ro + ro'				√						↕
	Immediate add	ro' = ro + imm	ro' ← ro + imm (where imm ≠ 1)										↕
	Sub	ro" = ro – ro'	ro" ← ro – ro'				√						↕
	Immediate sub	ro' = ro – imm	ro' ← ro – imm (where imm ≠ 1)										↕
	Arithmetic right shift	ro' = ro SRA rl	ro' ← ro >> rl				√						•
	Immediate arithmetic right shift	ro' = ro SRA imm	ro' ← ro >> imm										•
	Logical right shift	ro' = ro SRL rl	ro' ← ro >> rl				√						•
	Immediate logical right shift	ro' = ro SRL imm	ro' ← ro >> imm										•
	Logical left shift	ro' = ro SLL rl	ro' ← ro << rl				√						•
	Immediate logical left shift	ro' = ro SLL imm	ro' ← ro << imm										•
	AND	ro" = ro & ro'	ro" ← ro & ro'				√						•
	Immediate AND	ro' = ro & imm	ro' ← ro & imm										•
	OR	ro" = ro | ro'	ro" ← ro | ro'				√						•
	Immediate OR	ro' = ro | imm	ro' ← ro | imm										•
	Exclusive OR	ro" = ro ^ ro'	ro" ← ro ^ ro'				√						•
	Immediate exclusive OR	ro' = ro ^ imm	ro' ← ro ^ imm										•

Instruction	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trinomial	Binomial	Uninominal	Load/store	Transfer	Immediate value	Branch	Loop	Control	OV
Binomial operation	Less than	ro" = LT (ro, ro')	if (ro < ro') {ro" ← 0x0000000001} else {ro" ← 0x0000000000}				√						•
Uninominal operation	Clear	CLR (ro)	ro ← 0x0000000000				√					√	•
	Increment	ro' = ro + 1	ro' ← ro + 1				√					√	↕
	Decrement	ro' = ro – 1	ro' ← ro – 1				√					√	↕
	Absolute value	ro' = ABS (ro)	if (ro < 0) {ro' ← –ro} else {ro' ← ro}				√					√	↕
	1's complement	ro' = ~ro	ro' ← ~ro				√					√	•
	2's complement	ro' = –ro	ro' ← –ro				√					√	↕
	Clip	ro' = CLIP (ro)	if (ro > 0x007FFFFFFF) {ro' ← 0x007FFFFFFF} elseif {ro < 0xFF80000000} {ro' ← 0xFF80000000} else {ro' ← ro}				√					√	•
	Round	ro' = ROUND (ro)	if (ro > 0x007FFF0000) {ro' ← 0x007FFF0000} elseif {ro < 0xFF80000000} {ro' ← 0xFF80000000} else {ro' ← (ro + 0x8000) & 0xFFFFFF0000}				√					√	•
	Exponent	ro' = EXP (ro)	ro' ← $\log_2 (\frac{1}{ro})$				√					√	•
	Substitution	ro' = ro	ro' ← ro				√					√	•
	Accumulated addition	ro' + = ro	ro' ← ro' + ro				√					√	↕
	Accumulated subtraction	ro' – = ro	ro' ← ro' – ro				√					√	↕
	Division	ro' / = ro	if (sign (ro') == sign (ro)) {ro' ← (ro' – ro) << 1} else {ro' ← (ro' + ro)<<1} if (sign (ro')==0) {ro' ← ro' + 1}				√					√	↕

Instruction	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trinomial	Binomial	Uninominal	Load/store	Transfer	Immediate value	Branch	Loop	Control	OV
Load/store	Parallel load/store[Notes 1, 2]	ro = *dpx_mod ro' =*dpy_mod	ro ← *dpx, ro' ← *dpy	√	√	√							•
		ro = *dpx_mod *dpy_mod = rh	ro ← *dpx, *dpy ←rh										
		*dpx_mod = rh ro = *dpy_mod	*dpx ← rh, ro ← *dpy										
		*dpx_mod = rh *dpy_mod = rh'	*dpx ← rh, *dpy ← rh'										
	Partial load/store[Notes 1, 2, 3]	dest = *dpx_mod dest' = *dpy_mod	dest ← *dpx, dest' ← *dpy										•
		dest = *dpx_mod *dpy_mod = source	dest ← *dpx, *dpy ← source										
		*dpx_mod = source dest = *dpy_mod	*dpx ← source, dest ← *dpy										
		*dpx_mod = source *dpy_mod = source'	*dpx ← source, *dpy ← source'										
	Direct addressing load/store[Note 4]	dest = *addr	dest ← *addr										•
		*addr = source	*addr ← source										
	Immediate value index load/store[Note 5]	dest = *dp_imm	dest ← *dp										•
		*dp_imm = source	*dp ← source										
Register-to-register transfer	Register-to-register transfer[Note 6]	dest = rl	dest ← rl									√	•
		rl = source	rl ← source										
Immediate value setting	Immediate value setting	rl = imm (where imm = 0 to 0xFFFF)	rl ← imm										•
		dp = imm (where imm = 0 to 0xFFFF)	dp ← imm										
		dn = imm (where imm = 0 to 0xFFFF)	dn ← imm										
		dm = imm (where imm = 1 to 0xFFFF)	dm ← imm										

Notes 1. Of the two mnemonics, either one of them or both can be written.

2. After transfer, modification specified by mod is performed.

3. Select any of dest, dest' = {ro, reh, re, rh, rl}, source, source' = {re, rh, rl}.

4. Select any of dest = {ro, reh, re, rh, rl}, source = {re, rh, rl}, addr = $\left\{\begin{array}{l}0\text{: X-0xFFF : X (X memory)}\\0\text{: Y-0xFFFF: Y (Y memory)}\end{array}\right\}$.

5. Select any of dest = {ro, reh, re, rh, rl}, source = {re, rh, rl}.

6. Select any register other than general-purpose registers as dest and source.

Instruction	Instruction Name	Mnemonic	Operation	Instructions Simultaneously Written									Flag
				Trinomial	Binomial	Unionominal	Load/store	Transfer	Immediate value	Branch	Loop	Control	OV
Branch	Jump	JMP imm	PC ← imm									√	•
	Register indirect jump	JMP dp	PC ← dp									√	•
	Subroutine call	CALL imm	SP ← SP + 1 STK ← PC + 1 PC ← imm									√	•
	Register indirect subroutine call	CALL dp	SP ← SP + 1 STK ← PC + 1 PC ← dp									√	•
	Return	RET	PC ← STK SP ← SP − 1									√	•
	Interrupt return	RETI	PC ← STK STK ← SP − 1 Recovery of interrupt enable flag									√	•
Hardware loop	Repeat	REP count	Start RC ← count RF ← 0 During repeat PC ← PC RC ← RC − 1 End PC ← PC + 1 RF ← 1										•
	Loop	LOOP count (instruction of two or more lines)	Start RC ← count RF ← 0 During repeat PC ← PC RC ← RC − 1 End PC ← PC + 1 RF ← 1										•
	Loop pop	LPOP	LC ← LSR3 LE ← LSR2 LS ← LSR1 LSP ← LSP − 1										•
Control	No operation	NOP	PC ← PC + 1										•
	Halt	HALT	CPU stops.										•
	Stop	STOP	CPU, PLL, and OSC stop										•
	Condition	IF (ro cond)	Condition test			√		√		√			•
	Forget interrupt	FINT	Discard interrupt request										•

8. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = +25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	IV_{DD}	For DSP core	−0.5 to +3.6	V
	EV_{DD}	For I/O pins	−0.5 to +4.6	V
Input voltage	V_I	$V_I < EV_{DD}$ + 0.5 V	−0.5 to +4.1	V
Output voltage	V_O		−0.5 to +4.1	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_A		−40 to +85	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage	IV_{DD}	For DSP core	2.0		2.7	V
	EV_{DD}	For I/O pins	2.7		3.6	V
Input voltage	V_I		0		EV_{DD}	V

Capacitance (T_A = +25°C, IV_{DD} = 0 V, EV_{DD} = 0 V)

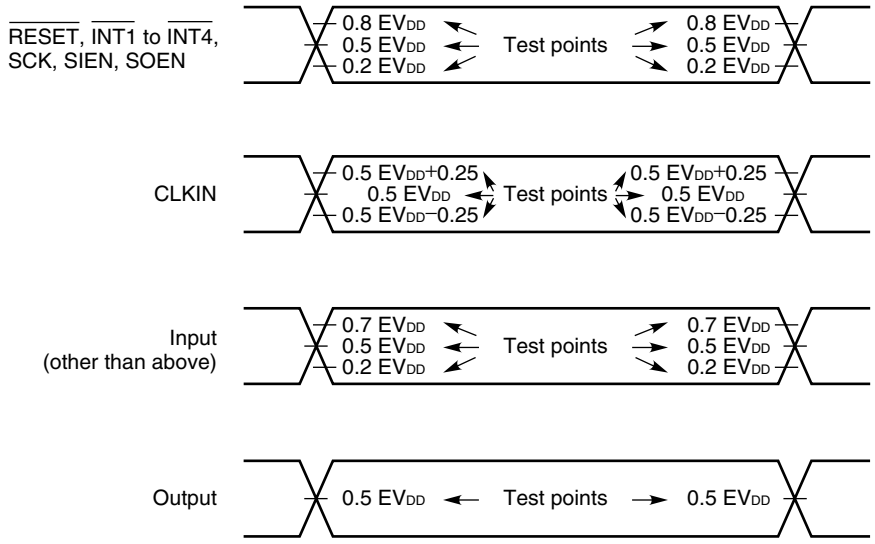
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz, Pins other than those tested: 0 V		10		pF
Output capacitance	C_O			10		pF
I/O capacitance	C_{IO}			10		pF

DC Characteristics (Unless otherwise specified, T_A = – 40 to + 85°C, with IV_{DD} and EV_{DD} within recommended operating condition range)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IHN}	Pins other than below	0.7 EV_{DD}		EV_{DD}	V
	V_{IHS}	$\overline{RESET}$, $\overline{INT1}$ to $\overline{INT4}$, SCK, SIEN, SOEN	0.8 EV_{DD}		EV_{DD}	V
	V_{IHC}	CLKIN	0.5 EV_{DD} +0.25		EV_{DD}	V
Low-level input voltage	V_{IL}	Pins other than below	0		0.2 EV_{DD}	V
	V_{IC}	CLKIN	0		0.5 EV_{DD} –0.25	V
High-level output voltage	V_{OH}	I_{OH} = –2.0 mA	0.7 EV_{DD}			V
		I_{OH} = –100 μA	0.8 EV_{DD}			V
Low-level output voltage	V_{OL}	I_{OL} = 2.0 mA			0.2 EV_{DD}	V
High-level input leakage current	I_{LH}	Other than TDI, TMS, and $\overline{TRST}$ $V_I = EV_{DD}$	0		10	μA
Low-level input leakage current	I_{LL}	Other than TDI, TMS, and $\overline{TRST}$ V_I = 0 V	–10		0	μA
Pull-up pin current	I_{PUI}	TDI, TMS, 0 V ≤ V_I ≤ EV_{DD}	–250		0	μA
Pull-down pin current	I_{PDI}	$\overline{TRST}$, 0 V ≤ V_I ≤ EV_{DD}	0		250	μA
Internal supply current [V_{IHN} = V_{IHS} = EV_{DD}, V_{IL} = 0 V, no load]	I_{DD}[Note]	During operating, 30 ns, IV_{DD} = 2.7 V		TBD	75	mA
	I_{DDH}	In halt mode, t_{cC} = 30 ns, divided by eight, IV_{DD} = 2.7 V		TBD	10	mA
	I_{DDS}	In stop mode, 0°C < T_A < 60°C			100	μA

Note The TYP. values are when an ordinary program is executed.
The MAX. values are when a special program that brings about frequent switching inside the device is executed.

Common Test Criteria of Switching Characteristics



AC Characteristics (T_A = – 40 to + 85°C, with IV_{DD} and EV_{DD} within recommended operating condition range)

Clock

Timing requirements

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
★ CLKIN cycle time[Note 1]	t_{cCX}			25			ns
		PLL lock range[Note 2]	IV_{DD} = 2.0 to 2.7 V	15 × m		50 × m	ns
			IV_{DD} = 2.3 to 2.7 V	10 × m		50 × m	ns
CLKIN high-level width	t_{wCXH}			12.5			ns
CLKIN low-level width	t_{wCXL}			12.5			ns
CLKIN rise/fall time	t_{rfCX}					5	ns
Internal clock cycle time requirements[Note 3]	$t_{cC\ (R)}$	IV_{DD} = 2.0 to 2.7 V		20			ns
		IV_{DD} = 2.3 to 2.7 V		13.3			ns

Notes 1. m: Multiple

2. This is the range in which the PLL is locked (stably oscillates). Input t_{cCX} within this range.

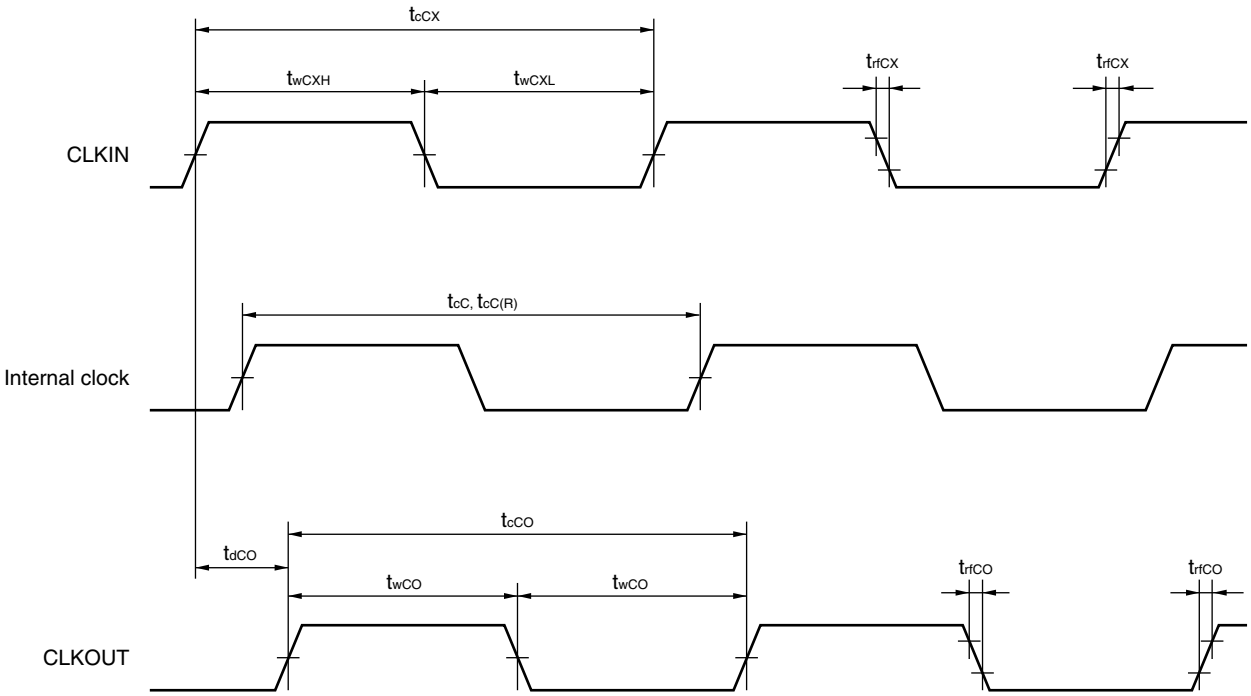
3. Input t_{cCX} so that the value of ($t_{cCX} \div m \times n$) satisfies this condition. m: Multiple, n: Division ratio

Switching characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Internal clock cycle[Note]	t_{cC}	External clock operation			t_{cCX}		ns
		PLL clock operation			($t_{cCX} \div m$) × n		ns
		In HALT mode			($t_{cCX} \div m$) × n × l		ns
CLKOUT cycle time	t_{cCO}				t_{cC}		ns
CLKOUT width	t_{wCO}	During normal operation	n = 1, or even number	$t_{cC} \div 2 - 3$			ns
			n = odd number (other than 1)	$t_{cC} \div n - 3$			ns
		In HALT mode		$t_{cC} \div n - 3$			ns
CLKOUT rise/fall time	t_{rfCO}					5	ns
CLKOUT delay time	t_{dCO}	IV_{DD} = 2.0 to 2.7 V				20	ns
		IV_{DD} = 2.3 to 2.7 V				15	ns

Note m: Multiple, n: Division ratio, l: HALT division ratio

Clock I/O timing



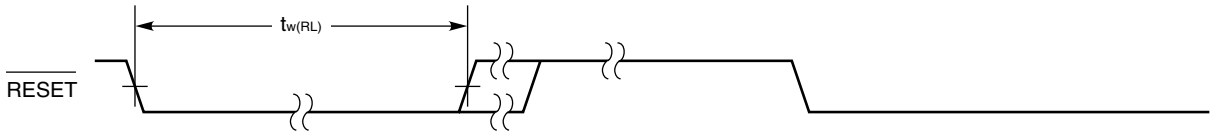
Reset, Interrupt

Timing requirements

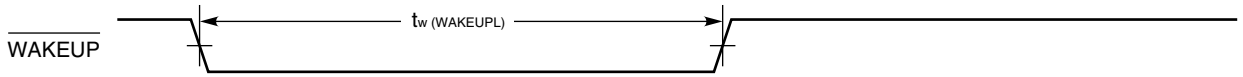
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	$t_{w\,(RL)}$		6 t_{CC}[Note]			ns
$\overline{\text{WAKEUP}}$ low-level width	$t_{w\,(WAKEUPL)}$		6 t_{CC}			μs
$\overline{\text{INT1}}$ to $\overline{\text{INT4}}$ low-level width	$t_{w\,(INTL)}$		3 t_{CC}[Note]			ns
$\overline{\text{INT1}}$ to $\overline{\text{INT4}}$ recovery time	$t_{rec\,(INT)}$		3 t_{CC}			ns

Note Note that t_{CC} is I (I = integer of 1 to 16) times that during normal operation in the HALT mode.

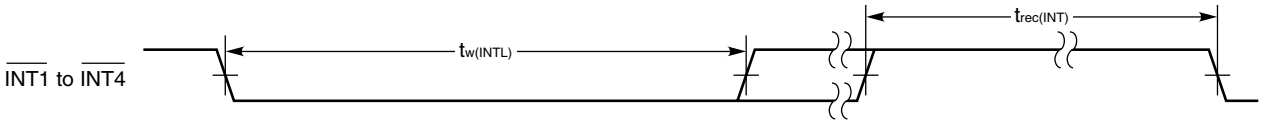
Reset timing



★ **WAKEUP timing**



Interrupt timing



Serial Interface (Audio Serial mode)

Timing requirements

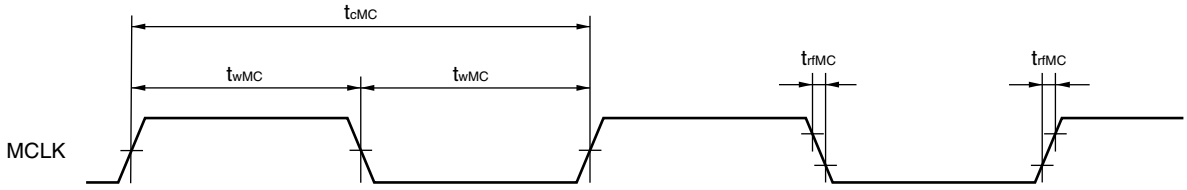
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MCLK cycle time	t_{cMC}	Master mode	40			ns
MCLK high-/low-level width	t_{wMC}	Master mode	0.4 × t_{cMC}			ns
MCLK rise/fall time	t_{rfMC}	Master mode			**Note**	ns
BCLK cycle time	t_{cBC}	Slave mode	300			ns
BCLK high-/low-level width	t_{wBC}	Slave mode	120			ns
BCLK rise/fall time	t_{rfBC}	Slave mode			20	ns
LRCLK setup time	$t_{su(BC-LR)}$	Slave mode	50			ns
SI setup time	t_{suSI}		50			ns
SI hold time	t_{hSI}		50			ns

Note 5 or maximum value of 0.1 × t_{cMC}

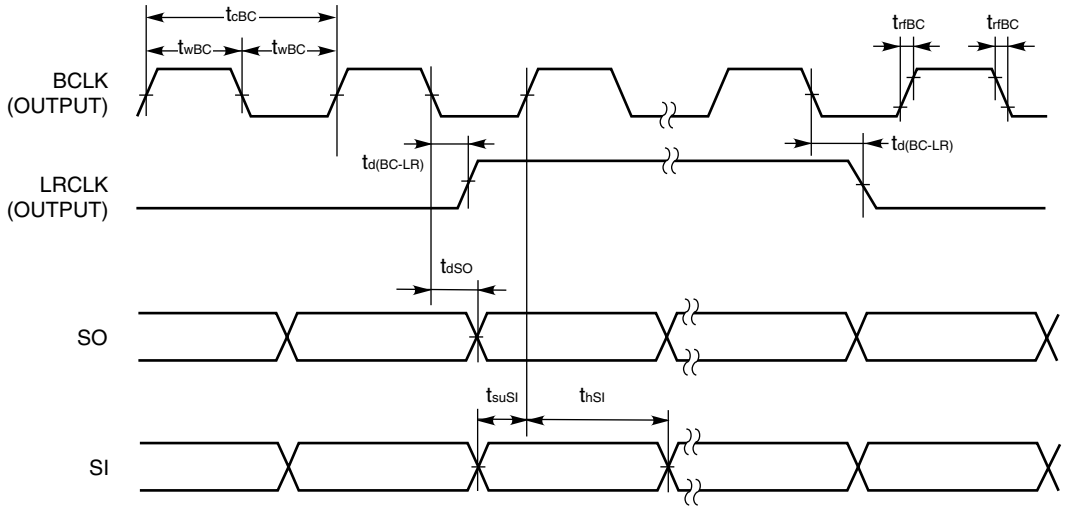
Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
BCLK cycle time	t_{cBC}	Master mode, 64-bit mode		1/64 fs		ns
		Master mode, 32-bit mode		1/32 fs		ns
BCLK high-/low-level width	t_{wBC}	Master mode	0.4 t_{cBC}			ns
BCLK rise/fall time	t_{rfBC}	Master mode			20	ns
LRCLK delay time	$t_{d(BC-LR)}$	Master mode	−40		+40	ns
SO output delay time	t_{dSO}		−40		+40	ns

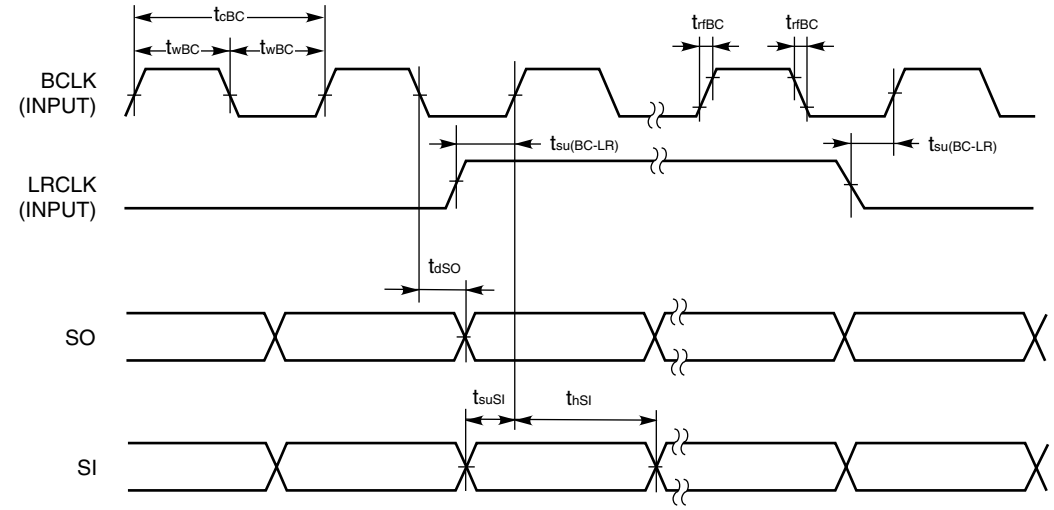
Audio Serial clock timing



Audio Serial Master mode timing



Audio Serial Slave mode timing



Serial Interface (Standard Serial mode)

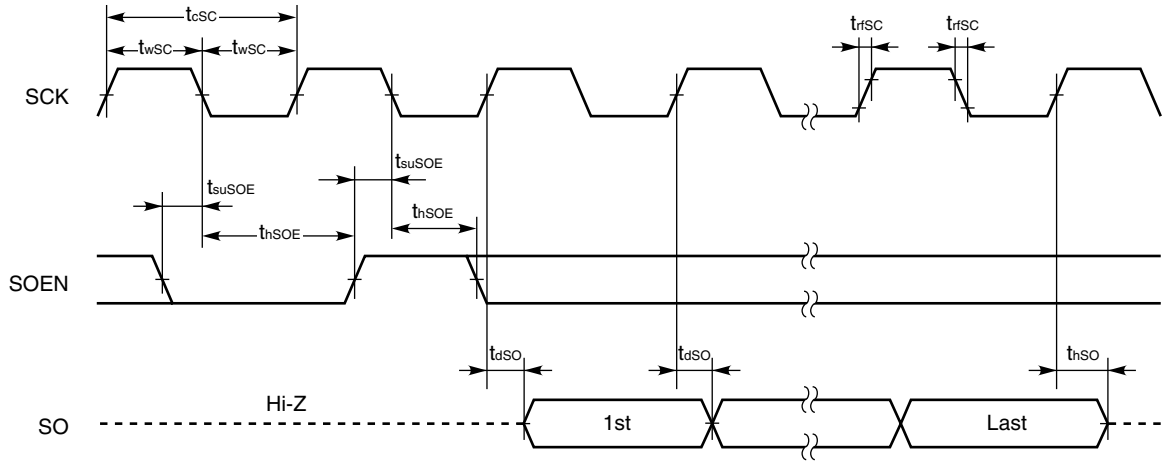
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCK cycle time	t_{cSC}		60 and $2t_{cC}$			ns
SCK high-/low-level width	t_{wSC}		25			ns
SCK rise/fall time	t_{rfSC}				20	ns
SOEN setup time	t_{suSOE}	IV_{DD} = 2.0 to 2.7 V	10			ns
		IV_{DD} = 2.3 to 2.7 V	5			ns
SOEN hold time	t_{hSOE}	IV_{DD} = 2.0 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns
SIEN setup time	t_{suSIE}	IV_{DD} = 2.0 to 2.7 V	10			ns
		IV_{DD} = 2.3 to 2.7 V	5			ns
SIEN hold time	t_{hSIE}	IV_{DD} = 2.0 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns
SI setup time	t_{suSI}	IV_{DD} = 2.0 to 2.7 V	10			ns
		IV_{DD} = 2.3 to 2.7 V	5			ns
SI hold time	t_{hSI}	IV_{DD} = 2.0 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns

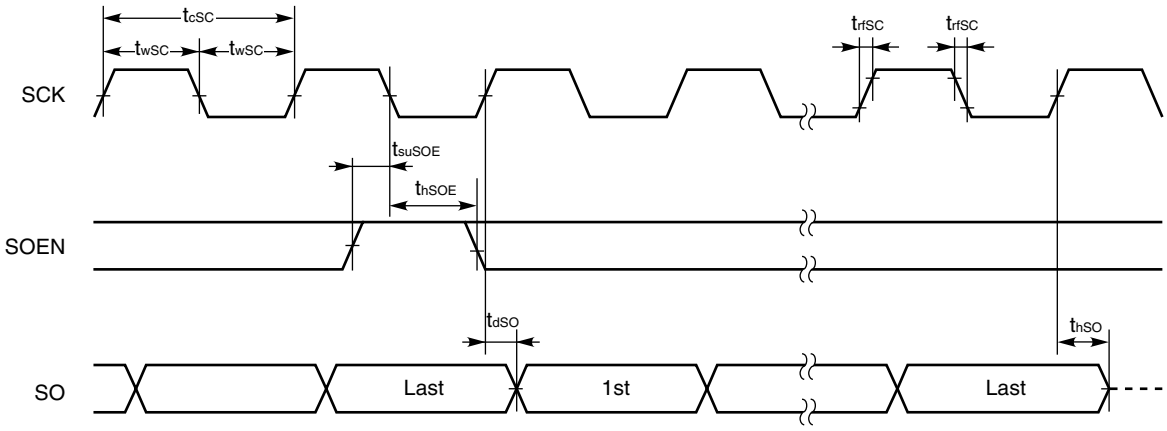
Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SO output delay time	t_{dSO}	IV_{DD} = 2.0 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
SO hold time	t_{hSO}		0			ns

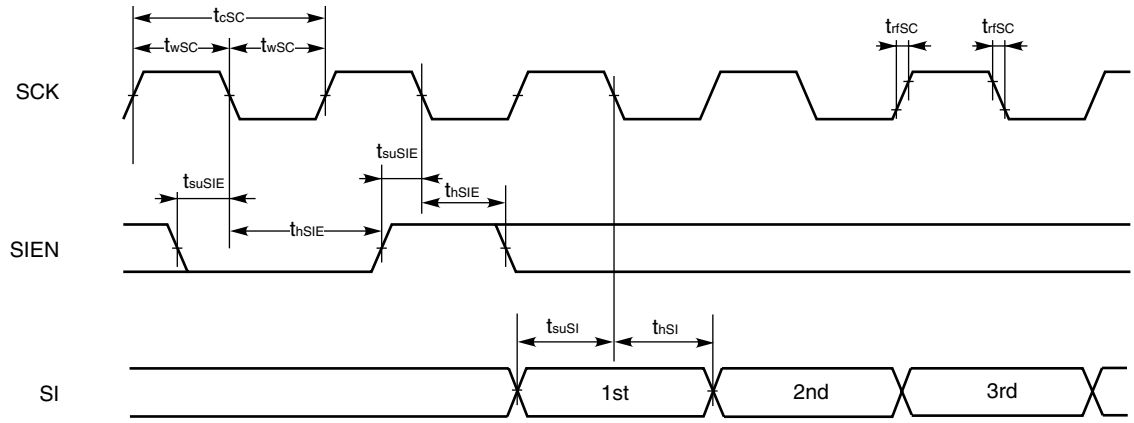
Serial output timing 1



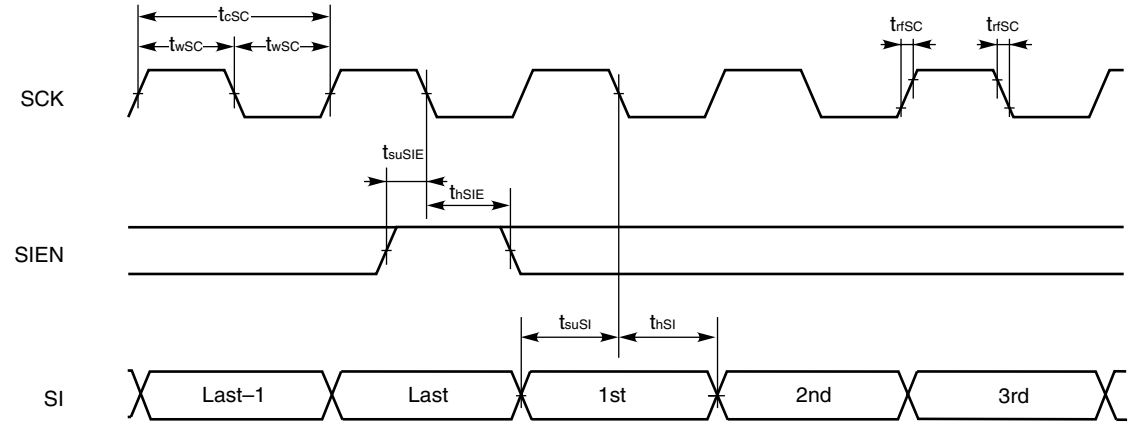
Serial output timing 2 (during successive output)



Serial input timing 1

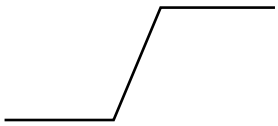


Serial input timing 2 (during successive input)



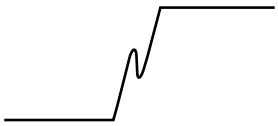
Caution If noise is superimposed on the serial clock, the serial interface may be deadlocked. Bear in mind the following points when designing your system:

- **Reinforce the wiring for power supply and ground (if noise is superimposed on the power and ground lines, it has the same effect as if noise were superimposed on the serial clock).**
- **Shorten the wiring between the device's SCK pin, and clock supply source.**
- **Do not cross the signal lines of the serial clock with any other signal lines. Do not route the serial clock line in the vicinity of a line through which a high alternating current flows.**
- **Supply the clock to the SCK pin of the device from the clock source on a one-to-one basis. Do not supply clock to several devices from one clock source.**
- **Exercise care that the serial clock does not overshoot or undershoot. In particular, make sure that the rising and falling of the serial clock waveform are clear.**



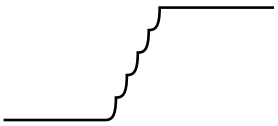
○

Make sure that the serial clock rises and falls linearly.



×

The serial clock must not bound. Noise must not be superimposed on the serial clock.



×

The serial clock must not rise or fall step-wise.

Host Interface

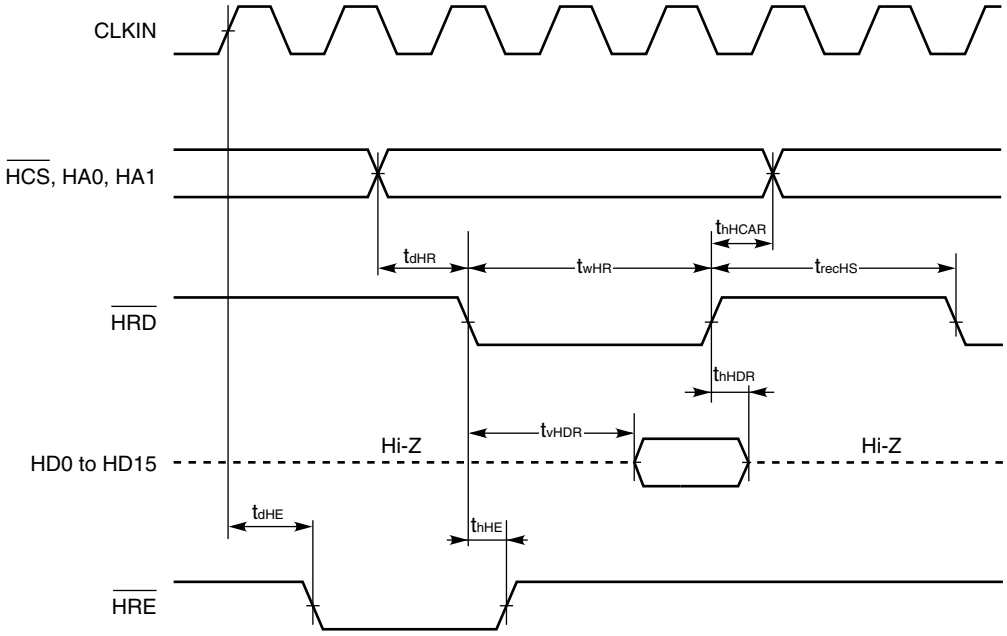
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{HRD}$ delay time	t_{dHR}	IV_{DD} = 2.0 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	5			ns
$\overline{HRD}$ width	t_{wHR}		40			ns
$\overline{HCS}$, HA0, HA1, read hold time	t_{hHCAR}		0			ns
$\overline{HCS}$, HA0, HA1 write hold time	t_{hHCAW}		0			ns
$\overline{HRD}$, $\overline{HWR}$ recovery time	t_{recHS}		$3t_{cC}$			ns
$\overline{HWR}$ delay time	t_{dHW}	IV_{DD} = 2.0 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns
$\overline{HWR}$ width	t_{wHW}		40			ns
$\overline{HWR}$ hold time	t_{hHDW}		0			ns
$\overline{HWR}$ setup time	t_{suHDW}	IV_{DD} = 2.0 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns

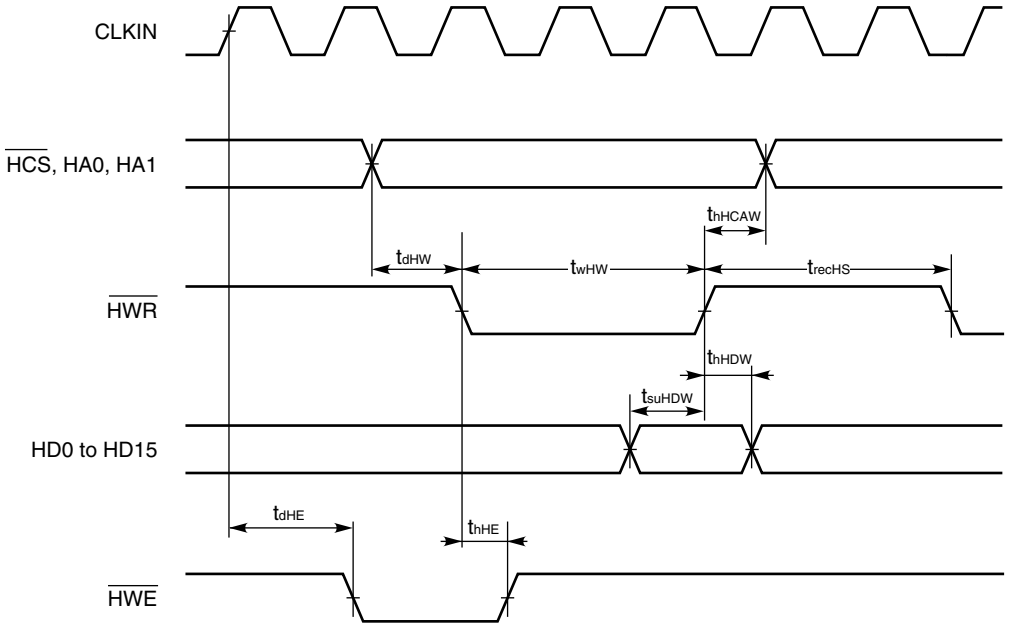
Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{HRE}$, $\overline{HWE}$ output delay time	t_{dHE}	IV_{DD} = 2.0 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
$\overline{HRE}$, $\overline{HWE}$ hold time	t_{hHE}	IV_{DD} = 2.0 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
$\overline{HRD}$ valid time	t_{vHDR}	IV_{DD} = 2.0 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns
$\overline{HRD}$ hold time	t_{hHDR}		0			ns

Host read interface timing



Host write interface timing



General-purpose I/O Port

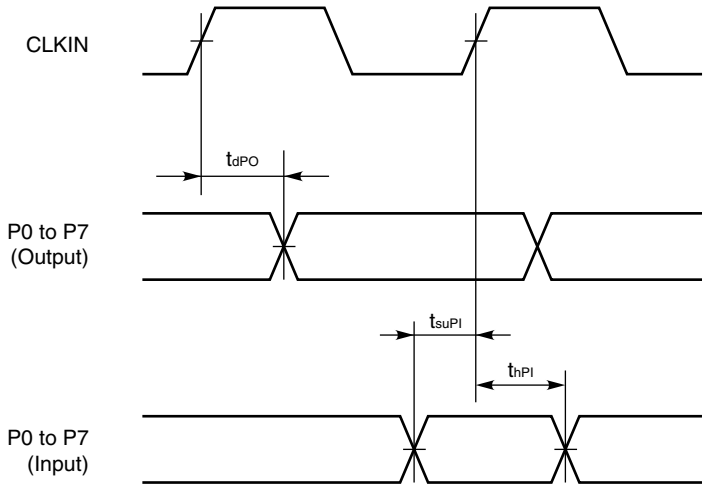
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Port input setup time	t_{suPI}		0			ns
Port input hold time	t_{hPI}	IV_{DD} = 2.0 to 2.7 V	15			ns
		IV_{DD} = 2.3 to 2.7 V	10			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Port output delay time	t_{dPO}	IV_{DD} = 2.0 to 2.7 V			30	ns
		IV_{DD} = 2.3 to 2.7 V			25	ns

General-purpose I/O port timing



SD card Interface

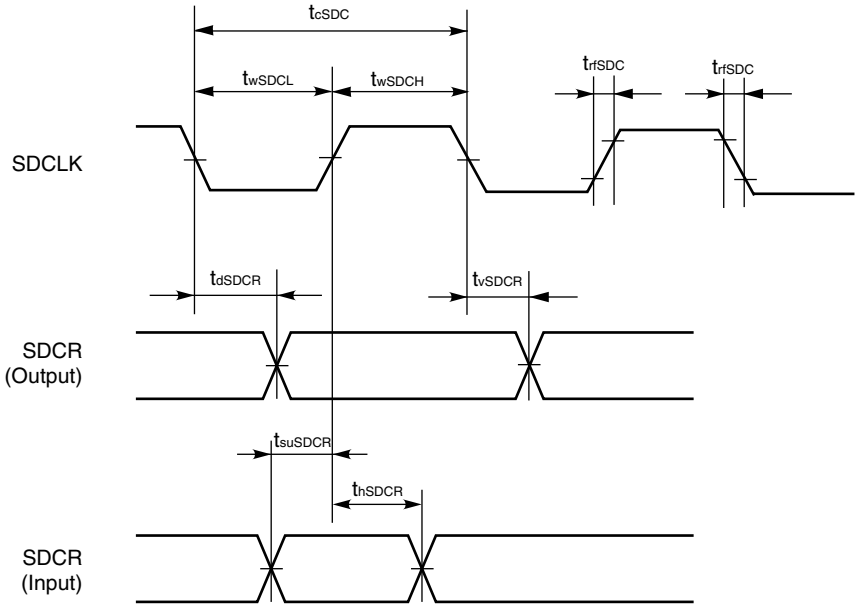
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SDCR input setup time	t_{suSDCR}	Input Response	5			ns
SDCR input hold time	t_{hSDCR}	Input Response	0			ns
SDDAT input setup time	t_{suSDD}	Input data	5			ns
SDDAT input hold time	t_{hSDD}	Input data	0			ns

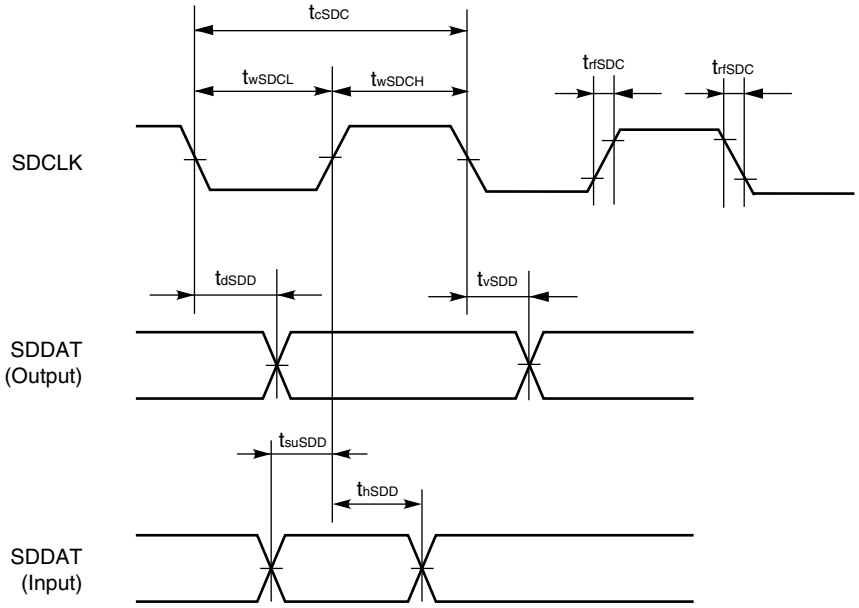
Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SDCLK cycle time	t_{cSDC}		40			ns
SDCLK high- level width	t_{wSDCH}		10			ns
SDCLK low-level width	t_{wSDCL}		10			ns
SDCLK rise/fall time	t_{rfSDC}				10	ns
SDCR output delay time	t_{dSDCR}	Output Command			10	ns
SDCR output valid time	t_{vSDCR}	Output Command	0			ns
SDDAT output delay time	t_{dSDD}	Output data			10	ns
SDDAT output valid time	t_{vSDD}	Output data	0			ns

SDCR timing



SDDAT timing



Debugging Interface (JTAG)

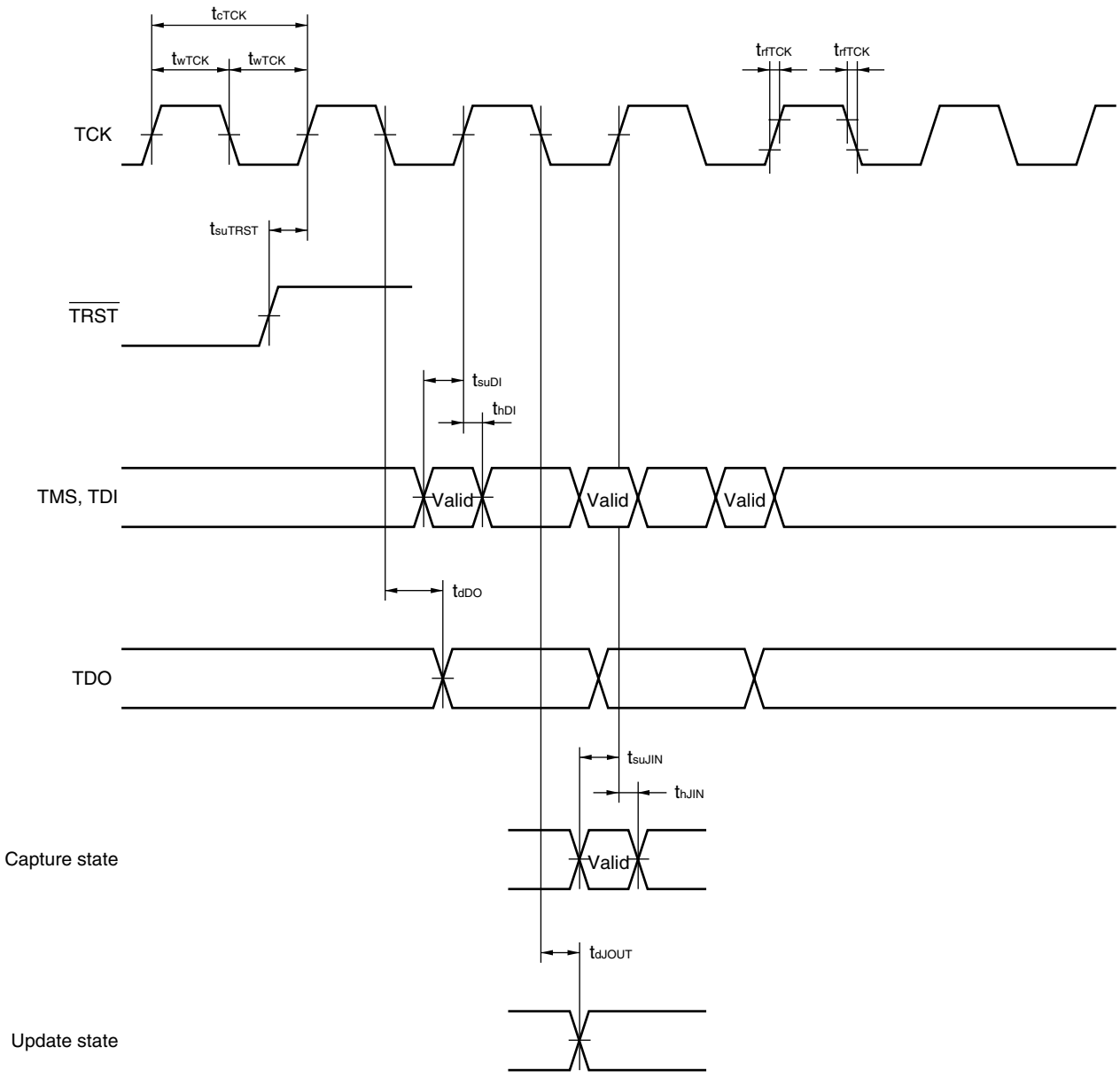
Timing requirements

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK cycle time	t_{cTCK}		120			ns
TCK high-/low-level width	t_{wTCK}		50			ns
TCK rise/fall time	t_{rfTCK}				20	ns
TMS, TDI setup time	t_{suDI}	IV_{DD} = 2.0 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
TMS, TDI hold time	t_{hDI}	IV_{DD} = 2.0 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
Input pin setup time	t_{suJIN}	IV_{DD} = 2.0 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
Input pin hold time	t_{hJIN}	IV_{DD} = 2.0 to 2.7 V	25			ns
		IV_{DD} = 2.3 to 2.7 V	20			ns
$\overline{\text{TRST}}$ setup time	t_{suTRST}		100			ns

Switching characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TDO output delay time	t_{dDO}	IV_{DD} = 2.0 to 2.7 V			25	ns
		IV_{DD} = 2.3 to 2.7 V			20	ns
Output pin output delay time	t_{dJOUT}	IV_{DD} = 2.0 to 2.7 V			25	ns
		IV_{DD} = 2.3 to 2.7 V			20	ns

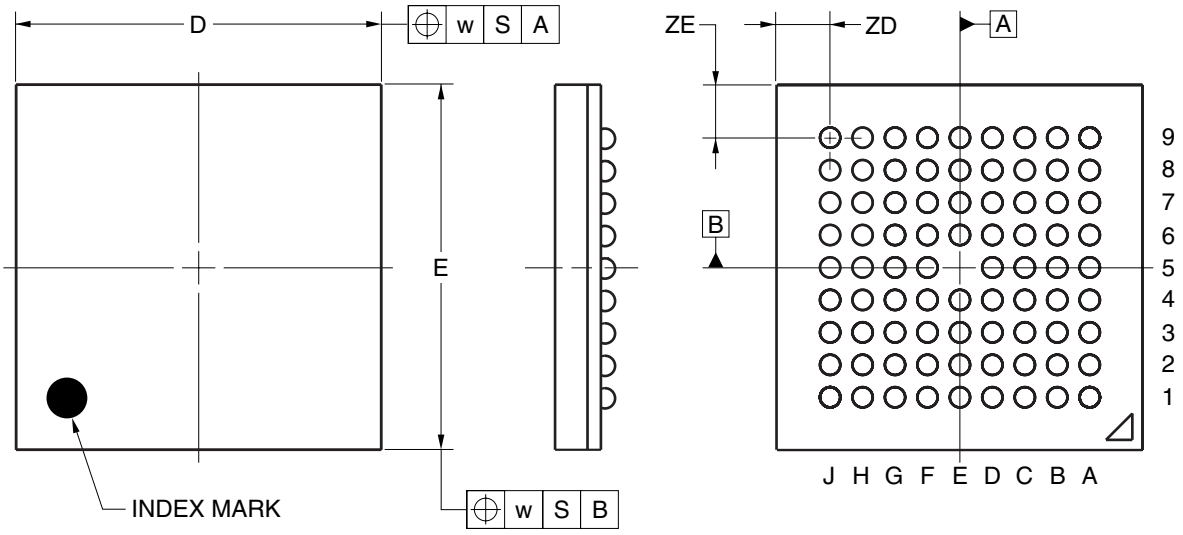
Debugging interface timing

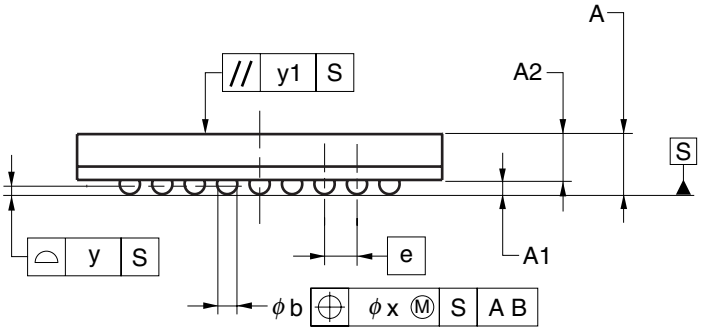


Remark For details of JTAG, refer to **IEEE1149.1**.

9. PACKAGES

★ 80-PIN PLASTIC FBGA (9x9)



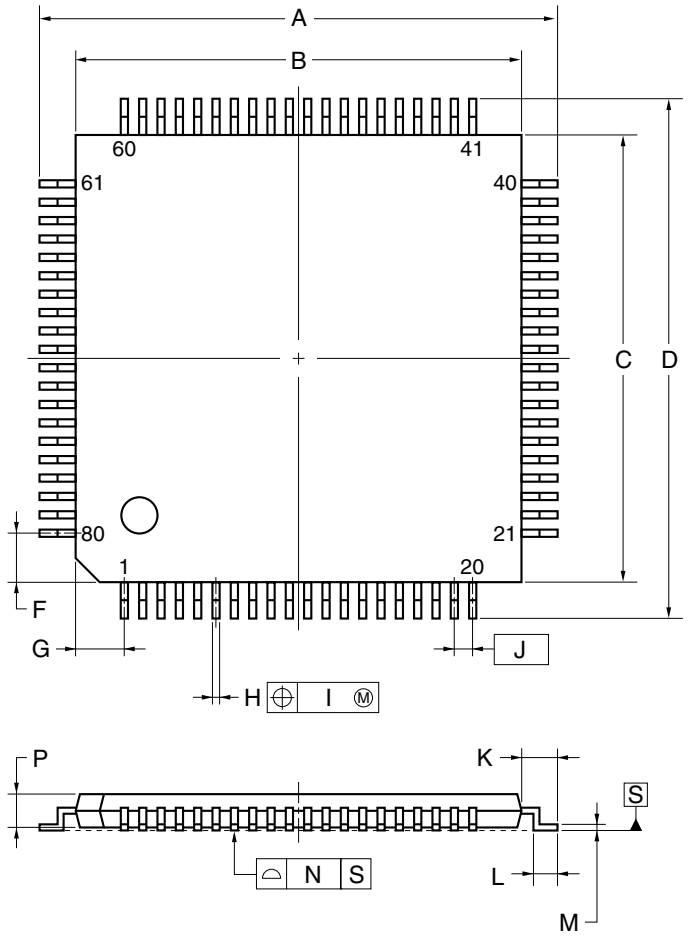


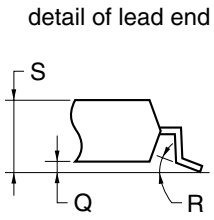
(UNIT:mm)

ITEM	DIMENSIONS
D	9.00±0.10
E	9.00±0.10
w	0.20
A	1.28±0.10
A1	0.35±0.06
A2	0.93
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.30
ZE	1.30

P80F1-80-CN6

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)





NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	0.145±0.05
N	0.10
P	1.0±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.

S80GK-50-9EU-1

10. RECOMMENDED SOLDERING CONDITIONS

It is recommended to solder this product under the following conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Surface-Mount Type

• μPD77115GK-9EU: 80-pin plastic TQFP (fine-pitch) (12 × 12)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Time: 30 seconds MAX (210°C MIN), Number of times: 2 MAX, Number of days: 3Note (after that, prebaking is necessary for 10 to 72 hours at 125°C))	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds MAX (200°C MIN), Number of times: 2 MAX, Number of days: 3Note (after that, prebaking isnecessary for 10 to 72 hours at 125°C)	VP15-103-2
Partial heating method	Pin temperature: 300°C MAX, Time: 3 seconds MAX (per side of device)	−

★ • μPD77115F1-CN6: 80-pin plastic FBGA (9 × 9)

★ • μPD77115AF1-xxx-CN6: 80-pin plastic FBGA (9 × 9)

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Time: 30 seconds MAX (210°C MIN), Number of times: 2 MAX, Number of days: 3Note (after that, prebaking is necessary for 10 to 72 hours at 125°C))	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds MAX (200°C MIN), Number of times: 2 MAX, Number of days: 3Note (after that, prebaking isnecessary for 10 to 72 hours at 125°C)	VP15-103-2

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25°C, 65% RH MAX.

Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC Electronics product in your application, please contact the NEC Electronics office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

[GLOBAL SUPPORT]
http://www.necel.com/en/support/support.html

NEC Electronics America, Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65030

- **Sucursal en España**
  Madrid, Spain
  Tel: 091-504 27 87
- **Succursale Française**
  Vélizy-Villacoublay, France
  Tel: 01-30-67 58 00
- **Filiale Italiana**
  Milano, Italy
  Tel: 02-66 75 41
- **Branch The Netherlands**
  Eindhoven, The Netherlands
  Tel: 040-244 58 45
- **Tyskland Filial**
  Taeby, Sweden
  Tel: 08-63 80 820
- **United Kingdom Branch**
  Milton Keynes, UK
  Tel: 01908-691-133

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-558-3737

NEC Electronics Shanghai Ltd.
Shanghai, P.R. China
Tel: 021-5888-5400

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 6253-8311

J04.1

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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